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ELECTRONIC DEVICES AND CIRCUITS



BALBIR KUMAR
SHAIL B. JAIN

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Electronic Devices and Circuits

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Electronic Devices and Circuits

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ELECTRONIC DEVICES AND CIRCUITS
Balbir Kumar and Shail B. Jain

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Preface

This book has been developed based on our teaching experience to the undergraduate students over the past several years. The aim is to provide finer explanations and detailed derivations at every step so that even an average student is at ease with the subject. The entire book has been evolved from the lecture notes prepared by us.

The book has been designed as a textbook for covering the core course in electronics, an essential course for the students of various engineering streams such as electronics and communication engineering, electrical engineering, computer science and engineering, IT, instrumentation and control, and mechanical engineering.

There are 13 chapters in this book. The first chapter covers the basic physics of the most commonly used semiconductor materials, i.e., Germanium (Ge) and Silicon (Si). The properties of the first semiconductor device, a *pn* junction diode, have been discussed in Chapter 2. Various applications of *pn* junction diode such as the rectifier, clipping and clamping are analyzed in Chapter 3.

Most of the electronic systems use Bipolar Junction Transistor (BJT) and Field Effect Transistor (FET) as the main active device for the purpose of amplification and signal processing. Analysis of these devices has been done in separate chapters due to their importance. The internal structure, *V-I* characteristics, small-signal models of a BJT are included in Chapter 4. For a BJT, three small signal models viz., *h*-parameter model, hybrid-π model and r_e-model are available in the literature. Various authors prefer only one type of the model and perform the analysis. We, however, in this book, have described all the three models and explored their advantages and disadvantages. Chapter 5 presents biasing (dc) conditions for realizing distortion-free operation of an amplifier. Issues regarding stability of operating point have also been explained in this chapter.

Analysis of various BJT amplifier configurations (CE, CC, CB) using all the three small signal models has been presented in Chapter 6. A student should be able to analyze the given circuit with any of the three models with equal ease. However, as hybrid-π model is more practical and provides exact analysis, more emphasis has been given on this model in the remaining chapters.

By the end of Chapter 6, students should have totally grasped the working and analysis of BJT circuits. This provides necessary background to understand the FET operation and analysis of its circuits. FET, the other important three terminal active device with a number of features better than the BJT, has been introduced in Chapter 7 and various FET amplifier configurations have been analyzed in Chapter 8.

Cascading of amplifier stages is a necessary requirement of many electronic systems; various methods of coupling stages are treated in Chapter 9. Differential amplifier, which is the basic building block of operational amplifier, is also addressed in this chapter. The behaviour of any electronic circuit changes at high frequencies and therefore, the reactance of various junction capacitances can not be neglected. High frequency response of a BJT and FET amplifier in different configurations are given in Chapter 10.

The concept of feedback in amplifiers is introduced in Chapter 11. Analysis of different types of feedback amplifier topologies have been reviewed. Chapter 12 deals with the principle of oscillation and analyzes various types of oscillator circuits. The power amplifier or large signal amplifiers and voltage regulators have been covered in Chapter 13.

In every chapter, the device characteristics used are for the commonly available devices so that the students can get a feel of the order of magnitude of device parameters. A large number of solved examples have been provided in every chapter. At the end of each chapter, summary highlighting the important points in the chapter has been included. Further, a number of intelligent review questions are given at the end of each chapter. Students are advised to go through the summary and grasp each point once the chapter is completed. And, then they should assess themselves by answering all the review questions. A good number of unsolved problems with answers are also included.

The authors will be glad to get feedback and suggestions from the faculty and the students so that the efforts could be made to further improve the text.

The authors are thankful to all those who knowingly or unknowingly have been a source of inspiration in writing this book.

Last but not the least, we wish to thank our families for their continuous support and encouragement during the preparation of this manuscript.

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CHAPTER 1

Semiconductor Physics

1.1 INTRODUCTION

In this chapter, we give a brief review of physics and some other associated phenomena necessary to understand the basics of Electronics and Electronic Devices. We first explain, in brief, the basic quantities such as forces, fields and energy which are necessary to explain the effects of charged particles and their motion. Then we explain the mechanism of conduction in metals and in semiconductors. The concept of electrons and holes as the charge carriers in extrinsic semiconductors is clarified. The Mass-action law associated with the extrinsic semiconductors is explained. Thereafter, the phenomenon of Diffusion and Drift is given, followed by Einstein Relationship. Finally, the contact potential difference for the case of most commonly used junction (i.e., Step-graded Junction) is derived.

It will be useful to list some important physical constants, and these are given in Table 1.1.

Table 1.1 Values of Important Physical Constants

S. No.	*Constant*	*Symbol*	*Value*
1.	Electronic charge	q	1.602×10^{-19} C
2.	Electronic mass	m	9.109×10^{-31} kg
3.	Ratio of charge to mass of an electron	q/m	1.759×10^{11} C/kg
4.	Mass of atom of unit atomic wt. (hypothetical)	...	1.660×10^{-27} kg
5.	Mass of proton	m_p	1.673×10^{-27} kg
6.	Ratio of proton to electron mass	m_p/m	1.837×10^{3}
7.	Planck's constant	h	6.626×10^{-34} Js
8.	Boltzmann constant	$\bar{k}$	1.381×10^{-23} J/K
9.	Stefan–Boltzmann constant	σ	5.670×10^{-8} W/(m^2 K^4)

(Contd.)

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Table 1.1 Values of Important Physical Constants (Contd.)

S. No.	Constant	Symbol	Value
10.	Avogadro number	N_A	6.023×10^{23} molecules per mol
11.	Gas constant	R	8.314 J/(deg. mol)
12.	Velocity of light (approx.)	c	3×10^8 m/s
13.	Faraday's constant	F	9.649×10^3 C/mol
14.	Volume per mole	V_0	2.241×10^{-2} m^3
15.	Acceleration due to gravity	g	9.807 m/s^2
16.	Permeability of free space = $4\pi \times 10^{-7}$	μ_0	1.257×10^{-6} H/m
17.	Permittivity of free space = $\frac{1}{36\pi} \times 10^{-9}$	ε_0	8.849×10^{-12} F/m
18.	1 electron volt (eV) equals $q \times 1$ volt and is the potential energy	eV	1.6×10^{-19} joules
19.	Boltzmann constant (another form)	k	8.620×10^{-5} eV/K

1.2 FORCES, FIELDS AND ENERGY

The controlled flow of charged particles is fundamental to the operation of all electronic devices. The materials used in these devices, therefore, must be capable to provide a source of mobile charge and the flow of charges must be controllable. The electrical characteristics which distinguish the material, whether it is an insulator, a semiconductor or a conductor are important parameters in Electronics. The two important processes for transporting the charge, and hence causing current are:

Drift: Drift is the motion of charges produced by an **electric field.** (Potential difference causes the electric field)

Diffusion: Diffusion is the motion resulting from a **non-uniform charge distribution**, i.e., due to charge density gradient.

Consider a wooden piece floating on the flowing water of a river (see Fig. 1.1). We say that the wooden piece is drifting due to force of flow of water.

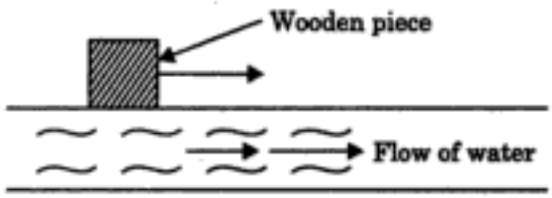


Fig. 1.1 Wooden piece drifting along the flow of water in the river.

Now, consider a chimney producing dense black smoke (see Fig. 1.2). As the nearby area has no/less smoke, the smoke from the chimney will diffuse on all sides in order to equalize the density of smoke. This phenomenon is called diffusion.

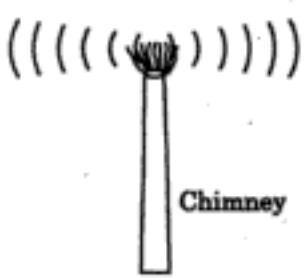


Fig. 1.2 Smoke from the chimney diffusing.

The aforementioned processes when applied to electric charges are explained in this chapter.

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1.2.1 Charged Particles

An electron has the physical parameters (approximately) as follows (see Table 1.1):

Charge of an electron q $= 1.60 \times 10^{-19}$ coulomb
Number of electrons $= 6 \times 10^{18}$ per coulomb
Mass of an electron m $\approx 9.1 \times 10^{-31}$ kg

Thus, about 6 trillion (6×10^{12}) electrons flow per second if the current I = charge/second, is 1 μA (1×10^{-6} A), i.e., a current of 1 pA ($= 10^{-12}$ A) amounts to flow of 6 million electrons per second.

An atom has a positive nucleus and a number of orbits having electrons. The nucleus together with charges of electrons in its orbits is overall neutral. We may consider the nucleus and all electronic orbits except the outermost as a +ve charged ion. This +ve charge is of course equal to the –ve charge of electrons in the outermost orbit. The valence electrons are the electrons in the outermost orbit. It may be possible, under certain circumstances, to remove or to add an electron in the outermost orbit. This would make the atom a +ve ion or a –ve ion. For example, the Sodium (Na) ion is +ve and Chlorine (Cl) ion is –ve, and both these ions combine to make NaCl (Sodium chloride, the common salt), which is a neutral molecule.

Silicon is tetravalent atom, i.e., there are four electrons in the outermost orbit of a Silicon atom. In Silicon crystal, each Silicon ion shares a pair of electrons with each of its *four neighbour Silicon ions*. Such a configuration is called a **covalent bond.** When an electron is missing from this structure the bond has one electron less thus termed as a **hole** in the bond. The atom with one electron missing from its outermost orbit may be termed as a **+ve charged ion.** Similarly, the structure may have an excess electron, thus simulating the condition of **–ve charged ion.** The holes (vacancies of electrons) may move from ion to ion in the crystal and produce the effect of motion of +ve charge (the hole). Each hole has a charge equal to that of an electron, in magnitude.

If, somehow, we add an electron (mass m, charge $-q$) to a neutral atom (of mass M, say), we get a negatively charged ion of mass $M + m$ and charge $-q$.

Of course mass m being much smaller than M, therefore, the overall mass of such a negatively charged ion is nearly equal to M. Similarly, if we remove a hole from a neutral atom (of mass M, say), the resultant positively charged ion has charge of $+q$ and overall mass of $M - m$ ($\approx M$). We may, therefore, assume that (an electron + a hole) equals zero charge and zero mass. Alternatively, we may replace a 'zero' by a hole-electron pair. We shall do so to explain the effect of doping (particularly, when dopant is a trivalent material).

1.2.2 Field Intensity ($\mathcal{E}$)

Let a charged particle (with charge q_1 coulomb) placed at $(x_1, 0)$ exerts a force F_x on another charged particle (with charge q_2 coulomb) placed at $(x_2, 0)$ such that

$$F_x = \frac{q_1 q_2}{4\pi\bar{\varepsilon}\,(x_2 - x_1)^2} \text{ newtons} \tag{1.1}$$

where F_x = Force in newtons (in x-axis direction for q_1, q_2 both being +ve)
q_1, q_2 = Charges in coulombs
$\bar{\varepsilon}$ = Permittivity of the medium in farads/m
x = Distances in metres (here separation distance is $x_2 - x_1$)

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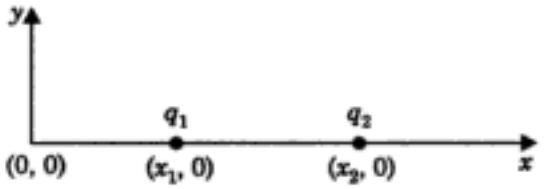


Fig. 1.3 Charges q_1, q_2 placed $(x_2 - x_1)$ apart exert force on each other.

Applying Newton's second law (Force = Mass × Acceleration) we may write, the force felt by particle with charge q_2 [assuming the particle with charge q_1, is stationary at $(x_1, 0)$] as:

$$F_x = \frac{q_1 q_2}{4\pi\bar{\varepsilon}(x_2 - x_1)^2} = \frac{d}{dt}(m_2 v_x) \text{ newton} \tag{1.2}$$

where m_2 is mass of q_2 and v_x is the velocity of q_2 in x-direction

$$\therefore \quad F_x = m_2 \frac{dv_x}{dt} = m_2 a_x \tag{1.3}$$

For a non-relativistic system, m_2 being constant, therefore, $a_x = dv_x/dt$, and is the acceleration in x-direction. We may also write Eq. (1.3) as:

$$F_x = \left(\frac{q_1}{4\pi\bar{\varepsilon}(x_2 - x_1)^2}\right).q_2 = \text{(Force exerted on unit charge)} \times \text{(Charge } q_2\text{)} \tag{1.4}$$

Thus, a convenient method for describing the effect on a charged particle with charge q, due to other charge is the use of field intensity, ε_x. We define ε_x as the force exerted on a unit +ve charge. Thus,

$$F_x = q\varepsilon_x \text{ newton} \tag{1.5}$$

Note that the value of F_x depends on q_1 and distance $(x_2 - x_1)$. But for a more generic case, there may be a number of different charges placed at various locations. ε_x signifies the overall effect of all these charges on a charge q, placed at a point $(x, 0)$.

Note that when q_1 is a +ve charge then it will repel a +ve charge towards +ve direction of x-axis (assuming x_2 is greater than x_1). Thus, the direction of the field intensity at a point is the direction in which a +ve charge would move when placed at that point. In Fig. 1.3, for q_1 and q_2 both assuming +ve charges, q_2 will move away from q_1 under the influence of field intensity ε_x. It resembles the situation of a body falling downward, along the direction of gravitational field. If we try to move q_2 towards q_1, we have to exert (i.e., do some work) against the electric field.

1.2.3 Potential (*V*)

Potential V (in volts) of a point B w.r.t. point A is the work done against the field in moving a unit positive charge from A to B. For point A at x_0 and B at x, we have

$$V = -\int_{x_0}^{x} \varepsilon_x \, dx \tag{1.6}$$

where ε_x represents the x component of the field. By differentiation, we get

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$$\varepsilon_x = -\frac{dV}{dx} \text{ V/m} \tag{1.7}$$

The **minus sign in Eqs. (1.6) and (1.7) indicates that the electric field is directed from** the region of higher **potential to a region of lower potential. Note that when we raise a body** of mass m from the **ground level to a height h, we are working against the gravitational force** (which is acting **downwards), and the body of mass m having raised to height h has potential** energy of mgh. Similarly, **here incremental work done against the field is** $-(\varepsilon_x \cdot dx)$, i.e., incremental potential raised **is** $-(\varepsilon_x \cdot dx)$ **and hence the net potential raised from** A **to** B **is** as given in Eq. (1.6).

We define **potential energy** U **as the product of the potential** V and the charge q, i.e.,

$$U = qV \text{ joules} \tag{1.8}$$

If we consider **an electron (with charge** $-q$**) then the potential energy of the electron is** $-qV$ joules. We **also use a unit *electron volt* given by**

$$1 \text{ electron volt} = 1.60 \times 10^{-19} \text{ joules} \tag{1.9}$$

Note that any **type of energy (electrical, mechanical, thermal or similar) may be expressed** in electrons volts.

If an electron falls **through a potential of 1 V, its kinetic energy increases and its** potential energy **decreases by 1 eV, i.e., by** 1.60×10^{-19} J.

Using law of conservations **of energy, we have**

$$\text{Total energy } W = \text{Potential energy } U + \text{Kinetic energy K.E.}$$

or
$$W = U + \frac{1}{2}mv^2 = \text{Constant} \tag{1.10}$$

1.2.4 Concept of Potential Barrier

Consider two **parallel plates** A **and** B **separated by a distance** x, **with plate** B **at a volt** $-V_d$ w.r.t. plate A. **[See Fig. 1.4(a)]**

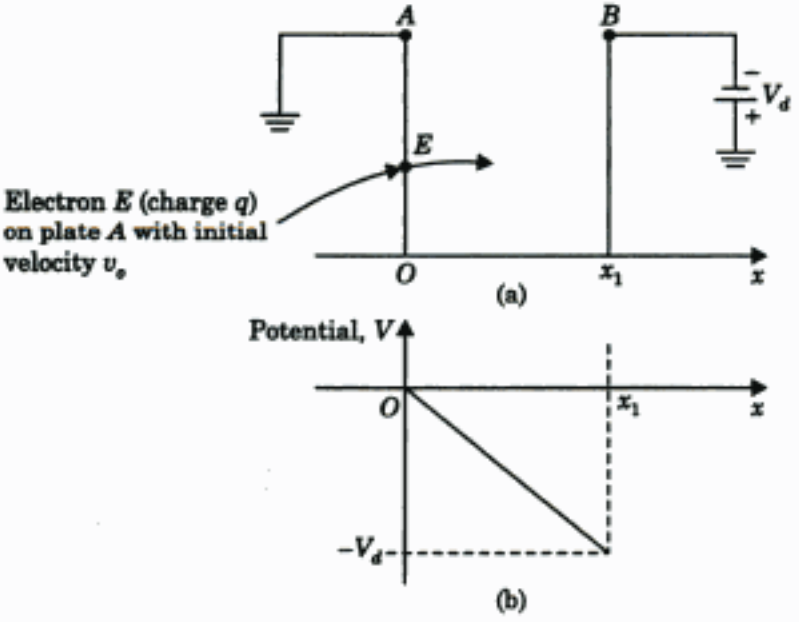


Fig. 1.4 (a) Parallel-plate system showing an electron leaving plate A with an initial velocity v_o and moving towards plate B, i.e., in a retarding field. (b) The potential between A and B.

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Let an electron E leaves the surface A with an initial velocity v_o in the x-direction. When this electron reaches B, let it have the velocity v (of course, $v < v_o$, due to retarding field). When the electron reaches B, it has acquired $(-q)(-V_d) = qV_d$ potential energy. By the law of conservation of energy, we have

$$\text{Total energy } W = \frac{1}{2}mv_0^2 = \frac{1}{2}mv^2 + qV_d \text{ joules} \tag{1.11}$$

We have assumed kinetic energy of the electron E at plate A as $\frac{1}{2}mv_0^2$ (and zero potential energy while at plate A, being earthed).

The final velocity v attained by the electron in this system (where W is constant) is independent of the form of field distribution, as long as the plate B is at $-V_d$ volts w.r.t. plate A. For the electron E to reach plate B, $\frac{1}{2}mv_0^2$ must be larger than qV_d, so that $\frac{1}{2}mv^2$ (the K.E. at $x = x_1$) is +ve, and the K.E. of the electron (due to velocity v_0) overcomes the repulsive force of plate B in moving from plate A to plate B.

Assuming that the electrodes A and B are large compared to the separation distance x_1, we may assume the plot of potential versus distance (linear plot), between plates A and B, as shown in Fig. 1.4(b).

It is clear that higher is the value of V_d (i.e., the plate B being more negative w.r.t. the plate A), higher is the K.E. required by the electron at A in order to reach plate B. The voltage V_d (which prevents electron at plate A to reach plate B) is called the **barrier voltage.** In other words, we must overcome the potential barrier to cause conduction. We shall see in the chapter on diode that we must apply an external voltage greater than voltage V_d to overcome the barrier effect of V_d volts.

1.3 CONDUCTION IN METALS AND ELECTRON GAS

In a metal, the outer or the valence electrons are very loosely (almost zero attachment) attached to any individual atom. These atoms have at least one (or two or three) electron per atom free to move throughout the interior of the metal when an electric field is applied.

In Fig. 1.5, a schematic diagram of the charge distribution within a metal has been shown. The +ve charge (⊕) shows the nucleus and it is tightly bound with the inner electrons (i.e., with the non-valence electrons). The black dots (•) show the outer or the valence electrons in each atom. In metals, these valence electrons move about freely and the swarm of these electrons is called **electron gas.**

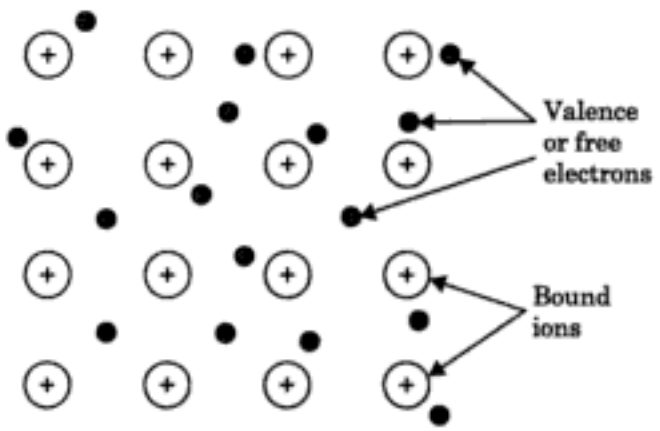


Fig. 1.5 Typical arrangement of the atoms in one plane in a conductor such as a metal, drawn for the monovalent atoms. Here, each atom contributes one electron (shown by a dot) to electron gas.

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As per the gas theory, the electrons in a metal are in continuous motion and the direction of their flight changes at each collision with the heavy (almost stationary) ions. The average distance between collision is called the **mean free path.** The net number of electrons crossing a unit area in the metal, during a given time is on the average, zero. Consequently, the average current is zero even if we short circuit two ends of a metallic conductor. In short circuiting the two ends of the conductor, we have zero electric field $\mathcal{E}$.

When we apply a constant electric field $\mathcal{E}$ to the metals, (see Fig. 1.6) the electrons, being almost free, would be accelerated and their velocity would increase indefinitely with time, if no collisions with the ions were there. At each *inelastic collision* of an electron with the ions, however, the electron loses energy and changes direction. After collision, the probability that the electron travels in a particular direction is equal to the probability that it travels in the opposite direction. We, therefore, assume that *the velocity of an electron increases linearly with time between collisions* and is, on an average, *reduced to zero at each collision.* A steady-state is reached when an average value of the drift velocity v_d is attained, its direction being opposite to that of $\mathcal{E}$ (the electric field), as shown in Fig. 1.6

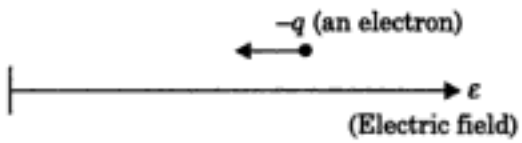


Fig. 1.6 An electron (charge, $-q$) moves left hand side, i.e., opposite to the direction of $\mathcal{E}$.

Between collisions, the electron picks up speed, given by at (acceleration × time). Here, a is acceleration which equals $\mathcal{E}q/m$ and t is the time reckoned from the last collision.

The drift velocity is proportional to $\mathcal{E}$ and is given by

$$v_d = \mu\mathcal{E} \tag{1.12}$$

where v_d is the drift velocity (m/s), *μ is the mobility* ($m^2/V - s$) *and $\mathcal{E}$ is the electric field (V/m).*

The mobility signifies the ease with which a body/particle can move under certain prescribed conditions. A high value of mobility μ implies that the body/particle will move faster than the body/particle having lower value of μ. Thus, a rubber ball is more mobile than a rough stone on the ground, when both are pushed with equal forces.

Thus, the electric field $\mathcal{E}$ has caused a steady-state drift velocity v_d and this velocity has been super-imposed on the random thermal motion of the electrons. Hence, we have a direct flow of electrons (due to non-zero v_d) which constitutes current.

1.3.1 Current Density (J)

Consider a conductor with length L and cross-sectional area A having N electrons uniformly distributed as shown in Fig. 1.7. Let electric field $\mathcal{E}$ be applied across the length L, which causes the electrons to travel distance L in time T.

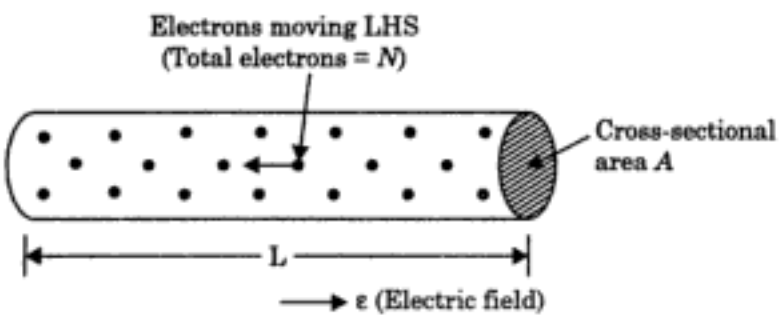


Fig. 1.7 Conductor for calculating the current density J.

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$$\text{Drift velocity } v_d = \frac{L}{t}$$

$$\text{Number of electrons crossing any area/sec} = \frac{N}{T} \text{ coulombs}$$

As each electron has charge q

$$\therefore \quad \text{Current } I = q\frac{N}{T} \qquad (\because \quad I = \text{Charge per sec}) \tag{1.13}$$

$$= q \cdot \frac{N}{L/v_d} \qquad [\because \quad T = L/v_d]$$

Hence, $$I = \frac{qNv_d}{L} \tag{1.14}$$

Thus, **Current density** $$J = \frac{\text{Current}}{\text{Area}} = \frac{I}{A} \text{ A/m}^2 \tag{1.15}$$

i.e., $$J = \frac{qNv_d}{LA}$$

As electron concentration $n = \dfrac{\text{No. of electrons}}{\text{Volume}}$

$$\therefore \quad n = \frac{N}{LA} \text{ number/m}^3 \tag{1.16}$$

By using Eqs.(1.15) and (1.16), we obtain

$$J = qnv_d = \rho_v v_d \tag{1.17}$$

or $$J = qn\mu\varepsilon \tag{1.18}$$

where ρ_v = Volume charge density = qn coulombs/m^3 (1.19)

The aforementioned derivation is independent of the form of conduction medium. Thus, Fig. 1.7 can represent a portion of a gaseous-discharge tube or a volume-element of a semiconductor. Moreover, neither ρ_v nor v_d need to be constant; these can have values which vary with time and situation.

1.3.2 Conductivity (σ) and Resistivity (ρ)

As we know, $$J = qnv_d$$
$$= qn\mu\varepsilon$$

We may write Eq. (1.18) as:

$$J = \sigma\varepsilon \tag{1.20}$$

where σ is called the **conductivity**. Hence we have

$$\textbf{Conductivity} \quad \sigma = qn\mu \ (\Omega\text{m})^{-1} \tag{1.21}$$

We confirm Ohm's law as follows:

$$I = JA = \sigma\,\varepsilon\,A \qquad (\because \quad J = \sigma\varepsilon)$$

*Equation (1.21) shows that the conductivity is proportional to the concentration n of the charge carriers.

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$$= \sigma A \frac{V}{L} \qquad \left(\because \varepsilon = \frac{V}{L}\right)$$

$$= \left(\frac{\sigma A}{L}\right) V$$

or $$I = \frac{V}{R} \qquad \left(\because R = \frac{L}{\sigma A}\right)$$

$\therefore$ **Resistance** $$R = \frac{1}{\sigma A} = \rho \frac{L}{A} \tag{1.22}$$

Conductivity $$\sigma = \frac{1}{\text{Resistivity}} = \frac{1}{\rho} \tag{1.23}$$

ρ is called resistivity.

EXAMPLE 1.1

A rectangular cross-section conductor has length/cross-sectional area ratio of 700×10^6 m^{-1}. A current of 5 mA produces a voltage drop of 100 mV across the length. Determine the electron concentration given that the electron mobility is 500 cm^2/Vs.

Solution: The given data is (see Fig. 1.8):

Voltage V = 100 mV = 0.1 V

Current I = 5 mA = 5×10^{-3} A

$$\frac{\text{Length}}{\text{cross-section}} = \frac{L}{A} = 700 \times 10^6 \text{ m}^{-1}$$

Mobility μ = 500 cm^2/*Vs* = 500×10^{-4} m^2/*Vs*

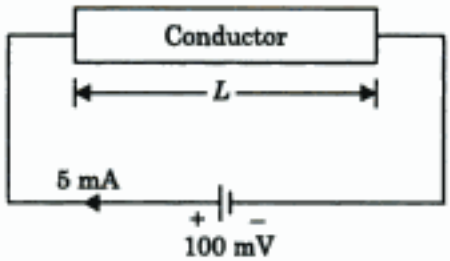


Fig. 1.8 The details of Example 1.1.

We know, $$\sigma = \frac{1}{\rho} = \frac{L}{AR} \qquad \left(\because R = \frac{\rho L}{A}, \therefore \frac{1}{\rho} = \frac{L}{AR}\right)$$

$$= \frac{L}{A} \cdot \frac{I}{V} \qquad \left(\because R = \frac{V}{I}\right)$$

$$= (700 \times 10^6) \frac{(5 \times 10^{-3})}{(0.1)}$$

$\therefore$ $\sigma = 3.5 \times 10^6 \ (\Omega\text{m})^{-1}$

Also, $$n = \frac{\sigma}{q\mu} \qquad [\because \ \sigma = qn\mu]$$

$$= \frac{3.5 \times 10^6}{(1.6 \times 10^{-19})(500 \times 10^{-4})} = 4.375 \times 10^{27} \text{ m}^{-3}$$

$= 4.375 \times 10^{21}$ cm^{-3} **Ans.**

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The free-electron concentration found in Example 1.1 is $n = 4.375 \times 10^{27}/m^3$ and is a typical value for the conductors. In insulators, however, only a few carriers, in the order of $n = 10^7/m^3$ are available as concentration. The material whose carriers concentration n lies between those of conductors and the insulators are called **semiconductors.** Semiconductors form an important category of materials in Electronics.

Typically, we have

Material	Concentration n
Conductors	10^{27} to 10^{28} nos/m^3
Semiconductors	10^{15} to 10^{16} nos/m^3
Insulators	10^6 to 10^7 nos/m^3

In Example 1.1, the ratio (length/cross-sectional area) is also typical and is 500 to 1000 $\times 10^6$ m^{-1}. Such values are valid for IC circuits. For example, in an LSI (large scale integration) type of IC, length L may be 2.5 mm and cross-sectional area $A = 1\ \mu m \times 3.5\ \mu m$, which gives $L/A = 7.15 \times 10^6$ m^{-1}. In nanotechnology, the size of ICs will further decrease and we expect a much lower value of cross-sectional area A, thereby the ratio L/A will increase.

1.4 THE INSTRINSIC SEMICONDUCTORS

Silicon (Si), Germanium (Ge) and Gallium Arsenide (GaAs) are the three most widely used materials for semiconductors. Silicon devices, however, are used in most of the applications. In this section, we bring out the conduction methodology in the semiconductors.

A pure Silicon atom has 14 electrons (arranged 2 + 8 + 4 in inner to outer orbits). Thus, Silicon has a valency of 4, i.e., it is tetravalent. Hence, an ionic core of Si atom would have a charge of +4 in units of electronic charge.

This implies that a Silicon ion obtained by removing four electrons from its outermost orbit will be a positively charged ion with $4 \times 1.6 \times 10^{-19}$ C charge. Due to valence binding, each Si atom is bound with its four neighbouring atoms by sharing each other's valence bond. The valence electrons are tightly bound and are hardly available for conduction.

1.4.1 The Concept of Hole

At a temperature of zero kelvin, the ideal structure shown in Fig. 1.9 behaves as an insulator because no free carriers of electricity are available (all the electrons being covalent bonded). At room temperature some covalent bonds may break, for example, in Fig. 1.9 an electron shown at location 1′ has come out from the covalent bonding (location 1), having been set free by thermal energy. Since an electron has left the covalent bond region 1, this region assumes a hole of the same value of charge (i.e., $+q$) as that of an electron. Thus, from a neutral atom, if an electron has been displaced (by any means, heat or electric field), the remaining atom (i.e., the +ve charged ion) may be imagined as a neutral atom plus a hole, where a hole has ($+q$) charged and ($-m$) mass. Addition of an electron and a hole results zero mass and zero charge. The energy E_G required to break a covalent bond at room temperature is about **1.1 eV for Silicon.** Thus, the absence of an electron in the covalent bond is shown

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by a hole (A hollow circle shown at location 1). Holes serve as carriers of electricity, though these are sluggish in movement (less mobile) as compared to the mobility of electrons.

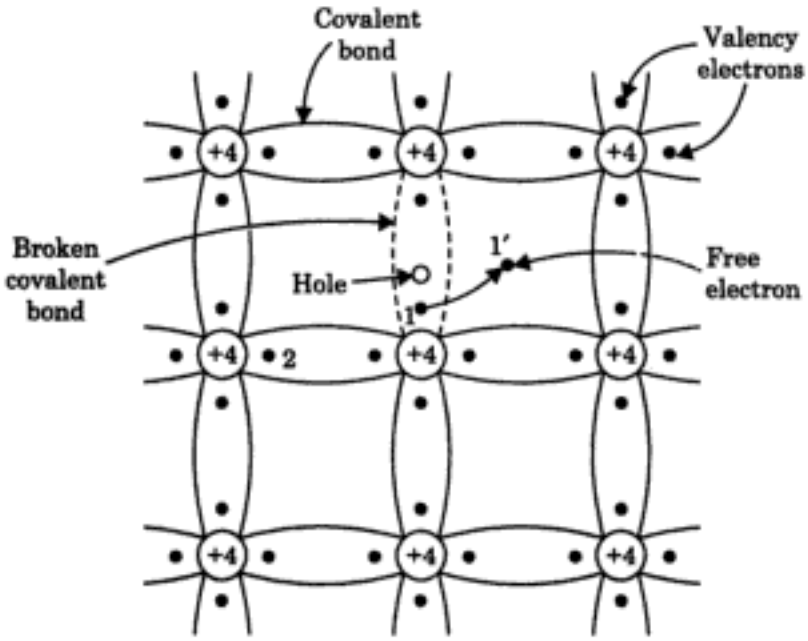


Fig. 1.9 A pictorial representation of a Silicon crystal when a covalent bond is broken. A broken covalent bond is shown in the centre by dashed lines.

When the location 1 lacks a covalent electron and instead a hole is there, it is easy for the neighbouring covalent electron (say, at location 2) to come/jump to location 1, make the location 1 as a proper covalent bond but in the bargain a hole gets generated at location 2 from where the electron has come. Effectively, a hole has moved from location 1 to location 2 and an electron from location 2 to 1. The motion of the hole in one direction actually means the transport of a –ve charge (by the electron) an equal distance in the opposite direction. A hole behaves like a +ve charge equal in magnitude to the electronic charge. By quantum mechanics, a hole can be proved to be a +ve charged particle.

The movement of a hole from one location (No. 2) to another location (No. 1) constitutes movement of charge $+q$ from location 2 to 1. This amounts to flow of current (because current = charge movement per second). Similarly, movement of a free electron from location 1 to 2 amounts to a negative current from location 1 to 2, i.e., a conventional positive current from location 2 to 1.

In other words, both holes and electrons movement contribute to the conduction process. Their mobilities are, of course, different. These p and n carriers move in the opposite direction but being of opposite signs (+ve and –ve), the current (conventional) contributed by movement of each is in the same direction. It may be noted that the time taken by the holes and the electron to move the same distance are not equal. The holes are sluggish in movement, i.e., these are less mobile as compared to the electrons, which are, more mobile. The net current caused by the movement of electrons and holes gives a current density J.

1.4.2 Conduction in Intrinsic Semiconductors

Pure Si or Ge crystals are called **intrinsic semiconductors.** In these intrinsic materials, creation of a free electron is accompanied by creation of a hole. Hence

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$$p = n = n_i \quad \text{for intrinsic semiconductor} \tag{1.24}$$

where p = Concentration of holes (Nos/m^3)
n = Concentration of electrons (Nos/m^3)
n_i = Concentration in intrinsic material (Nos/m^3)

The value of n_i is temperature dependent. As temperature increases n_i also increases. Net current density due to electron and hole movement under field intensity ε, by using Eq. (1.18) for electron n and hole p concentrations, is:

$$J = q(n\mu_n + p\mu_p)\varepsilon \tag{1.25}$$

or
$$J = \sigma\varepsilon \tag{1.26}$$

where Conductivity (in general)
$$\sigma = q(n\mu_n + p\mu_p) \tag{1.27}$$

For intrinsic semiconductor, since $p = n = n_i$, we, therefore, have

$$\sigma_i = qn_i\,(\mu_n + \mu_p) \tag{1.28}$$

where
q = Charge of an electron = 1.602×10^{-19} C
μ_n = Mobility of electrons (m^2/*Vs*)
μ_p = Mobility of holes (m^2/*Vs*)
ε = Electric field (V/m)
σ = Conductivity $(\Omega m)^{-1}$ (σ_i is for intrinsic materials)
J = Current density (A/m^2)

For silicon, atoms/cm^3 = 5.0×10^{22} and $n_i = 10^{10}$/cm^3.

Thus, only 1 atom in about 10^{12} atoms contributes a free electron-hole pair by breaking a covalent bond in Silicon crystal.

EXAMPLE 1.2

A slice of intrinsic silicon bar is 3 mm long and has a rectangular cross-section 50 μm × 10 μm. At 300 K, determine the electric field intensity in the bar and the voltage across the bar when a steady current of 2 μA is measured. Take the value of resistivity $\rho = 2.30 \times 10^5$ Ωcm at room temperature (300 K).

Solution: As $J = \sigma\varepsilon$

$$\therefore \quad \varepsilon = \frac{J}{\sigma} = \frac{I}{A}\cdot\frac{1}{\sigma} \qquad \left(\because J = \frac{I}{A}\right)$$

$$= \frac{I}{A}\cdot\rho \text{ V/m} \qquad \left(\because \frac{1}{\sigma} = \rho\right)$$

$$= \frac{2\times10^{-6}}{(50\times10^{-6})\times(10\times10^{-6})}\cdot\frac{2.3\times10^5}{100}$$

(taking A in m^2 and ρ in Ωm)

$$\therefore \quad \varepsilon = 9.2 \times 10^5 \text{ V/m}$$

Voltage across the bar $V_{bar} = \varepsilon L = 9.2 \times 10^5 \times 3 \times 10^{-3}$

$$\therefore \quad V_{bar} = 2760 \text{ V} \quad \textbf{Ans.}$$

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We note that in the intrinsic semiconductor, to pass a current of only 2 μA, we need a high voltage of 2760 V.

Example 1.2 shows that the intrinsic semiconductors are not suitable for electron devices since their conduction is too low, and we need very high voltages to obtain even micro ampere of current. This problem is solved by doping the intrinsic materials, which is discussed in Section 1.5.

1.5 EXTRINSIC SEMICONDUCTORS (DOPED SEMICONDUCTORS)

A common method to increase the number of charge carriers in the intrinsic semiconductor is to add a small, carefully controlled, impurity content into the intrinsic semiconductor. The addition of impurities, most often by a trivalent or a pentavalent atoms, converts the intrinsic semiconductor to extrinsic or doped semiconductor. Each type of impurity establishes a semiconductor which has predominance of one kind of carrier (i.e., either a hole or an electron). The usual level of impurity is in the range of 1 atom in 10^6 to 10^8 (note that in an intrinsic semiconductor roughly 1 atom in 10^{12} contributes a free electron or a free hole). The most commonly used intrinsic semiconductor is Silicon (tetravalent material).

1.5.1 *n*-type Semiconductors

To achieve *n*-type semiconductors, we dope the intrinsic semiconductor (say, Silicon) with a pentavalent impurity, and to achieve *p*-type semiconductors, we dope by a trivalent impurity. A few commonly used doping materials are

Donors (Pentavalent atoms): To obtain *n*-type extrinsic material

	Atomic number
Antimony (Sb)	51 (2 + 8 + 18 + 18 + 5)
Arsenic (As)	33 (2 + 8 + 18 + 5)
Phosphorous (P)	15 (2 + 8 + 5)

Acceptors (Trivalent atoms): To obtain *p*-type extrinsic material

	Atomic number
Boron (B)	5 (2 + 3)
Gallium (Ga)	31 (2 + 8 + 18 + 3)
Indium (In)	49 (2 + 8 + 18 + 18 + 3)

The figures in the brackets against each doping material indicate the number of electrons in various orbits starting from the innermost to the outermost orbit. Note that for pentavalent atoms, there are 5 electrons in their outermost orbits and similarly for trivalent atoms, there are 3 atoms in their outermost orbits.

As seen in Fig. 1.10 doping is done by a pentavalent atom (shown +5). Four of the valence electrons of the impurity atom occupy covalent bonds, along with the neighbouring 4 Silicon atoms. However, the fifth valence electron of the impurity atom remains unassigned or unbounded by any bond. This loose (fifth) electron is available as a carrier of current. *The energy required to detach this fifth unattached electron from the parent atom is*

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of the order of only ***0.05 eV for Silicon,*** and is considerably less than the energy required (1.1 eV) to break the covalent bond.

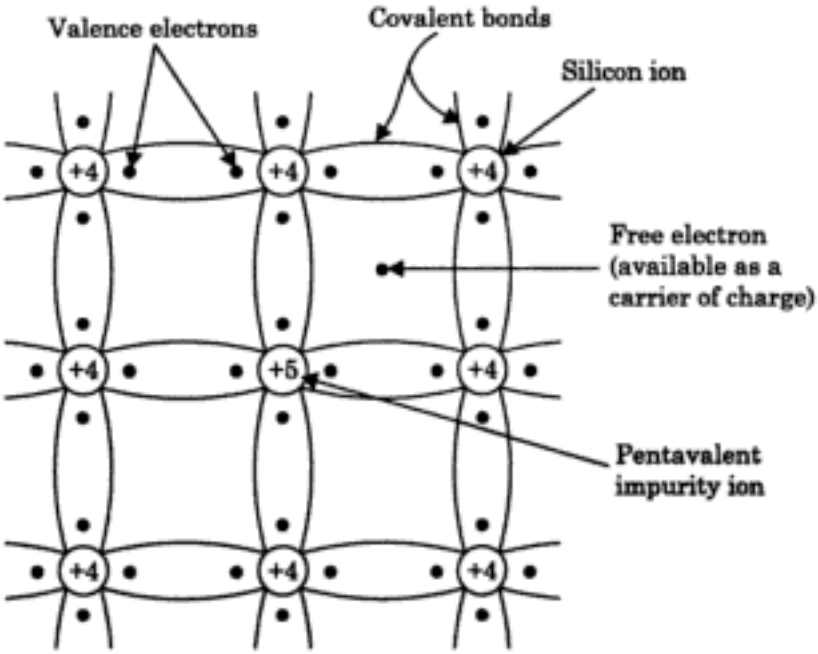


Fig. 1.10 A crystal lattice with Silicon atom (a tetravalent atom) when displaced by a pentavalent impurity atom (such as phosphorus, being a pentavalent atom).

Note that this energy (0.05 eV) is about one twentieth of the energy (1.1 eV) required to pull out an electron from the covalent bond. Whereas we needed a voltage of 1.1 V to pull out an electron from the covalent bond in the pure Silicon material, we require only 0.05 V to pull out an electron from the doped Silicon. Moreover, by "heavy/moderate" doping, we expect "heavy/moderate" currents, and that too with much lower electric field, from a doped Silicon material.

The commonly used pentavalent impurities are Antimony (Sb), Phosphorus (P), and Arsenic (As). Such impurities, which donate their excess (fifth) electron (as a carrier) are called **donor,** or **n-type impurities.**

Due to doping by an *n*-type material, the total number of carrier electrons increases and also the carrier holes available in the extrinsic material are less than those were in the undoped (intrinsic) material. This is so since a large number of relatively free electrons available in the doped, semiconductor material recombine with a few of its intrinsic holes. Thus, the dominant carrier in an *n*-type semiconductor are the electrons, though there are also a few holes available in the *n*-type semiconductor material.

1.5.2 *p*-type Semiconductors

Boron, Gallium and Indium are trivalent atoms and when added to an intrinsic semiconductor, they provide electrons to fill only three covalent bonds (see Fig. 1.11). In the fourth bond, nil electron of trivalent atom/impurity may be imagined as an electron-hole pair. The electron of this pair provides the fourth valence electron needed by the neighbouring Si atom leaving the hole free. The hole is relatively free to leave the covalent bond (shown dashed in Fig. 1.11). Thus, the trivalent impurities make positive holes available. As the holes can

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accept electrons hence trivalent impurities are called **Acceptors** and the trivalent impurities added to intrinsic semiconductors yield *p*-type semiconductors. In the *p*-type semiconductors the holes are the predominant carriers. A few of these holes combine with electrons available in the intrinsic Si (which we denoted by n_i). Thus, in an equilibrium state the net number of unbounded electrons is less than n_i and net number of holes is much more than p_i.

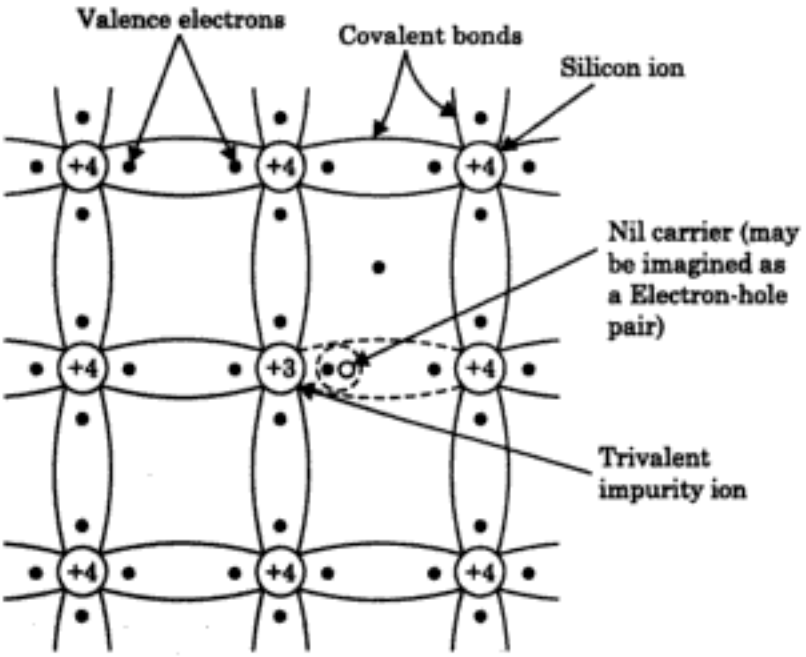


Fig. 1.11 A crystal lattice with Silicon atom (a tetravalent atom) when displaced by a trivalent atom (such as Indium).

The intrinsic semiconductor material may be made *n*-type or *p*-type extrinsic semiconductor by doping with Donor or Acceptor materials. At times we require doped (extrinsic) materials capable of behaving almost as a good conductor, this is accomplished by doping heavily. Such materials are denoted by n^+- or p^+-type extrinsic semiconductors. n^+ extrinsic material mean that the original (intrinsic) material has been doped heavily by a donor impurity, and that there are much more free electrons available in n^+ material than those in *n* material. This makes n^+ materials good conductors. Similar is the case for p^+ extrinsic materials, where heavy doping is done by acceptor impurities.

Also, a *p*-material (Si doped by trivalent dopant), can be made an undoped material by doping the given *p*-material by an *n*-dopant (i.e., by a pentavalent dopant). Similarly, a *n*-material (Si doped by a pentavalent dopant) can be changed to an undoped material by doping it by a trivalent dopant. Further doping can turn an *n*-material to a *p*-material. In short, it is feasible to change the nature of one type of doped (say, *p*) extrinsic Si to the other type of doped (say, *n*) extrinsic material. This facility enables us to fabricate a complete transistor device on a common Silicon substrate.

1.5.3 The Mass-Action Law

The addition of *n*-type impurities in the intrinsic semiconductor increases the free electrons concentration and decreases the free holes concentration from that was present in the intrinsic semiconductor. Similarly, the addition of a *p*-type impurity increases the holes and decreases the electron concentrations. **Under thermal equilibrium, the product of the**

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free negative and positive concentrations is a constant. This is called the Mass-action law, i.e.,

$$np = n_i^2 \tag{1.29}$$

where n = Concentration of –ve (electron) after doping

p = Concentration of +ve (holes) after doping

$n_i = p_i$ = Concentration of electron n_j or of holes p_i in the intrinsic semiconductor

In n-type semiconductor, the electrons are the majority carriers and holes the minority carriers. Reverse is the case of p-type semiconductor, where the holes are the majority carriers and electrons are the minority carriers. The word 'Carrier' implies that these (n or p) are the current carrying agents.

1.5.4 Carrier Concentrations

A small amount of energy is needed to ionize the atoms. When we remove an electron (or a hole) from an overall neutral atom, the remaining atom is positive (or a negative) ion. The energy needed to remove an electron (or a hole) from the neutral atom depends on the temperature, decreasing with increasing temperatures. The electronic devices normally operate at temperature greater than 200 K. At these temperatures, there is sufficient thermal energy to ionize almost all the extrinsic materials. Using the Mass-action law, we can determine the charge densities in the semiconductors.

If N_D is the concentration of donor atoms, there will be N_D immobile positive charges per unit volume contributed by the donor ions as the donor atoms are ionized to positive charge, since they give away their electron.

The positive charge density will, therefore, be $N_D + p$. Similarly, as the acceptor atoms are ionized (to negative charge) there will be N_A immobile negative charges per unit volume. The negative charge density will, therefore, be $N_A + n$.

Since the crystal is overall electric neutral, hence

$$N_D + p = N_A + n \tag{1.30}$$

where N_D = Concentration of donor atoms

N_A = Concentration of acceptor atoms

p = Concentration of holes

n = Concentration of electrons

In n-type materials, $N_A = 0$ and $p << n$, therefore, Eq. (1.30) gives

$$n \approx N_D \quad \text{in } n\text{-type semiconductor} \tag{1.31a}$$

Similarly, $$p \approx N_A \quad \text{in } p\text{-type semiconductor} \tag{1.31b}$$

Using $np = n_i^2$ (Mass-action law)

We finally have the following relations:

$$n = N_D;\ p = \frac{n_i^2}{N_D} \quad \text{for } n\text{-type semiconductors} \tag{1.32a}$$

$$p = N_A;\ n = \frac{n_i^2}{N_A} \quad \text{for } p\text{-type semiconductors} \tag{1.32b}$$

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EXAMPLE 1.3

An extrinsic n-type Silicon sample is 3 mm long and has a cross-section of 5×10^{-9} m^2. The donor concentration at 300 K is 5×10^{14}/cm^3 and corresponds to 1 impurity per 10^8 Silicon atoms. A steady current of 2 μA exists in the bar. Determine the electron and hole concentration, the conductivity, and the voltage across the bar (the n-type sample here has the same dimensions and current as does the intrinsic Silicon in Example 1.2).

(Use $n_i = 1.45 \times 10^{10}$/cm^3; $\mu_n = 1500$ cm^2/Vs for Silicon)

Solution Given $n = N_D = 5 \times 10^{14}$/cm^3 = electron concentration

$n_i = 1.45 \times 10^{10}$/cm^3 at 300 K

As $$p = \frac{n_i^2}{N_D} \qquad \text{[From Eq. (1.32}a\text{)]}$$

$$= \frac{(1.45 \times 10^{10})^2}{5 \times 10^{14}} = 4.2 \times 10^5/\text{cm}^3 \quad \textbf{Ans.}$$

Then Conductivity $\sigma = q(n\mu_n + p\mu_p)$ [From Eq. (1.27)]

$= qn\mu_n \quad (\because p << n$ for n-type semiconductor)

$= (1.60 \times 10^{-19})\ (5 \times 10^{14})\ (1.5 \times 10^3)$

$\therefore \quad \sigma = 0.12\ (\Omega\text{cm})^{-1}$ **Ans.**

and Resistivity $\rho = \frac{1}{\sigma} = \frac{1}{0.12}\ (\Omega\text{cm}) \qquad$ [From Eq. (1.23), $\rho = 1/\sigma$]

$= 8.33\ (\Omega\text{cm})$

Voltage across the bar

$$V_{bar} = \mathcal{E}L = \frac{J}{\sigma} L \qquad [\because J = \sigma\mathcal{E}, \text{ due to Eq. (1.25) and assuming } p << n]$$

$$= \frac{I}{A} \cdot \frac{L}{\sigma}$$

$$= \frac{(2 \times 10^{-6}) \times (3 \times 10^{-1})}{(5 \times 10^{-9} \times 10^4) \times 0.12} \qquad \left(\because A = 5 \times 10^{-9}\ \text{m}^2 = 5 \times 10^{-9} \times 10^4\ \text{cm}^2\right)$$

$\therefore \quad V_{bar} = 0.1$ V **Ans.**

Note that in intrinsic semiconductor (Example 1.2), we would require a voltage of 2760 V to produce a current of 2 μA, whereas in extrinsic semiconductor (here) we require only 0.1 V. This amounts to reduction of voltage by a factor 2760/0.1 = 27600. It also amounts to decrease in resistivity from 2.30×10^5 to 8.33 (Ωcm), i.e., the same factor. Such a dramatic increase in the number of free electrons (from 1.45×10^{10} in intrinsic to 5×10^{14} in extrinsic) occurs when **1 impurity atom is added in** 100×10^6 intrinsic atoms (i.e., 1 in 10^8 ratio). In fact, by controlling the impurity concentration while fabricating an extrinsic semiconductors, we can obtain any desired property of the doped materials.

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1.5.5 Generation and Recombination of Charges n^+, p^+

If we add an equal amount of donor and acceptor impurities to an intrinsic material, the net is again an intrinsic material as the equal and opposite type of impurities cancel each other's effect. Also, if we add *donor impurities to an n-type semiconductor, the n-type* **semiconductor can be termed to be heavily doped (n^+) material.** If we add acceptor impurities to n-type semiconductor, the n-type semiconductor may become lightly doped and even turn to p-type material. Under these conditions we use $N_D - N_A$ (or $N_A - N_D$) in the various formulas $n = N_D$ (or $p = N_A$) given by Eq. (1.31*a*) or Eq. (1.31*b*), respectively.

In fact, the above facts helps us in IC fabrication and to make *npn* or *pnp* transistors at will. We shall discuss the use of *npn* and *pnp* transistors in the subsequent chapters.

In intrinsic semiconductors, the number of holes is equal to the number of free electrons. Thermal agitation, however, continues to generate new hole-electron pairs per unit volume per second, where other hole-pairs disappear as a result of recombinations. On the average, a hole will exist for τ_p seconds before recombination. Similarly, an electron will exist for τ_n seconds before recombination. τ_p and τ_n are called the **mean life times** of the hole and electron, respectively. These parameters are important in semiconductor devices as they indicate the time required for electron and the hole concentrations, which have been caused to change, to return to their equilibrium concentrations. The mean life times assume special significance where we operate semiconductors at microwave frequencies.

1.6 EFFECT OF TEMPERATURE ON THE PROPERTIES OF SILICON: VARIATION OF MOBILITY WITH ELECTRIC FIELD ε

The conductivity of a semiconductor derived earlier (Eq. 1.27) is:

$$\sigma = q(n\mu_n + p\mu_p) \ (\Omega\text{m})^{-1} \tag{1.33}$$

Thus, σ is a function of hole and electron concentrations (p, n) and their mobilities (μ_p, μ_n). The semiconductor devices are subject to wide range of operating temperatures T, which in turn varies p, n, μ_p and μ_n and hence the conductivity σ of the semiconductor.

1.6.1 Intrinsic Concentration

In the intrinsic semiconductor, the hole-electron pairs increase with increase of temperature. Theoretically, we have the relation:

$$n_i^2 = A_o T^3 e^{-E_{GO}/kT} \tag{1.34}$$

where n_i = Intrinsic concentration in number/m^3.

E_{GO} = Energy gap, i.e., the energy needed to break a covalent bond at 0 K in eV

k = Boltzmann constant = 8.620×10^{-5} eV/K

A_o = A constant, independent of T

T = Temperature in kelvin

For an extrinsic semiconductor, variation of T changes the charge densities as follows. For, say, p-type semiconductor where $p >> n$ and $p \approx N_A$, all the acceptor atoms are almost

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ionized. As T increases, n_i increases. But $pn = n_i^2$ (the Mass-action law), and $p \approx N_A$ = constant. Thus, with increase of T, n must increase, i.e., the minority carriers increase. This is true for n-type semiconductor also. *Hence, increase of temperature T increases the minority carrier concentration.*

1.6.2 Mobility (μ)

For 100 K < T < 400 K, the mobility is approximated by

$$\mu = (\text{Constant } B_o) \cdot T^{-m} \tag{1.35a}$$

where m = 2.5 for electrons and 2.7 for holes, i.e., the holes are less mobile compared to the electrons.

Also, we note that the value of μ (the mobility) decreases with increase of temperature T. At higher temperatures more carriers are present. These carriers have more energies and, therefore, cause more collisions. As stated earlier, after each collision, the colliding carriers lose energy and speed, and almost come to standstill. Thus, more collisions makes the charge carrier less mobile. This results in decrease of mobility μ.

Mobility also is a function of electric field intensity, and is given (say, for electrons) as:

$$\mu_n = \begin{cases} \text{constant}, & \varepsilon < 10^3 \text{ V/cm} \\ A_1 \varepsilon^{-1/2}, & 10^3 \text{ V/cm} < \varepsilon < 10^4 \text{ V/cm} \\ A_2 \varepsilon^{-1}, & \varepsilon > 10^4 \text{ V/cm} \end{cases} \tag{1.35b}$$

where A_1 and A_2 are constants. The formulae given in Eq. (1.35) are almost approximate and not exact. It only shows the dependence of mobility (μ_n here) on the electric field intensity ε and temperature T.

Note that from Eq. (1.12), $v_d = \mu\varepsilon$ and for $\varepsilon > 10^4$ V/cm, $\mu_n\varepsilon = A_2$ (constant). Hence $v_d = A_2$, a constant for ε exceeding 10^4 V/cm.

The drift velocity approaches 10^7 cm/s (saturation velocity) when the electric field ε exceeds 10^4/cm, i.e., for $\varepsilon > 10^4$ V/cm.

1.6.3 Conductivity (σ)

(i) Conductivity of an intrinsic semiconductor increases with increasing temperature (as n_i increases) [see Fig. (1.12a)].

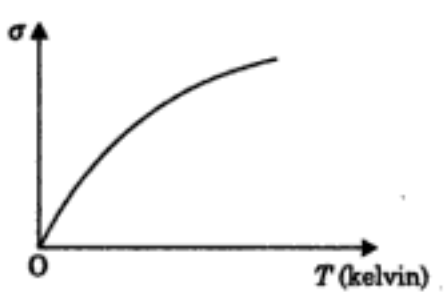


Fig. 1.12(a) Variation of conductivity σ with temp. T, for intrinsic semiconductor.

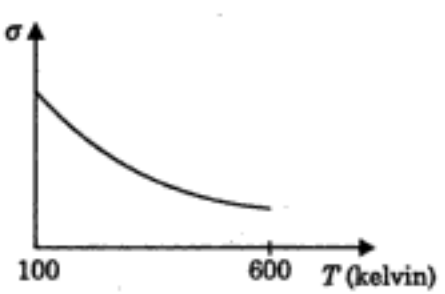


Fig. 1.12(b) Decrease in conductivity as temperature varies between 100 K and 600 K for extrinsic semiconductors.

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(ii) In extrinsic semiconductors for 100 K < T < 600 K, majority carriers are nearly constant but diminished mobility causes the decrease in conductivity with temperature rise. [see Fig. (1.12b)] Thus, when we use semiconductor devices (such as BJT transistors or MOSFETs), we must keep the operating temperature under control (say, by airconductioning), to achieve the designed performance of the systems.

1.7 DIFFUSION CURRENTS

In addition to the conduction current of charges in a semiconductor, the charges are also transported by a mechanism called **diffusion.** Note that *the diffusion is ordinarily not encountered in metals.* This is due to high conductivity in metals (good conductors) there is almost nil current carrier (the electrons) concentration variation along the path of conduction current. However, in the case of semiconductors, the charge carriers (n and p) do not get transported immediately. They have much lower mobilities (compared to the mobility of electrons in metals), and hence these tend to be distributed unequally along conduction path.

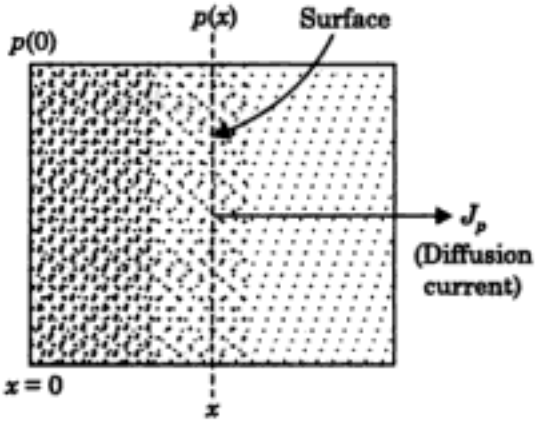


Fig. 1.13 A pictorial representation of a non-uniform hole density and the resulting current density J_p. Note that $p(x)$ has –ve gradient here and the current is towards increasing x-direction.

Let us consider non-uniform concentrations of particles in a semiconductor, i.e., that of holes as shown in Fig. 1.13; here the concentration of holes p varies with distance x, and there exits a concentration gradient dp/dx in the density of charges carriers. The holes are in a random motion due to the thermal energy; the holes continue to move back and forth across a given surface (like the one shown dashed). Since the concentration is higher on LHS of dashed surface, we may expect that in a given time interval, more holes will cross the surface from the side of greater concentration to the side of the smaller concentration. This net transport of holes across the surface constitutes a current in the +ve direction of x. It may be noted that this transport charge is not the result of mutual repulsion among the charges of the same sign but simply the result of a statistical phenomenon. This diffusion is analogous to that occuring in natural gas if a concentration gradient exists. In this case there is a gradient (i.e., variation) of hole density p as x varies. The current density due to diffusion is given by

$$J_p = -qD_p \frac{dp}{dx} \tag{1.36}$$

Similarly, for the case of gradient in electron density n, we have diffusion current:

$$J_n = +qD_n \frac{dn}{dx} \tag{1.37}$$

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The –ve sign in Eq. (1.36) is due to the fact that gradient dp/dx is –ve as x increases. But the current density J_p is towards increasing x-direction (i.e., current flows towards the increasing direction of x in Fig. 1.13). By taking –ve sign on RHS of J_p in Eq. (1.36), the value of current density J_p turns out to be +ve as is apparent in Fig. 1.13. However, in Eq. (1.37), we have taken +ve sign for RHS of J_n. Electron flowing towards +ve x-axis amount to –ve current flowing towards +ve x-axis. As dn/dx will be –ve in case of high concentration electrons on LHS of Fig. 1.13, the expression $+qD_n\, dn/dx$ as given in Eq. (1.37) will be –ve, as desired. We shall define the constant D_p and D_n in the next sub-section 1.7.1.

1.7.1 The Einstein Relationship

Both, the diffusion and mobility are statistical thermodynamic phenomena; hence D and μ are not independent. They are related by Einstein equation:

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = V_T \tag{1.38}$$

where $$V_T = \frac{\bar{k}T}{q} = \frac{T}{11{,}600} \text{ volt}$$

V_T = Voltage equivalent to temperature

D_p, D_n = Diffusion constants for hole and electrons, respectively in m^2/s

μ_p, μ_n = Mobilities for holes and electrons, respectively in m^2/Vs

$\bar{k}$ = Boltzmann constant = $1.60 \times 10^{-19} \times k = 1.381 \times 10^{-23}$ J/K

k = Boltzmann constant = 8.620×10^{-5} eV/K

At room temperature $$V_T = \frac{300}{11{,}600} \approx 25 \text{ mV} \tag{1.39a}$$

and $$\mu = 38.6D \text{ or } \mu \approx 40\ D \tag{1.39b}$$

1.7.2 Total Current

It is also possible to have both the potential gradient as well as concentration gradient to exist simultaneously within a semiconductor. In such cases, using Eqs. (1.18), (1.36) and (1.37), we get

Total current = Drift current (due to field $\mathcal{E}$) + Diffusion current (due to concentration gradient)

i.e., $$J_p = q\mu_p p\mathcal{E} - qD_p \frac{dp}{dx} \quad \text{(net hole current)} \tag{1.40}$$

$$J_n = q\mu_n n\mathcal{E} + qD_n \frac{dn}{dx} \quad \text{(net electron current)} \tag{1.41}$$

where μ_p, μ_n = Mobilities of holes and electrons in m^2/Vs

p, n = Concentrations of holes and electrons in Nos./m^3

$\mathcal{E}$ = Electric field intensity in V/m

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q = Charge of a hole/electron = 1.60×10^{-19} coulomb

$\frac{dp}{dx}, \frac{dn}{dx}$ = Hole and electron diffusion constants in m^2/s

The values of important parameters such as intrinsic concentration, mobility and diffusion constant for Silicon and Germanium are given in Table 1.2.

Table 1.2 Properties of Intrinsic Silicon and Germanium

Property	*Value*	
	Silicon (Si)	*Germanium (Ge)*
Atomic number	14	32
Atomic weight	28.1	72.6
Density (g/cm^3)	2.33	5.32
Relative permittivity (dielectric constant)	11.9 (≈ 12)	16
Atoms/cm^3	5.0×10^{22}	4.4×10^{22}
Energy gap E_{GO} at 0 K (eV)	1.21	0.785
Energy gap E_G at 300 K (eV)	1.12	0.72
Resistivity ρ at 300 K (Ωcm)	2.3×10^5	4.5×10^5
Electron mobility μ_n at 300 K (cm^2/Vs)	1500	3800
Hole mobility μ_p at 300 K (cm^2/Vs)	475 (≈ 500)	1800
Intrinsic concentration n_i at 300 K (Nos/cm^3)	1.45×10^{10} ($\approx 1.5 \times 10^{10}$)	2.5×10^{13}
Electron diffusion constant D_n at 300 K (cm^2/s)	34	99
Hole diffusion constant D_p at 300 K (cm^2/s)	13	47

1.8 GRADED SEMICONDUCTORS AND CALCULATIONS OF BARRIER POTENTIAL

Let us consider a graded semiconductor, i.e., the concentration of, say, p to be non-uniform, as shown in Fig. 1.14(a).

Hence in Fig. 1.14(a), the doping is graded, i.e., $p(x)$ is not constant. By Mass-action law, we have, therefore,

$$np = n_i^2$$

where n, p = Free electron and hole concentration after doping (Nos/m^3)

n_i = Concentration of hole = Concentration of electrons in an intrinsic semiconductor (Nos/m^3)

If $p(x)$ varies then $n(x)$ must also vary to make $p(x) \cdot n(x) = n_i^2$. Assume an open circuit semiconductor, and hence *net electronic current must be zero.* There can be no steady current, i.e., charge motion, under these conditions (i.e., in the open circuit.)

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As $p(x)$ is not constant, i.e., the hole gradient dp/dx exists (and is not zero). In Fig. 1.14(a) let $p(x)$ be maximum at $x = 0$ and minimum at $x = L$. The holes would try to diffuse from

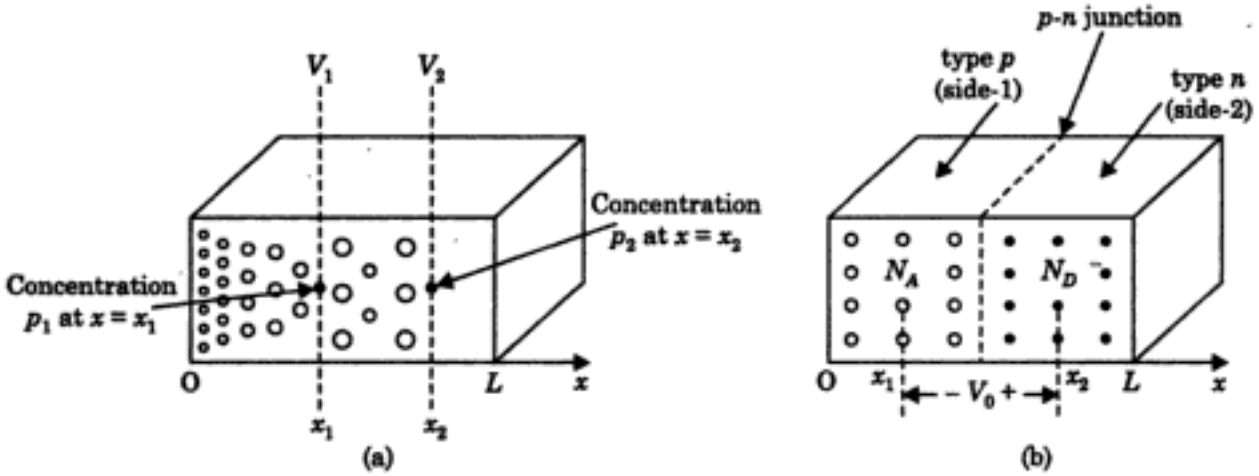


Fig. 1.14 (a) A graded semiconductor, i.e., $p(x)$ is not constant (b) A p-n junction in which p and n are uniformly doped with impurity concentration N_A and N_D, respectively.

LHS to RHS due to hole gradient. To have an overall zero current an equal but opposite drift current of holes coming from RHS to LHS must exist. But a drift current requires an electric field. Thus, as a result of non-uniform doping $p(x)$ an electric field $\varepsilon(x)$ is generated within the semiconductor, which will cause drift current. We know that hole current and electron current where drift and diffusion both are present are:

Net hole current $$J_p = q\mu_p p\varepsilon - qD_p \frac{dp}{dx}$$ [From Eq. (1.40)] (1.42)

Net electron current $$J_n = q\mu_n n\varepsilon + qD_n \frac{dn}{dx}$$ [From Eq. (1.41)] (1.43)

In the open circuited semiconductor Fig. 1.14a, net current must be zero. Hence putting $J_p = 0$ in Eq. (1.42), we get

$$0 = q\mu_p p\varepsilon - qD_p \frac{dp}{dx} \tag{1.44}$$

or $$\varepsilon = \frac{D_p}{\mu_p \cdot p} \frac{dp}{dx} \tag{1.45}$$

But $D_p = \mu_p V_T$ [From Eq. (1.38), i.e., Einstein equation]

Putting $D_p = \mu_p V_T$ in Eq. (1.45), we have

$$\varepsilon(x) = \frac{V_T}{p} \frac{dp}{dx}$$

But $$dV = -\varepsilon(x)\,dx \qquad \left(\because \varepsilon(x) = -\frac{dV}{dx}\right)$$

$\therefore$ $$dV = \left(-\frac{V_T}{p}\frac{dp}{dx}\right).dx$$

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or $$dV = -V_T \frac{dp}{p} \tag{1.46}$$

Integrating Eq. (1.46) on both sides, we get

$$[V]_{V1}^{V_2} = [-V_T \ln p]_{p1}^{p2}$$

or $$V_2 - V_1 = V_{21} = -V_T (\ln p_2 - \ln p_1) = V_T \ln \frac{p_1}{p_2}$$

Hence the potential difference $(V_2 - V_1)$ between two points x_2 and x_1 depends only on the concentrations p_2 and p_1 at these points independent of their separation $x_2 - x_1$. As

$$V_2 - V_1 = V_{21} = V_T \ln \frac{p_1}{p_2} \tag{1.47}$$

Note that if p_1 is greater than p_2 then $\ln \frac{p_1}{p_2}$ is +ve and $V_2 > V_1$. Hence diffusion phenomenon causes holes to flow from LHS to RHS in Fig. 1.14(a); but V_2 (at point x_2) being higher than V_1 (at point x_1), it produces an electric field such that the holes on LHS of x_2 are repelled back towards LHS (towards location x_1). The net effect of "diffusion tendency" is fully cancelled by "field effect" of voltage difference $(V_2 - V_1)$ so produced. Hence, there is no net current flow, as is expected (being an open circuited semiconductor).

The value of potential difference $(V_2 - V_1)$, derived in Eq. (1.42) holds good for a generic case of graded semiconductor (i.e., where $p_1 \neq p_2$). By using the result we can determine the "barrier potential" for specific cases. One commonly used device in semiconductor is step graded junction, called ***p-n* junction.**

1.8.1 Step-graded Junction (Open Circuited Case)

In most of the diodes and junction transistors the doping concentration is constant on p side and also constant on n side. Such a structure yields step-graded p-n junction, as shown in Fig. 1.14(b).

Thus, in a step-graded p-n junction, the concentration N_A and N_D are constant throughout the p and n sides, respectively. Hence, the doping density changes abruptly from p to n type. The junction is obviously located at the plane where the concentration is zero. In the equilibrium state, open circuited case, a contact difference of potential V_o must exist to have overall currents passing through the *p-n junction zero.* Let

$p_1 = p_{p_o}$ = Thermal-equilibrium hole concentration on p-side (side 1)

$p_2 = p_{n_o}$ = Thermal-equilibrium hole concentration on n-side (side 2)

$n_1 = n_{p_o}$ = Thermal-equilibrium electron concentration on p-side (side 1)

$n_2 = n_{n_o}$ = Thermal-equilibrium electron concentration on n-side (side 2)

But $p_{p_o} = N_A$ and $n_{n_o} = N_D$ [Due to Eq. (1.32)]

Also $p_{n_o} \times n_{n_o} = n_i^2$ (Mass-action law as applied on n-type side)

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$\therefore$ $$p_{n_o} = \frac{n_i^2}{N_D} = p_2 \qquad \text{(putting } n_{n_o} = N_D\text{)}$$

As $$V_2 - V_1 = V_{21} = V_T \ln \frac{p_1}{p_2} \qquad \text{[From Eq. (1.47)]}$$

Put $p_1 = p_{p_o} = N_A$ and $p_2 = p_{n_o} = n_i^2/N_D$, therefore, above relation yields

$$V_2 - V_1 = V_o = V_T \ln \frac{N_A}{(n_i^2/N_D)}$$

Finally, we get

$$V_o = V_T \ln \frac{N_A N_D}{n_i^2} \qquad \text{for step-graded } p\text{-}n \text{ junction} \qquad (1.48)$$

In deriving V_o, we have used the relation

$$V_{21} = V_T \ln \left(\frac{p_1}{p_2}\right) \qquad \text{[from Eq. (1.47)]}$$

However, if we use the relation

$$V_{21} = V_T \ln \frac{n_2}{n_1}$$

and put $n_2 = N_D$, $n_1 = n_i^2/N_A$ (Mass action law applied on p-side)

We again arrive at the result,

$$V_o = V_{21} = V_T \ln \frac{N_A N_D}{n_i^2}$$

We conclude that an open circuited piece of doped semiconductor cannot pass current. Internal barrier voltages get generated which completely cancel the tendency of charge carrier flow due to p or n concentration gradients. The barrier voltage V_o derived in the case of p-n junction diode plays an important role in explaining the operation of p-n devices, as will be discussed in subsequent chapters.

EXAMPLE 1.4

The junction on a step-graded p-n junction diode is doped with N_A corresponding to 1 acceptor atom per 10^6 Si atoms. Calculate the contact difference of potential V_o at room temperature. Assume $N_A = N_D$, $n_i = 1.45 \times 10^{10}/\text{cm}^3$ and Silicon has 5×10^{28} atoms/m.

Solution: $N_A = 1 : 10^6$ atoms of Silicon

But 1 m^3 of Silicon has 5.0×10^{28} atoms

$\therefore$ $$N_A = 5.0 \times \frac{10^{28}}{10^6} = 5.0 \times 10^{22} \text{ atoms/m}^3$$

and $N_D = N_A = 5.0 \times 10^{22}$ Nos/m^3 ($\because$ uniformly doped)

Now, $n_i = 1.45 \times 10^{10} \times 10^6$ Nos/m^3 $= 1.45 \times 10^{16}$ Nos/m^3

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As $V_T = \dfrac{T}{11{,}600} = 25$ mV at room temperature $= 25 \times 10^{-3}$ V

$\therefore \quad V_o = V_T \ln \dfrac{N_A N_D}{n_i^2}$

$$= (25 \times 10^{-3}) \ln \frac{(5 \times 10^{22})^2}{(1.45 \times 10^{16})^2}$$

$$= (25 \times 10^{-3}) \ln (11.8906 \times 10^{12})$$

$$= (25 \times 10^{-3}) \times (\log_{10} 11.8906 \times 10^{12}) (\log_e 10)$$

$$= (25 \times 10^{-3} (1.0752 + 12) (2.3)$$

$$= 751.824 \times 10^{-3}$$

$\therefore \quad V_o = 751.8$ mV **Ans.**

EXAMPLE 1.5

Verify the equation giving contact difference potential

$$V_o = V_{21} = V_T \ln \frac{p_{p_o}}{p_{n_o}} = V_T \ln \frac{N_A N_D}{n_i^2} \text{ volts}$$

where $p_1 = p_{p_o}$ = Thermal-equilibrium hole concentration in p side

$p_2 = p_{n_o}$ = Thermal-equilibrium hole concentration on n side

For the step-graded junction shown, by taking the electron current density $J_n = 0$ in Eq. (1.43)

Solution: The net electron current is given by

$$J_n = q \mu_n n \varepsilon + q D_n \frac{dn}{dx}$$

Putting $J_n = 0$, we obtain

$$\varepsilon = -\frac{D_n}{\mu_n} \frac{1}{n} \frac{dn}{dx}$$

$$= -\frac{V_T}{n} \frac{dn}{dx} \qquad \left(\because \frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T \right)$$

$\therefore \quad -\dfrac{dV}{dx} = -\dfrac{V_T}{n} \dfrac{dn}{dx} \qquad \left(\because \varepsilon = -\dfrac{dV}{dx} \right)$

or $\quad dV = V_T \dfrac{dn}{n}$

On integration, we have

$$\int_{V_1}^{V_2} dV = V_T \int_{n_1}^{n_2} \frac{dn}{n}$$

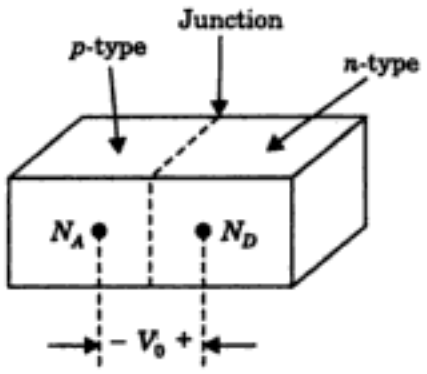


Fig. 1.15 A p-n junction in which p and n are uniformly doped with impurity concentrations N_A and N_D, respectively.

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$$V_2 - V_1 = V_T \left[\ln n\right]_{n_1}^{n_2}$$

or $$V_{21} = V_o = V_T \ln \frac{n_2}{n_1}$$

But $$n_2 = n_{n_o} = N_D \text{ and } n_1 = n_{p_o} = \frac{n_i^2}{p_{p_o}} = \frac{n_i^2}{N_A}$$

Therefore, we get $$V_o = V_T \ln \frac{N_A N_D}{n_i^2}.$$ Hence verified.

EXAMPLE 1.6

Verify the Boltzmann relationship for an open-circuited graded semiconductor.

Solution: The Boltzmann relationship to be verified is:

$$n_1 = n_2 \, \varepsilon^{-V_{21}/V_T}$$

As $$J_n = q\mu_n n\varepsilon + qD_n \frac{dn}{dx} = 0$$

(net current being zero for open circuit)

$$\therefore \quad \varepsilon = -\frac{D_n}{\mu_n} \frac{1}{n} \frac{dn}{dx}$$

$$= -\frac{V_T}{n} \frac{dn}{dx} \qquad \left(\because \frac{D_n}{\mu_n} = V_T\right)$$

i.e., $$-\frac{dV}{dx} = -\frac{V_T}{n} \frac{dn}{dx}$$

On integrating, we get

$$\therefore \quad V_{21} = V_T \int_{n_1}^{n_2} \frac{1}{n} dn$$

$$= V_T \left[\ln n\right]_{n_1}^{n_2}$$

$$= V_T \ln \frac{n_2}{n_1}$$

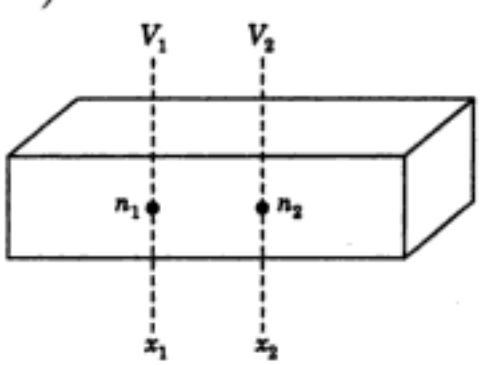


Fig. 1.16 A graded semiconductor.

or $$\frac{n_2}{n_1} = \varepsilon^{V_{21}/V_T}$$

or $$n_1 = n_2 \, \varepsilon^{V_{21}/V_T}$$

where n_1 = Concentration at $x = x_1$
n_2 = Concentration at $x = x_2$
$V_{21} = V_2 - V_1$ = Voltage at x_2 – Voltage at x_1. **Hence verified.**

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EXAMPLE 1.7

The resistivities of the two sides of a step-graded Silicon junction are 5 Ωcm (p side) and 2.5 Ωcm (n side). Calculate the height of the potential barrier V_o. Take μ_p = 475 cm²/Vs and μ_n = 1500 cm²/Vs at the room temperature of 300 K, and $n_i = 1.45 \times 10^{10}$ atoms/cm³.

Solution: Let $p_p = N_A$ and $n_n = N_D$.

Given $\rho_p = 5$ Ωcm, $\mu_p = 475$ cm²/Vs,

$\rho_n = 2.5$ Ωcm, $\mu_n = 1500$ cm²/Vs

But $$\rho_p = \frac{1}{\sigma_p} = \frac{1}{q\mu_p p_p} \qquad (\because \sigma_p = q\mu_p \cdot p_p)$$

$\therefore$ $$N_A = \frac{1}{q\,\mu_p\,\rho_p} \qquad (\because p_p = N_A)$$

$$= \frac{1}{(1.6\times10^{-19})\times 475 \times 5} = 2.631 \times 10^{15} \text{ atoms/cm}^3$$

Similarly, $$N_D = \frac{1}{q\,\mu_n\,\rho_n} \qquad (\because p_p = N_A)$$

$$= \frac{1}{(1.6\times10^{-19})\times 1500 \times 2.5} = 1.667 \times 10^{15} \text{ atoms/cm}^3$$

As $$V_o = V_T \ln \frac{N_A N_D}{n_i^2} \qquad \text{(Eq. (1.48))}$$

$$= (25) \ln \frac{(2.631\times10^{15})(1.667\times10^{15})}{(1.45\times10^{10})^2}$$

$$= 25 \times 2.3 \log_{10}\left(\frac{2.631\times1.667}{(1.45)^2}\times10^{10}\right)$$

$$= (25) \times 2.3\ (0.3198 + 10)$$

$\therefore$ V_o = 593.389 mV **Ans.**

EXAMPLE 1.8

(a) Determine the concentration of free electrons and holes in a sample of Germanium at 300°K which has a concentration of donor atoms equal to 2×10^{14} atoms/cm³ and a concentration of acceptor atoms equal to 3×10^{14} atoms/cm³. Is this p- or n-type Germanium? In other words, is the conductivity due primarily to holes or to electrons?

(b) Repeat Part (a) for equal donor and acceptor concentration of 10^{15} atoms/cm³. Is this p- or n-type Germanium?

(c) Repeat Part (a) for donor concentration of 10^{16} atoms/cm³ and acceptor concentration 10^{14} atoms/cm³.

Solution: Given $N_D = 2 \times 10^{14}$ atoms/cm³, $N_A = 3 \times 10^{14}$ atoms/cm³, $n_i = 2.5 \times 10^{13}$ atoms/cm³ at 300K (for *Ge*)

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(a) We know that $N_A + n = N_D + p$ and $np = n_i^2 = 6.25 \times 10^{26}$.

$\therefore$ $3 \times 10^{14} + n = 2 \times 10^{14} + p$

or $p - n = 1 \times 10^{14}$

or $p - \frac{n_i^2}{p} = 1 \times 10^{14}$

or $p^2 - 1 \times 10^{14} - 6.25 \times 10^{26} = 0$

or $p \times 10^{-13} = \frac{+10 \pm \sqrt{100 + 25}}{2}$

$= -0.59, 10.59$

Neglecting -0.59 as p should be +ve, we have

$p = 10.59 \times 10^{13}$ atoms/cm^3.

Now, $n = \frac{n_i^2}{p}$

$= \frac{6.25 \times 10^{26}}{10.59 \times 10^{13}} = 0.59 \times 10^{13}$

Thus,

$$\left.\begin{aligned} p &= 10.59 \times 10^{13} \text{ atoms/cm}^3 \\ n &= 0.59 \times 10^{13} \text{ atoms/cm}^3 \end{aligned}\right\} \quad \textbf{Ans.}$$

Therefore, Ge material is p-type as $p > n$.

(b) If $N_A = N_D = 10^{15}$ atoms/cm^3, then from the following equation:

$N_A + n = N_D + p$

we have $n = p$

Also $n \,.\, p = n_i^2$

Clearly, $n = p = n_i$. Therefore, Ge is intrinsic by composition

(c) Here $N_D = 10^{16}$ atoms/cm^3.

and $N_A = 10^{14}$ atoms/cm^3.

As $N_D >> N_A$

Therefore, $N_A + n = N_D + p$ gives us

$n \simeq N_D + p$

$n \simeq N_D = 10^{16}$ atoms/cms

and $p = \frac{n_i^2}{n}$

$= \frac{6.25 \times 10^{26}}{10^{16}} = 6.25 \times 10^{10}$ atoms/cm^3

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As $p = 6.25 \times 10^{10}$ atoms/cm^3

$\therefore$ $n = 1 \times 10^{16}$ atoms/cm^3

Thus, the Ge is n-type. **Ans.**

In this chapter, we have briefly given the physics of semiconductor, explaining the concept of doping mass-action law and barrier potential. Einstein relation connecting mobilities and (μ_p, μ_n), diffusion constants (D_p, D_n) and V_T has been given. The concept of diffusion and drift currents was used to prove that an open circuited bar of semiconductor cannot pass current. Potential barrier voltage (V_o) in respect of an important semiconductor device (i.e. p-n junction) has been derived.

The bare minimum related physical properties as given in this chapter, will enable us to cover the operation and use of diodes and junction/field effect transistors. Additional physical properties will be explained in some other chapter (such as Devices) on need based basis.

SUMMARY

The important points discussed in this chapter are as follows:

- Electric field intensity ε_x causes a positive charge to move along the direction of the field. An electron moves against the direction of the electric field.
- If charges (+ve or –ve) have a non-uniform gradient, the charges move along the direction of negative gradient.
- Potential V is the work done on a unit positive charge of one coulomb to move it from infinity to the point where the potential V is measured.

$$V_{10} = -\int_{x_0}^{x_1} \varepsilon_x \, dx$$

- In metals the outer or the valence electrons are very loosely attached and require extremely small electric force to move (pull) them out of the valence bond. These loose electrons contribute to electron gas.
- When the electrons move under the effect of electric field, they collide with the other electrons. This collision restricts the movement and the velocity attained is finite, depending upon μ, the mobility constant.
- Electrons are more mobile than the holes (i.e., $\mu_n > \mu_p$). Therefore, currents caused by electron movement give fast switching actions.
- Intrinsic semiconductor materials, such as Silicon and Germanium, have very small number of free charge carriers. By doping the intrinsic material, say, Silicon we can obtain p-type extrinsic Silicon (by doping with trivalent dopant such as Boron, Indium and Gallium). By using a pentavalent dopant (such as Phosphorus, Arsenic and Antimony) we obtain n-type extrinsic Silicon.
- The extrinsic (doped) semiconductors can cause greater currents compared to the intrinsic (pure) semiconductors.
- A hole has a charge of $+q$ and mass of $-m$. If an electron and a hole combine, it results zero charge and zero mass.

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- The mass action law: $p.n = n_i^2$ holds for the extrinsic semiconductor materials. In a p-material, $p \approx N_A$ and $n = n_i^2/N_A$ and in n-material, $n = N_D$ and $p = n_i^2/N_D$.
- n_i is temperature dependent and increases with increase in temperature.
- Due to electric field,

$$J_p = q\mu_p p\varepsilon_x \text{ and } J_n = q\mu_n n\varepsilon_x$$

and due to diffusion,

$$J_p = -qD_p\frac{dp}{dx} \text{ and } J_n = qD_n\frac{dn}{dx}$$

- Einstein relationship connects the mobility and diffusion constant, i.e.,

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = V_T$$

- Barrier potential in a step-graded p-n junction is:

$$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

REVIEW QUESTIONS

1.1 Define electric field intensity, potential energy and electron volt.

1.2 What is meant by electron gas in a conductor?

1.3 Define mobility, conductivity and diffusion constants.

1.4 What is a hole? Why holes are less mobile compared to the electrons?

1.5 How do intrinsic and extrinsic semiconductors differ?

1.6 How do we obtain an n, n^+, p, p^+ materials?

1.7 A semiconductor material has donor and acceptor concentrations of N_D and N_A, respectively. How do we determine the electron n and hole p concentrations?

1.8 As the temperature increases, does the resistance of a semiconductor increase or decrease?

1.9 What is the difference between diffusion and drift current?

1.10 A semiconductor extrinsic material has hole and electron concentrations of p and n, respectively. What is the total (a) diffusion current (b) drift current?

NUMERICAL PROBLEMS

P1.1 For pure Germanium, the mobilities of free electrons and holes are respectively 0.38 m^2/Vs and 0.18 m^2/Vs. The corresponding values for pure Silicon are 0.13 m^2/Vs and 0.05 m^2/Vs. Find the values of intrinsic conductivity for both these materials. Assume $n_i = 2.5 \times 10^{19}/m^3$ for Germanium and $n_i = 1.5 \times 10^{16}/m^3$ for Silicon at room temperature.

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[**Hint.** (a) For Germanium

$\sigma_i = qn_i (\mu_n + \mu_p)$ [From Eq. (1.28)]

$= (1.6 \times 10^{-19}) (2.5 \times 10^{19}) \times (0.38 + 0.18) = 2.24\ (\Omega m)^{-1}$ ***Ans.***

(b) For Silicon

$\sigma_i = (1.6 \times 10^{-19}) (1.5 \times 10^{16}) (0.13 + 0.05) = 0.43\ (\Omega m)^{-1}$ ***Ans.***]

P1.2 A 0.2 mm long bar of Silicon with cross-section 0.2 × 0.2 mm results in 8 mA current with 1 V impressed voltage across the bar. Assuming that the current is due to electrons, determine: (a) concentration of free electrons and (b) the drift velocity. Assume at 300 K, $\mu_n = 1300\ cm^2/Vs$ and $q = 1.6 \times 10^{19}$ C.

(***Ans.*** (a) Electron concentration = $1.92 \times 10^{21}/m^3$, (b) Drift velocity $v_d = 650$ m/s)

P1.3 Find the intrinsic carrier concentration of Germanium, if its intrinsic resistivity at 300 K is 0.47 Ωm. It is given that the electronic charge is 1.6×10^{-19} C and that electron and hole mobilities at 300 K are 0.39 and 0.19 m^2/Vs.

(***Ans.*** $n_i = 2.3 \times 10^{19}/m^3$)

P1.4 In a Germanium sample, a donor type impurity is added to the extent of 1 atom per 10^8 Germanium atoms. Show that the resistivity of the sample drops to 3.7 Ωcm. The given parameters are:

$\mu_n = 3800\ cm^2/Vs$; $\mu_p = 1800\ cm^2/Vs$;

$n_i = 2.5 \times 10^{13}/cm^3$; $N_{Ge} = 4.41 \times 10^{22}/cm^3$;

$q = 1.602 \times 10^{-19}$ C.

P1.5 Find the resistivity of intrinsic Silicon. What will this change to, when the Silicon is doped with a pentavalent impurity atoms with 1 atom for 50×10^6 Silicon atoms. The given data is:

Number of Silicon atom = $4.96 \times 10^{22}/cm^3$; Electron charge = 1.6×10^{-19} C; Intrinsic carrier concentration = $1.52 \times 10^{10}/cm^3$; Hole mobility = 0.048 m^2/Vs; Electron mobility = 0.135 m^2/Vs.

[**Hint.** Intrinsic resistivity $\rho = \frac{1}{\sigma} = \frac{1}{4.5 \times 10^{-6}} = 2.22 \times 10^5\ \Omega cm$

To find resistivity of doped Silicon,

$$N_D = \frac{Ni}{50 \times 10^6} = \frac{4.96 \times 10^{22}}{50 \times 10^6} = 9.92 \times 10^{14}/cm^3$$

No. of free electrons in the semiconductor $n = N_D = 9.92 \times 10^{14}/cm^3$

$$p = \frac{n_i^2}{N_D} = \frac{(1.52 \times 10^{10})^2}{9.92 \times 10^{14}} = 2.33 \times 10^5/cm^3$$

$$\sigma = qn\mu_n = (1.6 \times 10^{-19})(9.92 \times 10^{14})(0.135 \times 10^4) = 0.21\ (\Omega cm)^{-1}$$

$$\rho = \frac{1}{\sigma} = \frac{1}{0.21} = 4.67\ \Omega cm$$ ***Ans.***]

P1.6 Find the concentration of holes and electrons in a *P*-type Germanium at 300 K, if the conductivity is 100 per Ωcm. Also, find these values for *N*-type Silicon, if the

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conductivity is 0.1 per Ωcm. Given that for Germanium, $n_i = 2.5 \times 10^{13}/cm^3$, $\mu_n = 3800\ cm^2/Vs$, $\mu_p = 1800\ cm^2/Vs$, and for Silicon, $n_i = 1.5 \times 10^{10}/cm^3$; $\mu_n = 1300\ cm^2/Vs$ and $\mu_p = 500\ cm^2/Vs$.

(***Ans.*** $p = 3.47 \times 10^{17}/cm^3$; $n = 1.8 \times 10^9/cm^3$ for p-type Germanium and $p = 4.7 \times 10^5/cm^3$; $n = 4.8 \times 10^{14}/cm^3$ for N-type Silicon)

P1.7 (a) An intrinsic semiconductor (Silicon) has 5×10^{28} atoms/m^3 at 20°C room temperature. At this temperature, there are 1.5×10^{16} electron-hole pairs. Find the conductivity of Silicon (σ) at 20°C.

(b) If the above material is doped with Indium atoms at the rate of 1 atom per 10^7 Silicon atoms, find the conductivity of the doped material at room temperature.

(c) If the conductivity increases at the rate of 5% per °C. Find the conductivity of Silicon at 34°C. The given data is: $\mu_p = 0.048\ m^2/Vs$, $\mu_n = 0.135\ m^2/Vs$, $q = 1.602 \times 10^{-19}$ C.

[**Hint.** (a) $\sigma = qn_i(\mu_n + \mu_p) = 0.44 \times 10^{-3}\ (\Omega m)^{-1}$

(b) $N_A = \dfrac{5 \times 10^{28}}{10^7} = 5 \times 10^{21}/m^3$

$\therefore \quad n = \dfrac{n_i^2}{N_A} = \dfrac{(1.5 \times 10^{16})^2}{(5 \times 10^{21})}$

$= 4.5 \times 10^{10}/m^3$

$\sigma = qp\mu_p \approx qN_A\mu_p = 38\ (\Omega m)^{-1}$ ***Ans.***

(c) $\alpha = 0.05/°C$. Here $\Delta T = 34 - 20 = 14°C$

and conductivity at 20°C $= 0.44 \times 10^{-3}\ (\Omega m)^{-1}$

$\therefore \quad \sigma$ at 34°C $= (0.44 \times 10^{-3})(1 + \alpha \Delta T)$

$= (0.44 \times 10^{-3})(1 + 0.05 \times 14) = 0.75 \times 10^{-3}\ (\Omega m)^{-1}$ ***Ans.***]

P1.8 (a) For an intrinsic specimen of semiconductor material with $n_i = 1.48 \times 10^{10}$ electrons (holes)/cm^3 at 300K, electron mobility $\mu_n = 1300\ cm^2/Vs$ and the hole mobility $\mu_p = 500\ cm^2/Vs$, calculate the value of conductivity.

(b) If a Si specimen is doped with an appropriate n-type (donor) material to a small concentration of one part per million atoms, determine the resulting conductivity of the specimen in Part a.

(c) The mobility is known to vary over a temperature range from 200K to 400K as $T^{2.6}$, find the approximate mobilities of electrons and holes in Si at $T = 400K$.

(***Ans.*** (a) 2.35×10^5 Ωcm; (b) σ (with doping) $= 10.37\ (\Omega cm)^{-1}$; (c) $\mu_n \approx 2746\ cm^2/Vs$ and $\mu_p \approx 1056\ cm^2/Vs$).

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CHAPTER 2 The *p-n* Junction Diode

2.1 INTRODUCTION

In this chapter, we shall learn about the physical properties of a *p-n* junction diode. The *p-n* junction diode is the basic building block on which the operation of all the semiconductor devices depends. The *p-n* junction itself is a two-element device. The word *diode* was coined from *di* + electr*odes*, i.e., having two terminals. With the invention of valves, the first most useful electronic device was the diode and triode. Tetrode, pentode, etc. were invented afterwards. However, with the invention of transistors, *p-n* junction acting as a diode continues to be used extensively for various operations.

We shall cover the operation modes (forward- and reverse-biased *p-n* junction), large signal and small signal models and switching times of *p-n* junction diodes in this chapter. The volt-ampere characteristics and the capacitance across the *p-n* junction is also covered. After discussing the main properties of *p-n* junctions, we shall consider their applications in Chapter 3.

2.2 THE *p-n* JUNCTION

A *p-n* junction is formed when a single crystal of semiconductor is doped with an acceptor on one side (to make this side *p*-type) and with a donor on the other side (to make this side *n*-type). Schematic details of a *p-n* junction are shown in Fig. 2.1. The doping atoms are shown in large circles, a hole by small circle (o) and an electron by a solid small circle (•). Note that each doping atom is neutral (and so are all the intrinsic atoms of Silicon or Germanium). A pentavalent (donor) dopant element is shown by large circle with +ve sign in it (i.e., ⊕) and an electron is shown along with it, thus ⊕ indicates +ve ion with a +ve charge equal to that of an electron. Similarly, an acceptor type doping element (a trivalent atom) is shown as a –ve ion ⊖ along with a hole (•). As the doping atom is neutral, therefore, the ion ⊖ has a –ve charge equal to that of an electron. As mentioned earlier the

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donors are all pentavalent element such as Antimony (Sb), Arsenic (As) and Phosphorus (P); and the acceptors are all trivalent elements such as Boron (B), Indium (In) and Gallium (Ga).

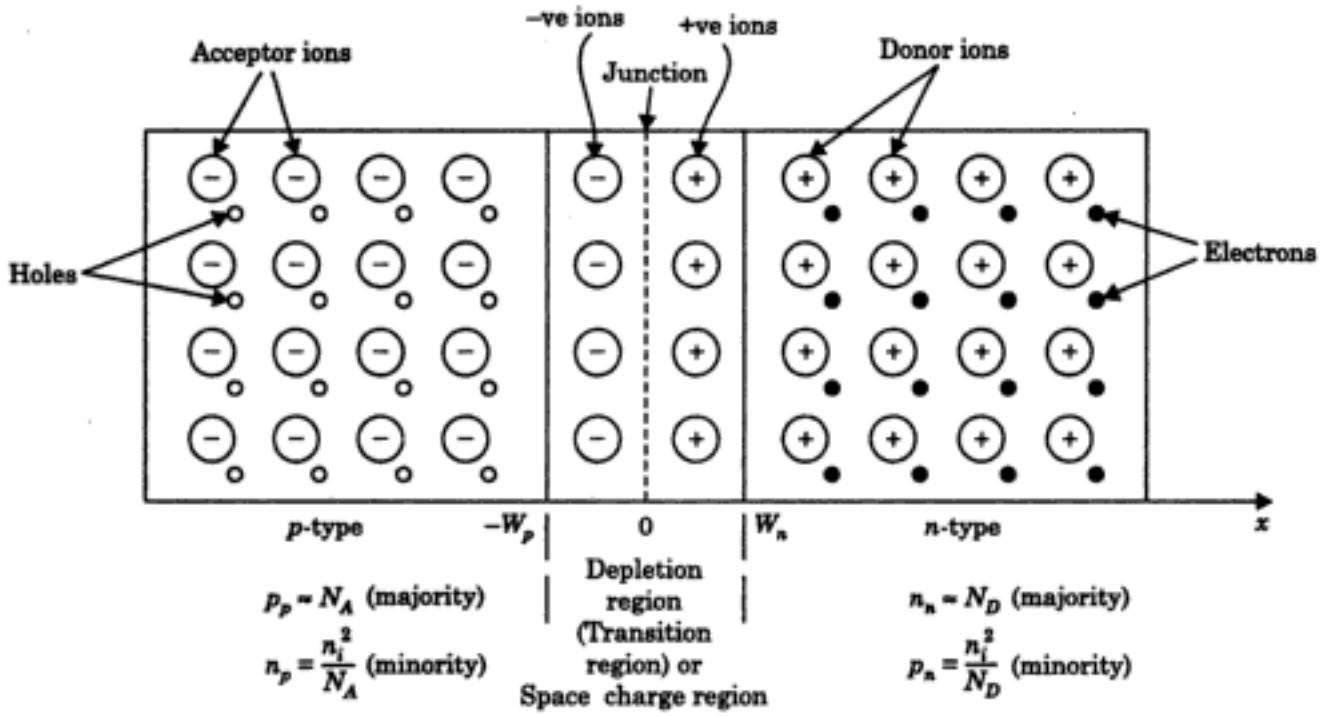


Fig. 2.1 Schematic details of a *p-n* junction diode. The approximate values of charge carrier concentrations (*p* and *n*) are shown on the respective side.

2.3 THE OPEN CIRCUITED *p-n* JUNCTION

Consider the situation as shown in Fig. 2.1. It is clear that on the opposite sides of the junction the charge carriers have different concentrations. For example, the hole concentration p_p on the *p*-side (LHS of the junction in Fig. 2.1) is much greater than the hole concentration p_n on the *n*-side (RHS of the junction in Fig. 2.1). Similarly, the values of n_n is much higher than n_p, where n_n and n_p are the electron concentrations on *n*-side and *p*-side, respectively. We call this situation by saying that there is a concentration gradient across the *p-n* junction.

The holes on *p*-side and the electrons on *n*-side tend to come close to the junction and even cross to the other side and holes and electrons combine in equal number. This implies that if an acceptor atom ($\ominus^\circ$) has lost its hole and it is reduced to a –ve charged ion ($\ominus$), then an electron from a donor atom ($\oplus^\cdot$) combines with the hole (which carries the acceptor atom) and the donor atom gets converted to a +ve charged ion ($\oplus$). It is clear that the number of –ve ions ($\ominus$) produced on *p*-side is equal to the +ve ions ($\oplus$) produced on *n*-side due to the diffusion/recombination process. The region around the *p-n* junction which has lost its free charge carriers (holes and the electrons) has only ions in that region. This region is called **depletion region** or **transition region** or **space charge region**. These names obviously indicate the status of the region as this region has lost its free charge carriers (hence depletion region), is a transition from *p* to *n* side (hence transition region) and

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contains +ve and –ve charged ions (hence space charge region). The width of the depletion region is only a few tenths of a micrometre. Also note that the p-n junction lies inside the depletion region, i.e., the depletion region appears around the p-n junction. In case the concentration of holes p_p on p-side is equal to the concentration of electrons n_n on the n-side, the p-n junction will lie in the middle of the depletion region, since the number of –ve ions formed on p-side must be equal to the +ve ions formed on n-side. With $p_p = n_n$ the depletion width W_p on the p-side is equal to the depletion width W_n, i.e., for $p_p = n_n$ we have $W_p = W_n$. However, if, say, $p_p >> n_n$, then $W_p << W_n$, since only small width W_p can cover as many –ve ions (⊖) as does the width W_n covers +ve ions (⊕) in this case. This suggests us that the depletion widths (W_p and W_n) in p-side and n-side can always be made unequal by choosing the doping concentration N_A and N_D different. We shall learn in the chapter on Field Effect Transistors (FET) that it is desirable to make one width, say, W_p much lower than the width W_n, and in this case the overall depletion width $W = W_p + W_n \approx W_n$. We only need to make N_A much higher than N_D for the junction.

It is important to note that the formation of depletion region generates +ve charge on n-side of the junction and –ve charge on p-side of the junction due to the ions so formed. There is a stable state when further widening of depletion region stops. When the +ve charge on n-side is sufficient strong, it repels any additional holes from p-side to cross to the n-side. Similarly, the strong –ve charge in depletion region on p-side stops any additional electrons from n-side to cross the junction.

Also, in open circuited p-n junction, no current flows across the junction or outside the p-n diode. Suppose, for the open circuited p-n junction diode, current could flow from p- to n-side across the junction due to law of diffusion. Due to the open circuit of the diode the holes flowing from p- to n-side, if any, would accumulate on n-side. This would make n-side having higher holes concentration than the p-side; causing electric field from n- to p-side, the law of drift will apply, and these "extra holes" on n-side will go back to p-side. In fact, the space charge in the depletion region forms an electric field across the junction which stops the shift of majority carriers across the junction. It is, therefore, concluded that there is an equilibrium condition, and a zero resultant current flows in an open circuited p-n junction diode.

2.4 CHARGE DISTRIBUTION, ELECTROSTATIC POTENTIAL AND POTENTIAL BARRIER DUE TO DEPLETION REGION

We now calculate the parameters like charge distributions, electrostatic potential and the potential barrier created due to the depletion region. In the depletion region we have only ions (and not free charge carriers). Figure 2.2(a) shows an open circuited p-n junction and the depletion region.

Since the region $0 < x < W_n$ has +ve charged ions and the region $-W_p < x < 0$ has –ve charged ions, the charge density distribution ρ_v has typical curve shown in Fig. 2.2(b). The electric field intensity $\mathscr{E}(x)$ can be obtained from Poisson's equation:

$$\frac{d^2V}{dx^2} = -\frac{\rho_v}{\varepsilon} \qquad \text{(Poisson's Equation)} \qquad (2.1)$$

$$\mathscr{E}(x) = -\frac{dV}{dx} \qquad \text{[due to Eq. (1.7)]} \qquad (2.2a)$$

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Integrating Eq. (2.1a), we get

$$\mathcal{E}(x) = \int \frac{1}{\varepsilon} \rho_v(x)\, dx \tag{2.2b}$$

$\mathcal{E}(x)$ is shown in Fig. 2.2(c).

Clearly, the curve for $\mathcal{E}(x)$ is proportional to the integration of charge density $\rho_v(x)$. As maximum –ve charge is in the area from $x = -W_p$ to $x = 0$, therefore, $\mathcal{E}(x)$ is maximum –ve at $x = 0$. As we take area of the curve under $\rho_v(x)$ after $x = 0$, the net area under $\rho_v(x)$ curve becomes less negative till at $x = W_n$, the total area of curve $\rho_v(x)$ for $-W_p$ to W_n is zero. This is expected because the number of –ve ions in $x = -W_p$ to $x = 0$ are equal to +ve ions in the range $x = 0$ to $x = W_n$. Hence $\mathcal{E}(x)$ has zero value in the range away from the depletion region, i.e. no electric field exists in the region $x < -W_p$ and $x > W_n$. It also implies that the potential at all the points for $x < -W_p$ part of the (undepleted) p-n diode is equal, i.e., if we, say, apply a voltage V_1 on p-side of the p-n diode, then the potential of every point in the undepleted portion on p-side of the p-n junction will be V_1. Similarly, the potential of undepleted part ($x > W_n$) of the p-n diode will be the same.

The electrostatic potential $V = -\int \mathcal{E}(x)\, dx$ i.e., the value of potential V is negative of integration (i.e., area) under curve $\mathcal{E}(x)$. The value of V is clearly zero at $x = -W_p$ and V has maximum value at $x = W_n$, say, V_0, and for $x > W_n$, V remains at V_0. This has been shown in Fig. 2.2(d). It is this potential barrier which prevents further broadening of the depletion region for the open circuited p-n junction. Point $x = W_n$ is at potential + V_0 and this potential does not allow any

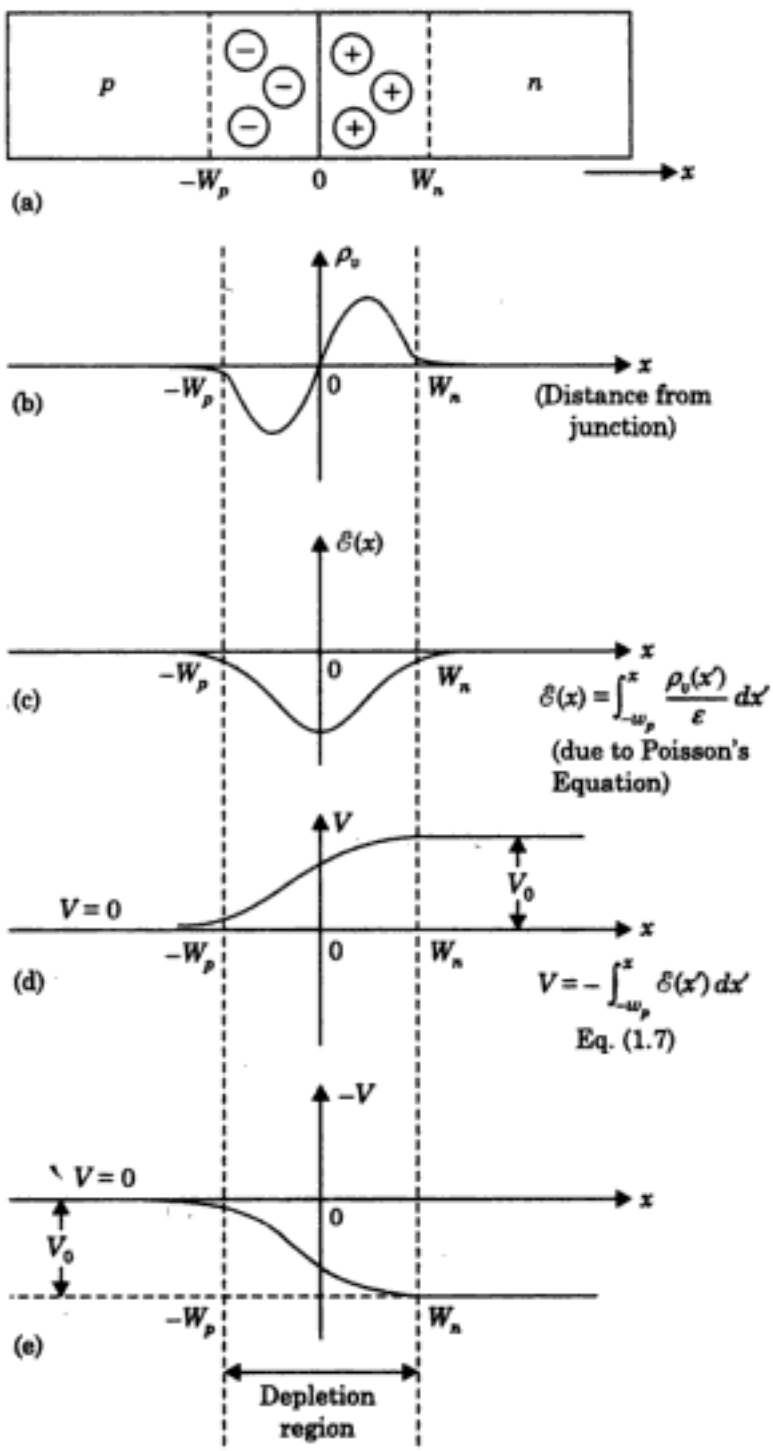


Fig. 2.2 (a) The p-n junction with depletion region from $-W_p$ to W_n (b) The charge density ρ_v (c) Electric field intensity $\mathcal{E}(x)$ (d) Electrostatic potential V (e) Potential energy barrier for electrons ($-V$).

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additional holes from p-side to cross the p-n junction. Similarly, we may argue that the point $x = -W_p$ is at potential $-V_0$ w.r.t n-side. Hence this does not permit additional electrons from n-side to cross the p-n junction. So, there is an equilibrium state keeping the depletion region width constant. The potential energy barrier for electrons is negative of that for the holes. This is shown in Fig. 2.2(e). In practical p-n junctions, V_0 has the value 0.2 V to 0.8 V. The potential barrier voltage V_0 is also called the **cut-in voltage**.

2.5 FORWARD AND REVERSE BIASING THE *p-n* JUNCTION

We have earlier learnt that an open circuited p-n junction diode developes a depletion region (of total width $W = W_p + W_n$ shown in Fig. 2.1) and that a barrier voltage of V_0 is developed [as shown in Fig. 2.2(d) and 2.2(e)]. Such a barrier voltage makes the depletion width W constant under equilibrium state. Now, we learn that the width W of the depletion region can be varied (increased or decreased or even made zero) by application of voltage externally across the p and n electrodes. We shall call the metal contact on p-side end as **anode** and the metal contact on n-side end as the **cathode** as indicated by A and C, respectively, in Fig. 2.3.

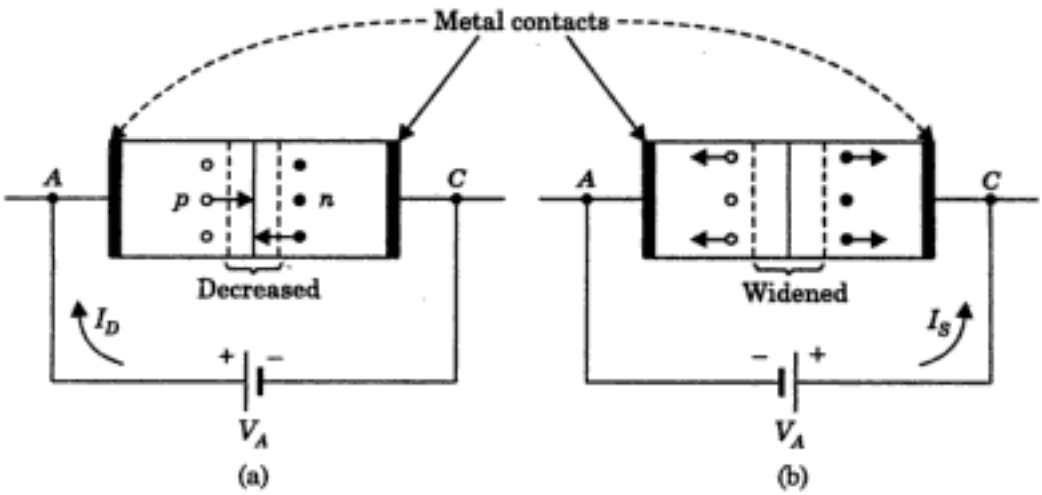


Fig. 2.3 (a) Forward-biased p-n junction (depletion region decreases) (b) Reverse-biased p-n junction (depletion region increases). A and C indicate anode and cathode contacts, respectively.

2.5.1 Forward-Biasing the *p-n* Junction

If we apply a voltage, say, V_A with +ve on anode side and –ve on cathode side [see Fig. 2.3(a)], this is called **forward biasing** the p-n juncton diode. This makes the net barrier voltage across the junction as $V_0 - V_A$. Assume that V_A is less than V_0 then the net barrier reduces from V_0 to $V_0 - V_A$ and does not become zero. The +ve V_A voltage on anode of the p-n diode repels the holes of the undepleted region of the p-side towards the junction. This in turn neutralizes some of the –ve ions ($\ominus$) of the acceptor atoms and makes them again neutral. Thus, net –ve charge in the erstwhile depleted region from $x = -W_p$ to $x = 0$ (see Fig. 2.1) is reduced, i.e., net –ve ions ($\ominus$) in this region are reduced, i.e., the width $-W_n$ to 0 decreases. Similarly, application of V_A voltage with –ve on cathode side decreases the depletion

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region from erstwhile $x = 0$ to $x = W_n$ to a value lower than W_n. The overall effect of forward biasing of the *p-n* junction diode, therefore, decreases the depletion width from $W(= W_p + W_n)$ to a lower value than W, and the revised potential barrier due to the decreased depletion width is now $V_0 - V_A$. We also note that if $V_A = V_0$, the net barrier voltage reduces to zero and the depletion region reduces to zero width. In other words, for $V_A \geq V_0$, the barrier to the flow of charge carriers (holes and the electrons) completely vanishes, and in fact for $V_A > V_0$ there is a "helping" (antibarrier) voltage equalling $V_A - V_0$ which will cause a diode current. Thus, when V_A exceeds V_0, it causes a forward current (flowing from Anode to Cathode) in the diode.

2.5.2 Reverse-Biasing the *p-n* Junction

The effect of reverse-biasing the junction is opposite to that of the forward biasing. Let us apply voltage V_D with –ve polarity on the anode and +ve polarity on the cathode side of the *p-n* junction diode [see Fig. 2.3(b)] such a polarity of V_D makes the holes of *p*-side and electrons of *n*-side all the more difficult to go towards the junction or to cross it. In fact the –ve voltage applied on anode side attracts some holes from the *p*-side and creates more –ve ions (⊖) thereby. Similarly, the +ve voltage applied on cathode side attracts some more electrons and creates additional +ve ions (⊕). Such action widens the depletion region. The resultant barrier potential is now $V_0 + V_D$.

It may be, however, noted that the reverse biasing voltage V_D helps the minority carriers to go towards the junction. In Fig. 2.1, the minority carrier concentration has been indicated by n_p on *p*-side (where the electrons are in minority) and p_n on *n*-side (where the holes are in minority). Clearly, a +ve voltage on cathode repels the minority carrier holes p_n on *n*-side to proceed towards the junction, and these are further helped by the negative ions on the other side of the junction to continue flowing. In short, the reverse voltage (+ve on cathode) causes holes to move from RHS to LHS in Fig. 2.1. Similarly, the reverse voltage on anode (i.e., –ve voltage) causes the minority electrons n_p on *p*-side to travel towards the junction, and are assisted by the +ve ions (⊕) on the other side of the junction. The net result of above mentioned movement of minority carriers under the influence of reverse biasing is flow of reverse current, i.e., a current from *n*-side to *p*-side inside the *p-n* diode. This current is due to movement of minority carriers, and is called **reverse saturation current** and is denoted by the symbols I_S. As the minority carriers are very small in number (compared to the majority carriers p_p and n_n), the reverse saturation current cannot exceed beyond a limit I_S. The current I_S is calculated assuming that all the available minority charge carriers (p_n and n_p) are generating this current. We shall deal with the current I_S in Section 2.6 when we discuss the volt-ampere characteristics of a *p-n* junction diode. Also, we shall discuss the effect of applying high reverse biasing voltage when we discuss Zener breakdown or the Avalanche effect.

2.5.3 Contact Points for Anode and Cathode (Ohmic Contacts)

In order to make necessary connections on anode and cathode sides of the *p-n* junction diode metal contacts are provided as shown in Fig. 2.3. These contacts are assumed to be non-rectifying and are called ohmic contacts, i.e., the potential difference across these metal contacts and semiconductor material (*p* or *n*) is constant and has very small value. We also neglect the voltage drop across the bulk of the semiconductor crystal, i.e., we assume that

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the electric field is zero in the undepleted regions of p and n parts of the semiconductor. The change in the potential barrier due to applied voltage V_D effectively occurs across the p-n junction. Hence we can assume that the application of $+V_D$ or $-V_D$ (reference point being the cathode of the diode) makes the revised barrier voltage $V_0 - V_D$ or $V_0 + V_D$, respectively.

2.5.4 Short Circuiting the p-n Junction

In Fig. 2.4, there are no free charges between the space A'–A'' and C'–C'' i.e., there is no potential difference between A' and A'' and also between C' and C''. Therefore, we can say that the barrier voltage V_0 effectively appears across points A'' and C'' as shown in Fig. 2.4. One may feel that short circuiting the anode (point A) and the cathode (point C) might cause current I_{sc} in the shorted link, due to V_0. However, due to ohmic contacts (metal contacts) at anode and cathode the voltage developed across AA' as well as across $C'C$ would be $V_0/2$ due to the current I_{sc}. The voltage drop across metal ohmic contacts will heat these contacts. Since the p-n device has not been supplied by any external power source (V_A being zero here), the heat must come from within the device and thereby cooling the device. Thus, heating and cooling of the device has to occur at the same time. This is a contradiction. Hence, there is neither heating nor cooling due to short circuiting A and C, i.e., the short circuiting current I_{sc} must be zero.

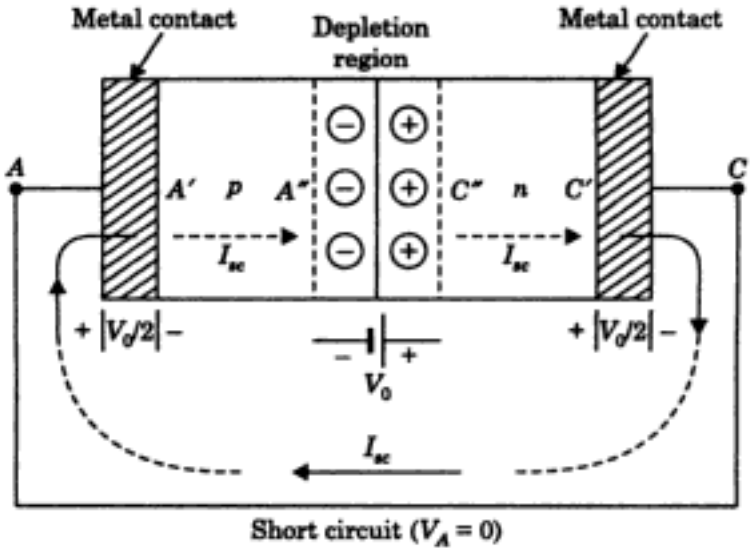


Fig. 2.4 Voltage distribution when anode and cathode terminals of the p-n junction diode are short circuited. Assuming the barrier voltage as a "battery" of voltage V_0, the short circuit I_{sc} should flow as shown.

We cannot measure the voltage V_0 across the p-n diode, by putting a voltmeter across points A and C in Fig. 2.4 when there is no short circuit. It is so because any measurement by a voltage essentially requires an extremely small current through the measuring voltmeter. Passage of any current through the p-n junction diode is not feasible as discussed earlier. Hence the voltmeter reads zero volt, i.e., we cannot measure the barrier voltage V_0 by any voltmeter.

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EXAMPLE 2.1

Assuming that the diodes in the circuits are ideal, utilize Thevenin's theorem to simplify the circuits shown in Fig. 2.5, and thus find the values of the labelled currents and voltages. Assume that an ideal diode behaves as a short-circuit when forward biased and open-circuit when reverse biased.

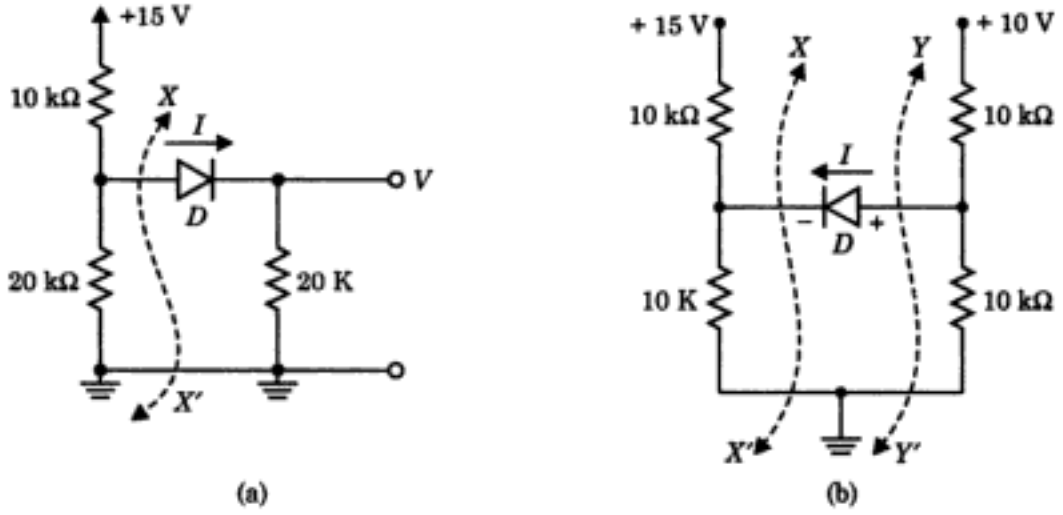


Fig. 2.5 Circuits for Ex. 2.1.

Solution:

(A) Applying Thevenin's theorem at XX', in Fig. 2.5(a),

$$V_{TH} = 15 \times \frac{20}{10+20} = 10 \text{ V}$$

$$Z_{Th} = 10 \text{ k}\Omega \parallel 20 \text{ k}\Omega$$

$$= \frac{10 \times 20}{10+20} = \frac{200}{30} = \frac{20}{3} \text{ k}\Omega$$

Clearly, from the Thevenin's equivalent diagram, in Fig. 2.5(c),

$$I = \frac{10}{\left(\frac{20}{3} + 20\right)} = \frac{30}{80} = \frac{3}{8} \text{ mA}$$

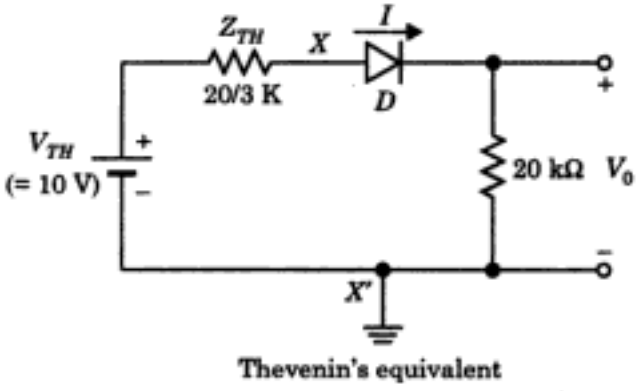


Fig. 2.5(c) Equivalent circuit from 2.5(a).

$$\therefore \quad V_0 = 20 \times \frac{3}{8} = \frac{15}{2} = 7.5 \text{ V} \quad \textbf{Ans.}$$

(B) For the circuit, shown in Fig. 2.5(b) and applying Thevenin's theorem at XX' and YY', we get

$$\therefore \quad V_{TH1} = 15 \times \frac{10}{10+10} = 7.5 \text{ V}$$

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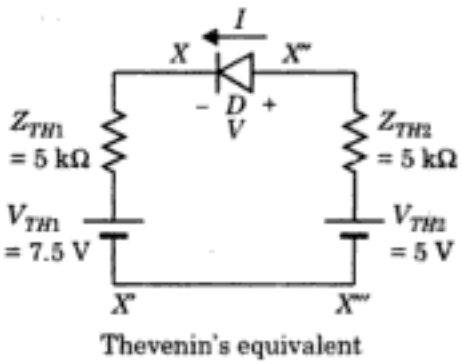
$$Z_{TH1} = 10 \| 10 = 5 \text{ k}\Omega$$

$$V_{TH2} = 5 \text{ V}, \; Z_{TH2} = 5 \text{ k}\Omega$$

From the Thevenin's equivalent diagram, showing Fig. 2.5(d) D is clearly Off since anode side is at a lower potential than the cathode side

$$\therefore \qquad I = 0$$

Thus, $$V = 5 - 7.5 = -2.5 \text{ V} \quad \textbf{Ans.}$$



Thevenin's equivalent

Fig. 2.5(d) Equivalent circuit from 2.5(b).

2.6 THE VOLT-AMPERE CHARACTERISTIC OF A *p-n* DIODE

As indicated in the previous section, we cannot measure the value of barrier voltage V_0. However, the values of voltage V_D across the junction diode and the diode current I_D can be easily measured. In Fig. 2.3(a), consider the situation when V_D (i.e., forward bias) is increased till V_D is nearly equal to V_0 (or V_γ). The barrier now will be $V_0 - V_D$ and approaches zero i.e. the barrier almost disappears and the current should be arbitrarily large. However, in practice the barrier can never be reduced to zero because the bulk resistance of the crystal as well as the resistance of the ohmic contacts limit the current even if V_D exceeds V_0. Under the conditions (as V_D becomes comparable to V_0), the current in a practical p-n junction is governed by the ohmic contacts and the semiconductor bulk resistances.

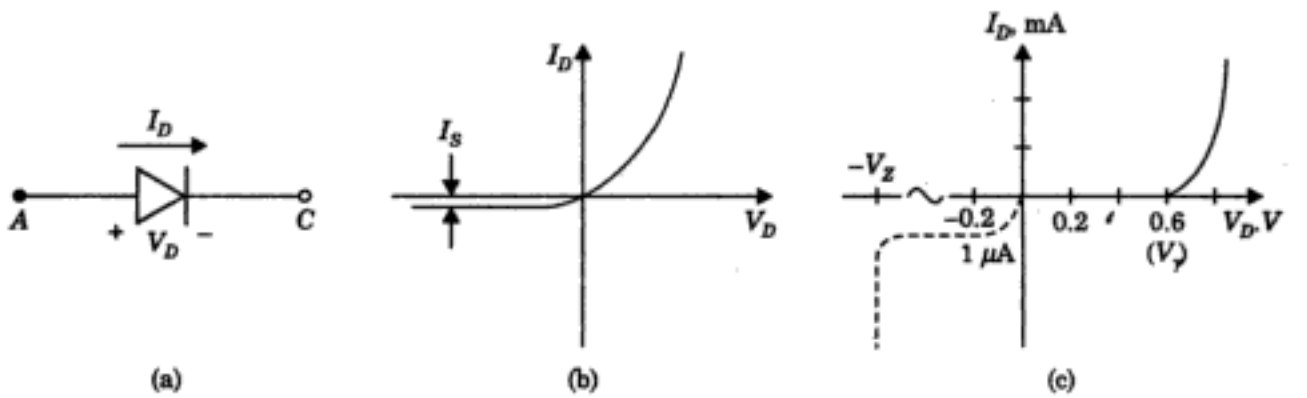


Fig. 2.6 (a) Junction diode symbol and the customary direction of current in the diode I_D and the net voltage across the junction V_D (b) $V_D - I_D$ characteristic of a junction diode and (c) The volt-ampere characteristic redrawn to clarify the magnitude of current I_D and the reverse breakdown voltage V_Z.

The volt-ampere characteristic of a diode relates the voltage V_D applied to the junction and the current I_D it produces. Theoretically, the current I_D in a diode is given by

$$I_D = I_S \left(e^{V_D / \eta V_T} - 1\right) \tag{2.3a}$$

where I_S = Reverse saturation current in Ampere

V_D = Junction voltage in volt

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η = Constant with values 2 for Silicon and 1 for Germanium diodes
V_T = Voltage equivalent of temperature at T and is given by

$$V_T = \frac{\bar{k}T}{q} \tag{2.3b}$$

where k = Boltzmann constant = 8.620×10^{-5} eV/K
$\bar{k}$ = Boltzmann constant = 1.381×10^{-23} J/K
q = Charge of an electron = 1.6×10^{-19} C

Putting the values of $\bar{k}$ and q in Eq. (2.3b), we get

$$V_T = (1.381 \times 10^{-23}) \times T/(1.6 \times 10^{-19})$$

$$= \frac{T}{11{,}585} \approx \frac{T}{11{,}600}$$

For temperature of 20°C, ($\therefore$ T = 293 K), $V_T \approx 25$ mV
For temperature of 27°C, ($\therefore$ T = 300 K), $V_T \approx 25.8$ mV
When temperature T is not specified, we assume $V_T = 25$ mV in numericals.

The diode current I_D is +ve from p-type to n-type within the semiconductor [see Fig. 2.6(a)]. The reverse saturation current I_S depends on the hole concentration p_n in n-type and electron concentration n_p in p-type, as has also been explained in the last section (reverse biasing of the p-n junction). Note that $p_n = n_i^2/N_D$ and $n_p = n_i^2/N_A$. [see Fig. (2.1)]. We can, therefore, say that the reverse saturation current I_S depends on the hole and electron concentrations (N_A and N_D). I_S serves as a "scale factor" for the junction current I_D. The capacity of junction current I_D also increases with increase in the junction area for fixed values of N_A and N_D.

From Eq. (2.3), if $V_D >> V_T$ then $e^{V_D/\eta V_T} >> 1$ and we can neglect 1 w.r.t. $e^{V_D/\eta V_T}$, and Eq. (2.1) reduces to

$$I_D \approx I_S e^{V_D/\eta V_T} \quad \text{for } V_D >> V_T \tag{2.4}$$

At T = 25 mV,

$$I_D \approx I_S e^{20V_D} \quad \text{for Silicon} \tag{2.4a}$$

$$I_D \approx I_S e^{40V_D} \quad \text{for Germanium} \tag{2.4b}$$

Equation (2.4) shows that the current I_D varies exponentially with the applied voltage V_D, as shown in Fig. 2.6(b). It is so since the increase of V_D implies decrease in the potential barrier, and more majority carriers diffuse across the junction.

Note that when V_D is sufficiently negative such that $e^{V_D/\eta V_T}$ has value much less than unity then

$$I_D \approx I_S (0 - 1)$$

$$\therefore \quad I_D = -I_S \quad \text{for reverse bias and } |V_D| >> V_T \tag{2.5}$$

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The reverse bias current I_D is –ve and equals I_S, i.e., now I_D flows from n-type to p-type in the device and is a constant. As the value of I_D in reverse bias is very small in the range of micro amps for Silicon diodes and nano amps for Germanium diodes, it has been shown on an expanded scale in Fig. 2.6(c). The current I_D remains constant at $-I_S$ till the reverse voltage V_D reaches $-V_Z$. Here the junction breakdown occurs, and V_Z is called the **zener breakdown** or **Avalanche breakdown** voltage.

EXAMPLE 2.2

Determine the change in diode voltage V_D, corresponding to 15:1 change in diode current I_D for a junction diode operating at room temperature.

Solution: We know that

$$I_D = I_S(e^{V_D/\eta V_T} - 1) \approx I_S e^{V_D/\eta V_T}$$

$$\therefore \quad I_{D_1} = I_S(e^{V_{D1}/\eta V_T})$$

and $$I_{D_2} = I_S(e^{V_{D2}/\eta V_T})$$

i.e., $$\frac{I_{D2}}{I_{D1}} = e^{(V_{D2} - V_{D1})/\eta V_T}$$

or $$\Delta V_D = V_{D2} - V_{D1} = \eta V_T \ln \frac{I_{D2}}{I_{D1}}$$

Put $\eta = 1$, $V_T = 25$ mV, $I_{D2}/I_{D1} = 15$, we get

$$\Delta V_D = 1 \times 25 \times \ln 15 = 67.7 \text{ mV} \quad \text{(for Ge)} \quad \textbf{Ans.}$$

For $\eta = 2$,

$$\Delta V_D = 2 \times 67.7 = 135.4 \text{ mV} \quad \text{(for Si)} \quad \textbf{Ans.}$$

EXAMPLE 2.3

(a) For what voltage will the reverse current in a p-n junction Germanium diode reach 90% of its saturation value at room temperature of 27°C.

(b) What is the ratio of the current for a forward bias of 0.05 V to the current for the same magnitude reverse bias?

(c) If the reverse saturation current is 10 μA, calculate the forward current for voltages of 0.1, 0.2 and 0.3 V, respectively.

Solution:

(a) Here $\eta = 1 \quad \therefore \quad \eta V_T = V_T$

At $T = 27°$, $V_T = 26$ mV.

Now, $$I = I_S(e^{V/V_T} - 1) = I_S(e^{V/0.026} - 1) \quad \text{(i)}$$

and $$I = -0.9I_S \text{ (Given), } (I \text{ –ve sign means reverse current)} \quad \text{(ii)}$$

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Equating Eqs. (i) and (ii), we get

$$-0.9I_S = I_S(e^{V/0.026} - 1)$$

or $$0.1 = e^{V/0.026}$$

or $$V = -59.85 \text{ mV}$$

(b) Forward current at $V = 0.05$ V $= I_S(e^{0.05/026} - 1)$

Reverse current at $V = -0.05$ V $= I_S(e^{-0.05/0.026} - 1)$

Then ratio of forward to reverse current $= \dfrac{I_S(e^{0.05/0.026} - 1)}{I_S(e^{-0.05/0.026} - 1)}$

$$= \frac{e^{50/26} - 1}{e^{-50/26} - 1}$$

$$= \frac{6.8419 - 1}{0.14616 - 1} = -6.84 \quad \textbf{Ans.}$$

(c) $I_S = 10\ \mu$A (given)

Now, for $V_1 = 0.1$ V $= 100$ mV

$$I_{D1} = 10(e^{100/26} - 1)$$

$$= 10(46.8126 - 1) = 458\ \mu\text{A} \quad \textbf{Ans.}$$

For $V_2 = 0.2$ V $= 200$ mV

$$I_{D2} = 10(e^{200/26} - 1)$$

$$= 10(2191.42 - 1) = 21.9\ \text{mA} \quad \textbf{Ans.}$$

and $V_3 = 0.3$ V $= 300$ mV

$$I_{D3} = 10(e^{300/26} - 1)$$

$$= 10(102586.49 - 1) = 2.025\ \text{A} \quad \textbf{Ans.}$$

EXAMPLE 2.4

In a Ge-diode, the leakage current is 10 μA and the breakdown voltage is 25 V. Compute current for

(a) Reverse bias of 24 V

(b) Reverse bias of 0.02 V

(c) Forward bias of 0.3 V

Solution: Given $I_S = 10\ \mu$A (reverse saturation current or the leakage current)

$\eta = 1$ Germanium diode case

Assume $V_T = 25$ mV at room temperature.

(c) *Forward bias*

$$I_D = I_S(e^{V_D/\eta V_T} - 1)$$

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For $V_D = 0.3$ V = 300 mV, $\eta = 1$,

$$I_D = 10 \times 10^{-6} (e^{300/25} - 1) A$$

$$= 10^{-5}(e^{12} - 1)$$

$$= 1.6275\ A \quad \textbf{Ans.}$$

Reverse bias

(a) If $V_D = -24$ V,

then $I_D = I_S(e^{V_D/V_T} - 1)$ ($\because \eta = 1$ here)

$= (10 \times 10^{-6})(e^{-24/0.025} - 1) = -10\ \mu A$ **Ans.**

(b) If $V_D = -0.02$ V,

then $I_D = (10 \times 10^{-6})\ (e^{-20/25} - 1)$

$= 20$ mV

$= (10 \times 10^{-6})(e^{-0.8} - 1)$

$= (10)(0.449328 - 1)$

$= -5.5067\ \mu A$ **Ans.**

EXAMPLE 2.5

Calculate the change in diode voltage V_D if the diode current I_D assumes the new value of 10 times the previous value. Take operating temperature $T = 300$ K.

Solution: As $I_D \approx I_S e^{V_D/\eta V_T}$ for $V_D >> V_T$

Let $I_{D1} = I_S e^{V_{D1}/\eta V_T}$ (Initial value of diode current)

and $I_{D2} = I_S e^{VD_2/\eta V_T}$ [I_{D2} is 10 times the initial diode current i.e., $I_{D2}/I_{D1} = 10$]

$$\therefore \quad \frac{I_{D2}}{I_{D1}} = e^{(V_{D2} - V_{D1})/\eta V_T} \qquad \text{(i)}$$

Taking log on both sides of Eq. (i), we obtain (using $\log_e 10 = 2.303$)

$$\log_{10} \frac{I_{D2}}{I_{D1}} = \frac{(V_{D2} - V_{D1})}{2.303\,\eta V_T} = \frac{(V_{D2} - V_{D1})}{2.303\,\eta V_T}$$

or $$V_{D2} - V_{D1} = 2.303\,\eta V_T \log_{10} \frac{I_{D2}}{I_{D1}}$$

At $T = 300$ K, $V_T = \dfrac{300}{11{,}600} = 26$ mV and $\dfrac{I_{D2}}{I_{D1}} = 10$ (Given)

$\therefore$ Voltage change $= V_{D2} - V_{D1} = 2.303\ \eta V_T \log_{10} 10$

$= 2.303\ .\ \eta\ .\ (26\ \text{mV}) \times 1 = 60\ \eta$ mV

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For $\eta = 2$, $V_{D2} - V_{D1} = 60 \times 2 = 120$ mV (for Silicon)
For $\eta = 1$, $V_{D2} - V_{D1} = 60 \times 1 = 60$ mV (for Germanium) **Ans.**

EXAMPLE 2.6

For the circuit shown in Fig. 2.7, both the diodes are identical conducting 10 mA at 0.7 V and 100 mA at 0.8 V. Find the value of R for which $V = 50$ mV.

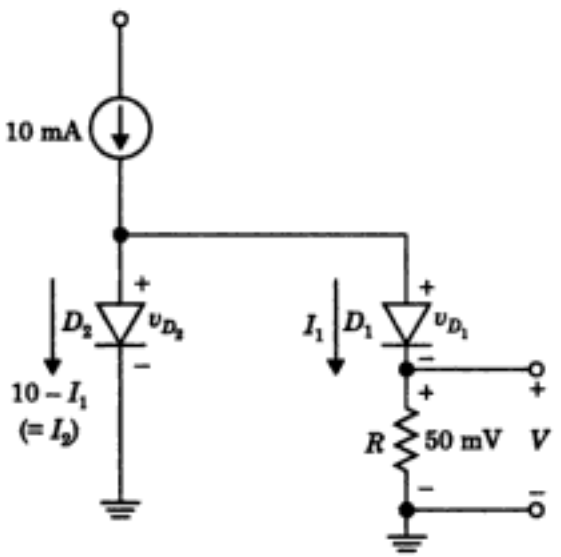


Fig. 2.7 Circuit for Ex. 2.6.

Solution: We first find the value of ηV_T from the given data. The given data is:

$$10 = I_S e^{V_{D1}/\eta V_T} = I_S e^{0.7/\eta V_T} \quad \text{(i)}$$

$$100 = I_S e^{V_{D2}/\eta V_T} = I_S e^{0.8/\eta V_T} \quad \text{(ii)}$$

Dividing Eq. (ii) by Eq. (i), we get

$$\frac{100}{10} = e^{(0.8-0.7)/\eta V_T}$$

$$\therefore \quad 10 = e^{0.1/\eta V_T}$$

Taking log on both sides, we get

$$\log_e 10 = \frac{0.1}{\eta V_T}$$

or $$\eta V_T = \frac{0.1}{2.3} = 0.0434782$$

Now, in the circuit

$$V_{D2} = V_{D1} + 0.05 \quad \text{or} \quad V_{D2} - V_{D1} = 0.05 \text{ V}$$

Now, $$I_2 = I_S e^{V_{D2}/\eta V_T} \quad \therefore \quad 10 - I_1 = I_S e^{V_{D2}/\eta V_T} \quad \text{(iii)}$$

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Also, $I_1 = I_S e^{V_{D1}/\eta V_T} \quad \therefore \quad I_1 = I_S e^{V_{D1}/\eta V_T}$ (iv)

or Dividing Eq. (iii) by Eq. (iv), we get

$$\frac{10 - I_1}{I_1} = e^{(V_{D2} - V_{D1})/\eta V_T}$$

$$= e^{0.05/0.0434782} = 3.158198$$

or $$\frac{10}{I_1} = 3.158198 + 1 = 4.158198$$

or $$I_1 = \frac{10}{4.158198} = 2.40488 \text{ mA}$$

As $I_1 R = 500$ mV

$\therefore$ $$R = \frac{50 \text{ mV}}{2.40488 \text{ mA}} = 20.79 \approx 21\,\Omega$$ **Ans.**

EXAMPLE 2.7

Determine the current I_D and the diode voltage V_D for the circuit shown in Fig. 2.8 with V_{DD} = 5 V and R = 1 kΩ. Assume that the diode has a current of 1 mA at a voltage of 0.7 V, and that its voltage drop changes by 0.1 V for every decade change in current.

Solution: We know that

$$I_D = I_S(e^{V_D/\eta V_T} - 1)$$

For forward biased case,

$$I_D = I_S e^{V_D/\eta V_T}$$

or $$I_D = I_S e^{kV_D}$$

where $$k = \frac{1}{\eta V_T}$$

Let $I_D = I_{D_1}$ for $V_D = V_{D_1}$ and $I_D = I_{D_2}$ for $V_D = V_{D_2}$.

$\therefore$ $$I_{D_1} = I_S e^{kV_{D_1}}$$ (i)

and $$I_{D_2} = I_S e^{kV_{D_2}}$$ (ii)

$$\frac{I_{D_2}}{I_{D_1}} = e^{k(V_{D2} - V_{D1})}$$

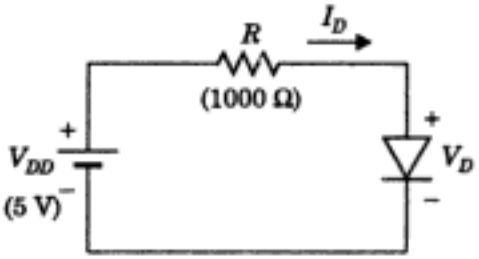


Fig. 2.8 The given circuit for Ex. 2.7.

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Taking log on both sides, we have

$$\log_{10}\frac{I_{D_2}}{I_{D_1}} = k(V_{D2} - V_{D1}) \cdot \log_{10} e$$

$$\therefore \quad V_{D2} - V_{D1} = \left(\frac{2.3}{k}\right)\log_{10}\frac{I_{D_2}}{I_{D_1}} = 2.3\,\eta V_T \log\frac{I_{D_2}}{I_{D_1}} \qquad \text{(iii)}$$

For the given conditions,

$$V_{D2} - V_{D1} = 0.1 \quad \text{and} \quad \frac{I_{D_2}}{I_{D_1}} = \frac{10}{1}$$

Substituting the given values in Eq. (iii), we get

$$0.1 = (2.3\,\eta V_T)\log_{10}\frac{10}{1}$$

$$\therefore \quad \eta V_T = \frac{0.1}{2.3} = \frac{1}{23}$$

Hence $$I_D = I_S e^{V_D(23)}; \quad V_2 - V_1 = 0.1\log_{10}\frac{I_2}{I_1} \qquad \text{(iv)}$$

First iteration

$$I_D = \frac{V_{DD} - V_D}{R}$$

Assume $V_D = 0.7$ V.

$$\therefore \quad I_D = \frac{5 - 0.7}{1000} = 4.3 \times 10^{-3}\ \text{A}$$

Putting $I_{D2} = 4.3$, $I_{D1} = 1.0$, $V_{D1} = 0.7$ in Eq. (iv), we get

$$V_{D2} - 0.7 = 0.1\log_{10}\frac{4.3}{1.0}$$

or $$V_{D2} = 0.7 + 0.1 \times 0.6334 = 0.76334\ \text{V}$$

Thus, the results of the first iteration are $I_D = 4.3$ mA and

$$V_{D2} = 0.7633\ \text{V}. \quad \textbf{Ans.}$$

Second iteration

$$I_{D2} = \frac{5 - 0.7633}{1000} = 4.2367\ \text{mA}$$

Putting $I_{D2} = 4.2367$, $I_{D1} = 1.0$, $V_{D1} = 0.7$ in Eq. (iv), we get

$$V_{D2} - 0.7 = 0.1\log_{10}\frac{4.2367}{1}$$

or $$V_{D2} = 0.7 + 0.1 \times 0.627 = 0.7627\ \text{V}$$

(not much different from 1st iteration)

Thus, $V_D \approx 0.762$ V and $I_D \approx 4.2367$ mA **Ans.**

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2.7 TEMPERATURE DEPENDENCE OF THE V-I CHARACTERISTICS

From the diode equation given by

$$I_D = I_S(e^{V_D/\eta V_T} - 1) \tag{2.6}$$

the parameters I_S and V_T are heavily temperature dependent. V_T is given by

$$V_T = \frac{T}{11{,}600} \tag{2.7a}$$

Equation (2.7) shows that V_T varies linearly with temperature T in kelvin.

I_S is analytically given by

$$I_S = KT^2 e^{-E_{G0}/V_T} \tag{2.7b}$$

where K is a constant and E_{G0} is the energy gap at 0°K

Theoretically, I_S varies about 8% per °C change. Practical diodes slightly deviate from 8% figure since the reverse saturation current (i.e., I_S) has also a component due to surface leakage. *Practical diodes show a change of I_S by about 7% per °C change.* Thus, for 10°C increase of temperature, I_{S_1} increases to I_{S_2} such that

$$I_{S_2} = I_{S_1}(1.07)^{10} = 2I_{S_1} \tag{2.8}$$

Hence, the reverse saturation current doubles for every 10°C rise in temperature or for every 10° kelvin temperature rise.

From the given diode reverse saturation current I_{S_1} at temperature T_1 kelvin we can compute the revised reverse saturation current I_{S_2} at temperature T_2 kelvin, remembering that every 10°C rise (or 10° kelvin rise) doubles the reverse saturation current.

$$I_{S_2} = I_{S_1} \cdot 2^{(T_2 - T_1)/10} \tag{2.9}$$

where I_{S_1} = Reverse saturation current at temperature T_1

I_{S_2} = Reverse saturation current at temperature T_2

Besides I_S and V_T, there is one more parameter viz. the diode voltage V_D which has to be changed to maintain constant I_D when temperature T changes.

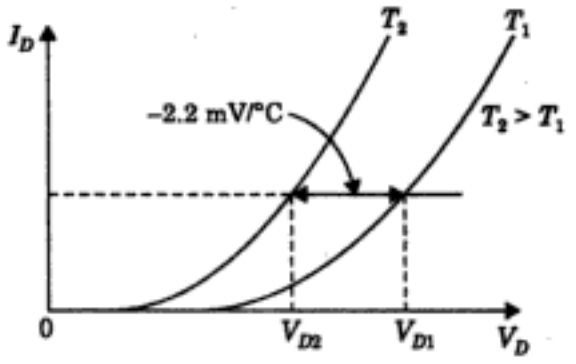


Fig. 2.9a *V-I* curves of a diode at temperature T_1 and T_2 ($T_2 > T_1$).

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If we wish to have no change in the diode current inspite of temperature increase, we must decrease the diode voltage from V_{D1} to a lower value V_{D2} as can be seen from Fig. 2.9a, b.. This is often desirable so that the diode continues passing a safe current inspite of temperature rise.

Theoretically,

$$\frac{dV_D}{dT} = -2.2 \text{ mV/°C} \qquad \text{for } I_D \text{ constant} \tag{2.10}$$

Thus, with temperature increase, we require a lower value of voltage V_D to keep diode current constant. If a diode is already passing a maximum safe current, and the temperature goes up, we must decrease the diode voltage V_D so that the diode current does not exceed its safe value.

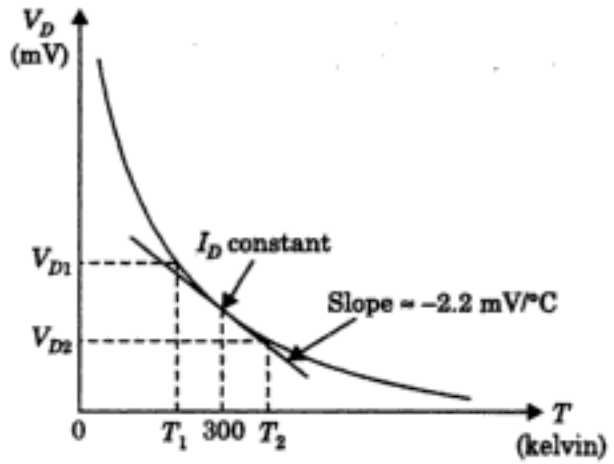


Fig. 2.9b A typical graph showing the variation of diode voltage V_D with temperature T.

2.8 THE DIODE AS A CIRCUIT ELEMENT

An ideal diode is a two-terminal device. The symbol of an ideal diode is shown in Fig. 2.10(a) and volt-ampere characteristics is illustrated in Fig. 2.10(b).

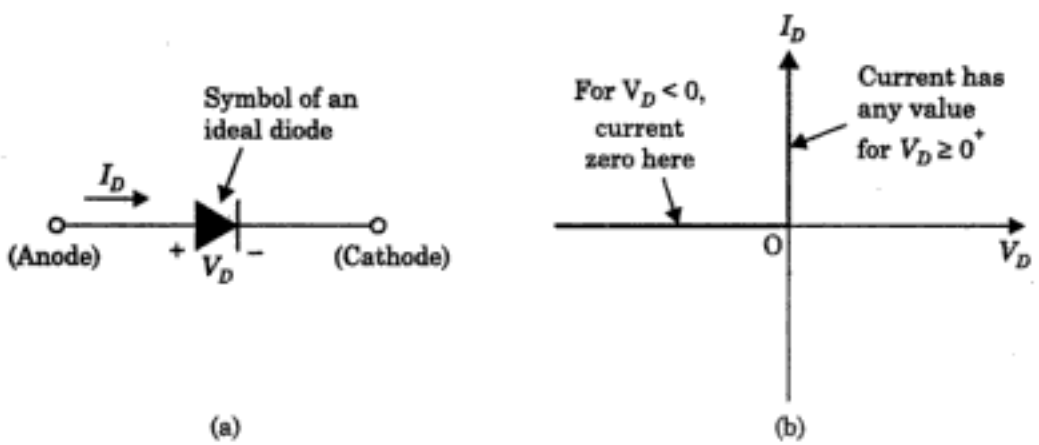


Fig. 2.10 (a) Circuit symbol for an ideal diode with forward current I_D
(b) Volt-Ampere characteristic of an ideal diode.

Thus, an ideal diode is a unilateral circuit element. This unilateral behaviour is important in switching operations. Note that for the ideal diode,

(i) When V_D is zero, I_D can have any +ve value. (ON)
(ii) When I_D is zero, V_D can have any –ve value. (OFF)

In practice, the real diodes have a small non-zero, reverse current and also a voltage drop exists for forward bias (i.e., $V_D \neq 0$). The $V_D - I_D$ curve is, in practice, nonlinear (and

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not a straight line) for non-ideal diodes, as shown in Fig. 2.10(b). However, if we consider a small portion of the $V_D - I_D$ characteristic, this may be almost linear. We shall use this concept and it will be clear in subsequent section on small signal model of the diode.

2.9 THE LOAD-LINE CONCEPT

Consider a diode D fed from a DC voltage source V_{AA} in series with resistance R, as shown in Fig. 2.11(a).

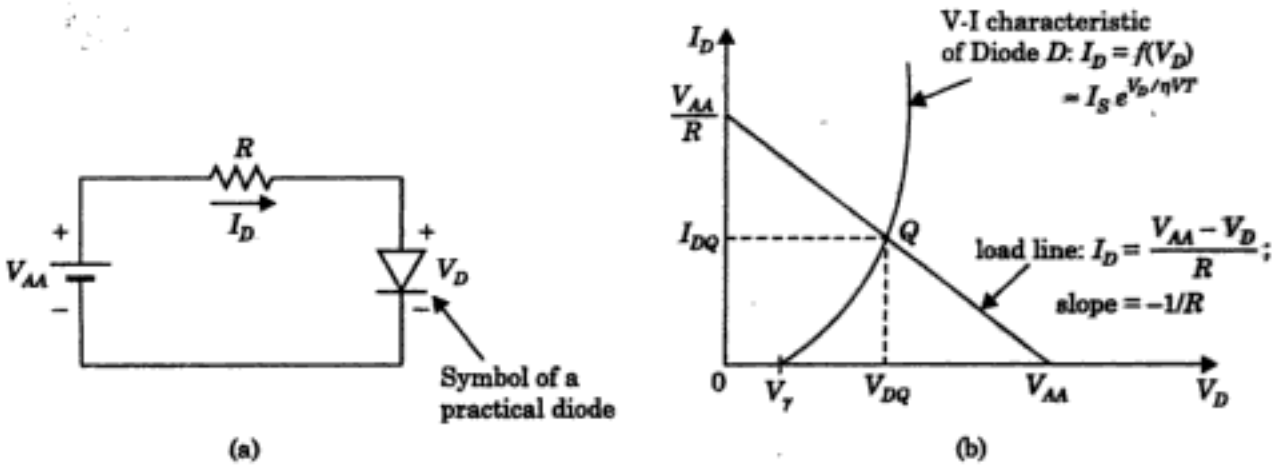


Fig. 2.11 (a) Diode circuit driven by an external voltage source V_{AA} in series with resistance R. (b) Diode characteristic and load line for the circuit of (a).

Applying Kirchhoff's voltage law (KVL) to the circuit depicted in Fig. 2.11(a), we get

$$V_{AA} = I_D R + V_D \tag{2.11}$$

or

$$I_D = -\frac{1}{R} V_D + \frac{V_{AA}}{R} = \frac{V_{AA} - V_D}{R} \tag{2.12}$$

Equation (2.12) is a straight line called the **load line**. Slope of this load line is obtained by comparing Eq. (2.12) with the general equation of a straight line with slope m

$$y = mx + c$$

Here "x" is V_D and "y" is I_D.

Therefore,

$$m = -\frac{1}{R}$$

i.e., slope of the load line is $-1/R$

When $I_D = 0, \quad V_D = V_{AA}$ (2.12a)

When $V_D = 0, \quad I_D = V_{AA}/R$ (2.12b)

The load line joins the points $(V_{AA}, 0)$ and $(0, V_{AA}/R)$ as shown in Fig. (2.11b). The point of intersection of load line with the diode V-I characteristic is called **Q point**. Point Q is also called the **quiescent point** or the **operating point**. Such a concept of obtaining the operating point holds good for any device, and not necessary for the diodes.

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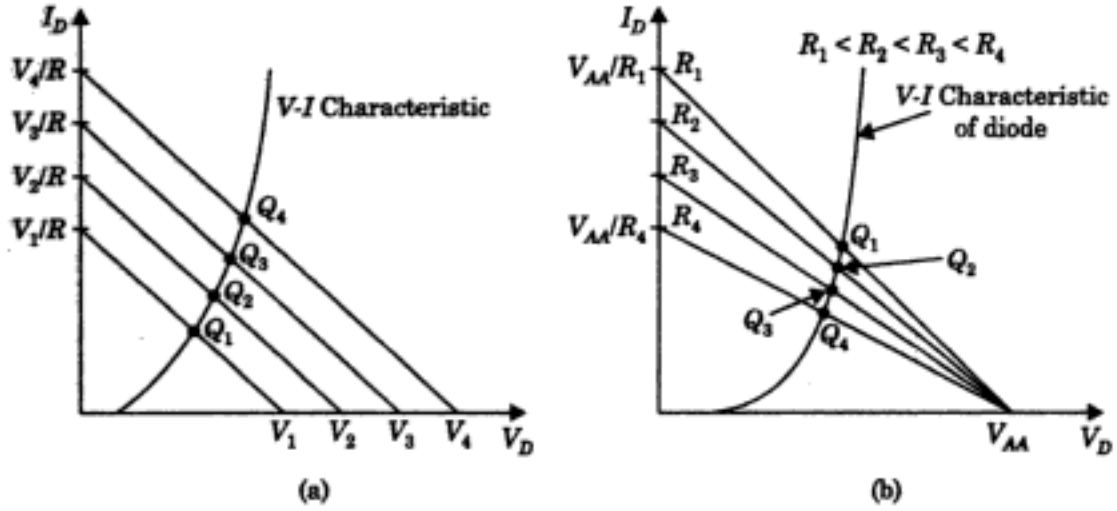


Fig. 2.12 Shifts in operating point for the cases when: (a) V_{AA} varies from V_1 to V_4 (keeping R constant) (b) R varies from R_1 to R_4 (keeping V_{AA} constant).

The load line passes through the points $(V_{AA}, 0)$, $(0, V_{AA}/R)$, and these points are independent of the device characteristics. If we vary V_{AA} from V_1, to V_2, V_3, V_4 keeping R constant, we get a set of load lines shown in Fig. 2.12(a). If we change R from R_1, to R_2, R_3, R_4 keeping V_{AA} constant, we obtain load lines shown in Fig. 2.12(b).

Note that *for small changes in* V_D, say, from V_1 to V_2, the Q-point changes from Q_1 to Q_2. *The device characteristic between* Q_1 *and* Q_2 *may be assumed approximately a straight line.* However, for large changes in V_D, say, from V_1 to V_4, the diode characteristic between Q_1 and Q_4 is nonlinear. We shall, while dealing with small signals (v_d) across the diode, assume that the operating point moves along a small part of the *V-I* characteristic assumed to be almost straight. This will ensure that the slope of the small part of *V-I* characteristic where the point Q moves (due to variation of small signal v_d) is constant. Note that slope of *V-I* characteristic at any point is 1/resistance.

We shall now learn about large signal (or DC) model and the small signal (or AC) model of the diode.

2.10 LARGE SIGNAL DIODE MODELS (DC MODELS)

We have two cases of large signals applied across the diode, viz. the forward-biased diodes and the reverse-biased diodes.

2.10.1 Forward-Biased Diode (ON State)

Figure 2.13(a) is the actual circuit such that V_D is greater than V_γ. (We have used V_γ here instead of the voltage barrier V_0 described earlier. However, the notation V_γ and V_0 carry the same meaning). If V_D is greater than V_γ (the cut-in voltage) then the diode is said to be forward biased. The diode *V-I* characteristic shows that the current I_D is very very small for $V_D < V_\gamma$. We assume this current as zero [see *OA* in Fig. 2.13(b)]. As V_D exceeds V_γ, the practical diode gives current $I_S e^{V_D/\eta V_T}$, i.e., an exponential curve, shown in Fig. 2.13(b). For large signal, forward-biased diode we approximate the exponential curve beyond V_γ by a straight line (see *AB*) as shown in Fig. 2.13(b).

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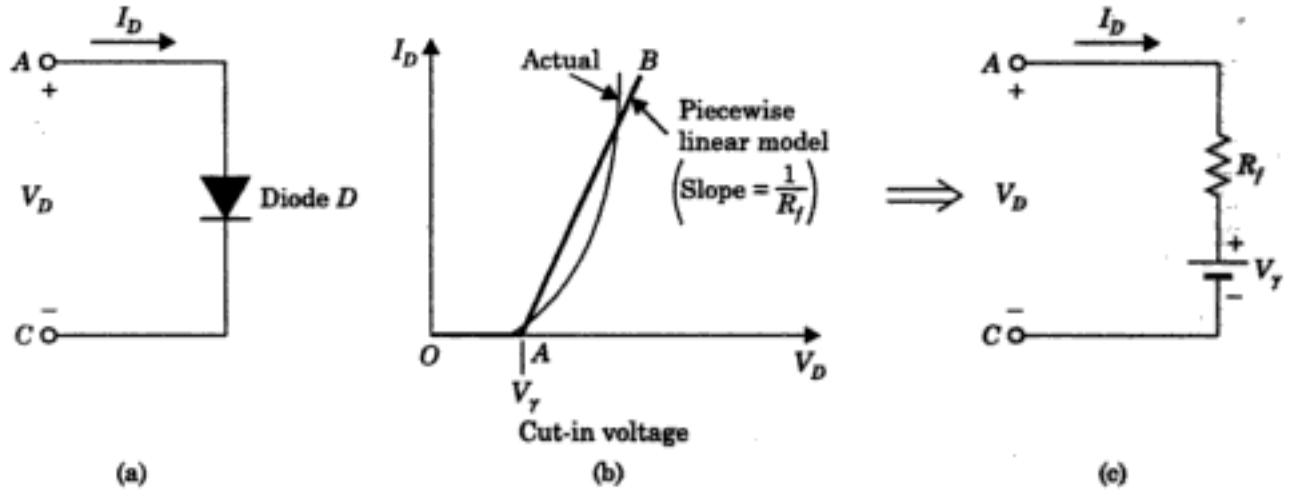


Fig. 2.13 (a) The actual and the piece-wise linear characteristic for forward-bias (b) Diode model for forward bias and (c) The actual circuit for forward-biased diode D.

The equivalent circuit which results by replacing the actual exponential V-I characteristic of the diode by a piece-wise linear model (comprising OA for $I_D = 0$ upto V_γ and a slant straight line AB when V_D exceeds V_γ, is shown in Fig. 2.13(c). The forward resistance R_f is the 1/slope of slant straight line AB in Fig. 2.13(b). It is also assumed that V_D exceeds V_γ and hence the current I_D flows in the forward direction. For Silicon diodes V_γ is approximately 0.6 V and for Germanium diodes it is approximately 0.2 V. The forward resistance R_f varies in the range from 5 to 50 ohms (i.e., it is quite low). The above mentioned model is also called the **DC Model.**

2.10.2 Reverse-Biased Diode (OFF State)

For the reverse-biased diode shown in Fig. (2.14a), and its actual V-I characteristic shown in Fig. 2.14(b), the diode current is very small and almost constant at I_S. The piece-wise linear characteristic for the reverse-biased diode is shown in Fig. 2.14(b) by OB, representing

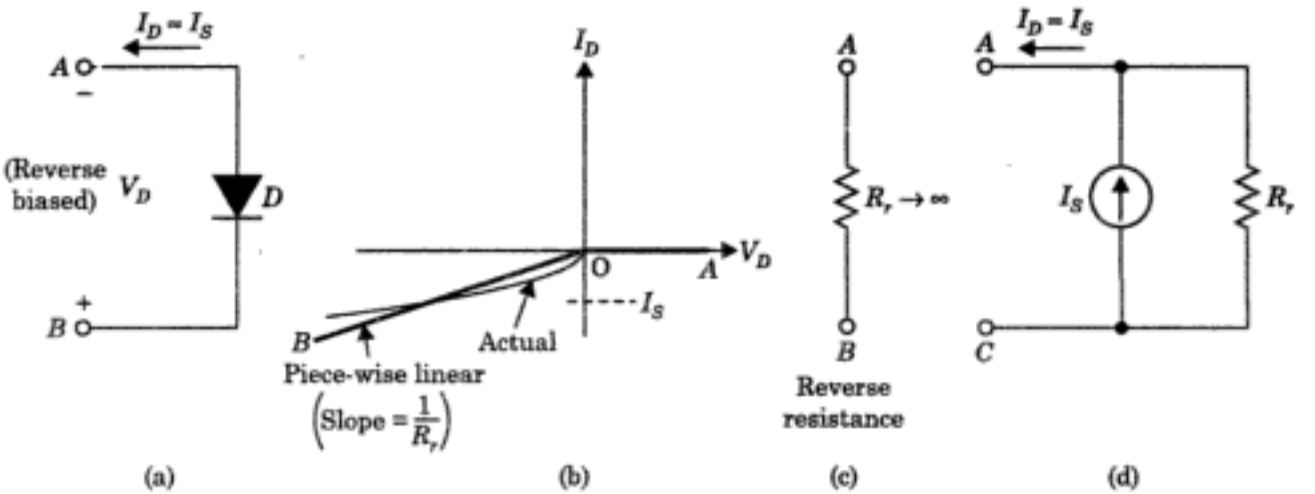


Fig. 2.14 (a) Circuit for reverse-biased diode D (Note the direction of the diode current I_D), (b) Actual and piece-wise linear characteristic for the reverse-biased diode, (c) Diode model, as a circuit element, based on piece-wise linear representation of the characteristic, (d) A more accurate model to include surface leakage.

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a slant line passing through the origin, with slope very close to zero but not actually zero. Such a piece-wise linear characteristic facilitates us to equate the operation of the diode to a very very high reverse resistance R_r, (R_r tends to infinity), as shown in Fig. 2.14(c). A more accurate circuit model, for accurate designs is exhibited in Fig. 2.14(d). This model takes into account the increase in the reverse current with the increase of reverse voltage. Such an increase is due to surface leakage. R_r is generally several hundred kilo ohms or more, and we often assume it as infinity for calculation purposes.

EXAMPLE 2.8

For the circuit shown in Fig. 2.15, find out the output voltage v_0 for the cases

(a) $V_1 = V_2 = 5$ V, (b) $V_1 = 5$ V, $V_2 = 0$ V, (c) $V_1 = V_2 = 0$ V

For the Silicon diodes D_1 and D_2 used in the circuit assume $V_\gamma = 0.6$ V, $R_f \approx 0$, $R_r \to \infty$ and reverse saturation current $I_S = 0$ for reverse-bias diodes.

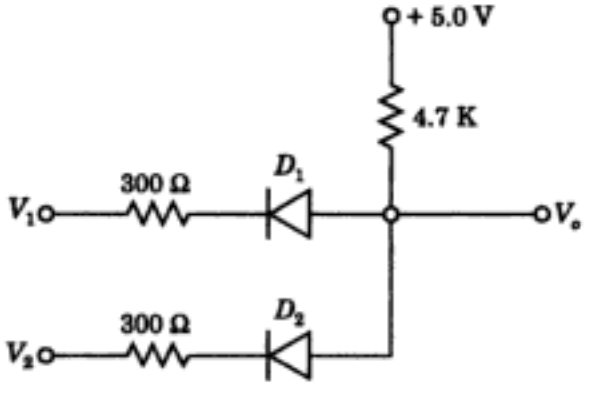


Fig 2.15 The circuit for Ex. 2.8.

Solution: Figure 2.16(a) is the circuit redrawn with voltages V_1 and V_2 shown with reference to earth.

(a) If $V_1 = V_2 = 5$ V, the diodes D_1 and D_2 are both OFF since for a diode to conduct the anode potential must be higher than the cathode potential at least by V_γ (here 0.6 V). As D_1, D_2 are non-conducting these are replaced by open circuits (since $R_r = \infty$, given) as shown in Fig. 2.16(b). As no loop is complete, no current flow, therefore, $V_o = 5.0$ V.

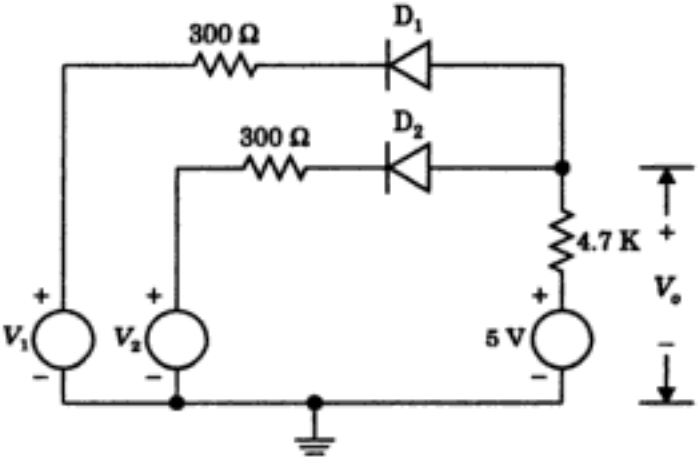


Fig. 2.16(a) Given circuit redrawn with a reference to earth.

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(b) $V_1 = 5$ V, $V_2 = 0$ V, and the circuit reduces to Fig. 2.16(c), D_1 is OFF here as potential difference between the anode and cathode of D_1 (i.e., V_{D1}) is less than 0.6 V. D_2 should be ON here and its equivalence is 0.6 V in series with R_f (R_f being zero here).

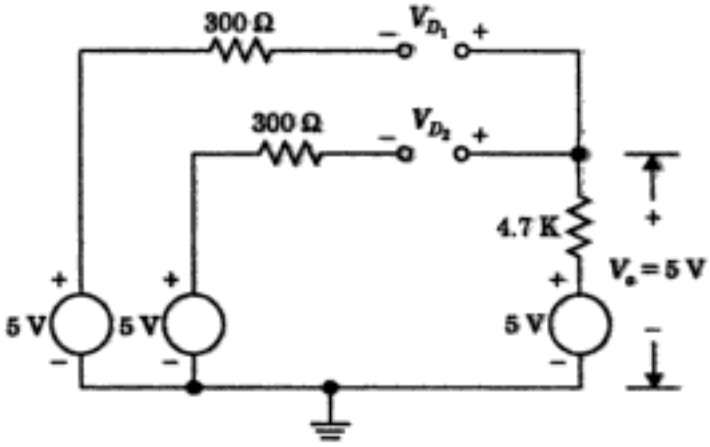


Fig. 2.16(b) Figure 2.16(a) redrawn for D_1 and D_2 OFF ($R_r \to \infty$).

Now, $$I_{D2} = \frac{(5 - 0.6)}{(4.7 \times 10^3 + 300)}$$

$$= \frac{4.4 \times 10^{-3}}{5} = 0.88 \text{ mA}$$

and $$V_o = 5 - I_{D2} \times 4.7$$

$$= 5 - 0.88 \times 10^{-3} \times 4.7 \times 10^3 = 0.864 \text{ V}$$

Note that $V_{D1} = V_o - 5 \text{ V} = 0.864 - 5 = -4.136$ V

So D_2 is indeed OFF.

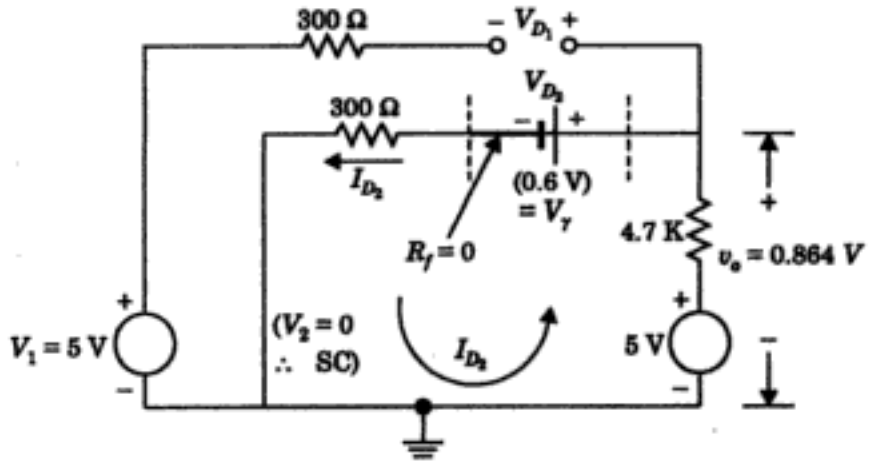


Fig. 2.16(c) The equivalent circuit for $V_1 = +5$ V, $V_2 = 0$.

(c) $v_1 = v_2 = 0$ V, and the circuit reduces to Fig. 2.16(d).

Here, both the diodes are forward biased, therefore, both D_1 and D_2 are ON. $I_{D1} = I_{D2} = I$, say, (due to symmetry). By applying KVL for the diode D_2,

$5 - 2I \times 4.7 - 0.6 - I \times 0.3 = 0$.

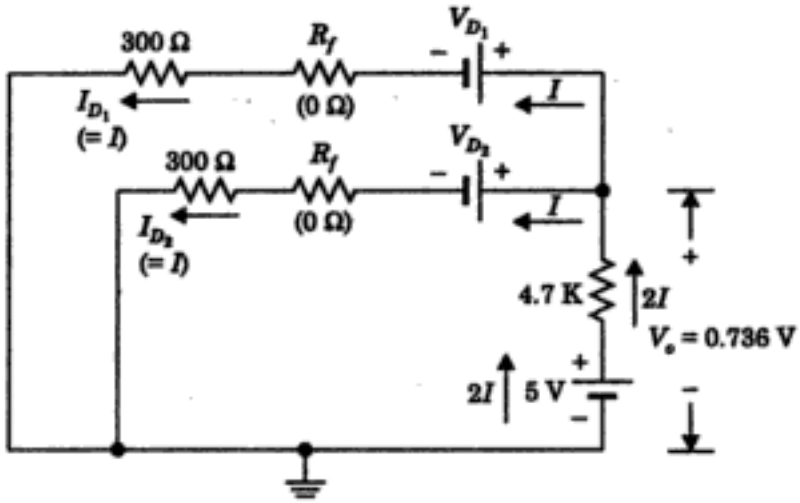


Fig. 2.16(d) The equivalent circuit for $V_1 = V_2 = 0$.

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$\therefore$ $$I = \frac{4.4}{9.7} = 0.454 \text{ mA}$$

and $$V_o = 5 - (2I)(4.7)$$
$$= 5 - (2 \times 0.454)(4.7) = 0.736 \text{ V}$$

To summarize

V_1	V_2	Output V_o
5 V	5 V	5 V
5 V	0 V	0.864 V
0 V	5 V	0.864 V
0 V	0 V	0.736 V

If we assign logic symbol '1' to voltage ≥ 3.5 V and '0' to voltage < 3.5 V. This is a typical AND gate operation.

EXAMPLE 2.9

Determine the output voltage V_o and the diode currents I_{D1}, I_{D2}, shown in Fig. 2.17, for (i) $V_I = 0$ (ii) $V_I = 4$ V. Assume $V_\gamma = 0.7$ V.

Solution: Let $V_I = 0$. Assume that D_1 is OFF. If V_A turns out to be +ve then we are right and D_1 would be indeed OFF.

If D_1 is OFF then

$$I_{R1} = I_{D2} = I_{R2} = \frac{+5 - V_\gamma - (-5\,V)}{R_1 + R_2}$$

$$= \frac{5 - 0.7 + 5}{5 + 10} = 0.62 \text{ mA}$$

$\therefore$ $V_o = 5 - 0.62 \times 5 = 1.9$ V

and $V_A = V_o - 0.7 = 1.9 - 0.7 = 1.2$ V

D_1 is indeed OFF for $V_1 = 0$ volt and we were right.

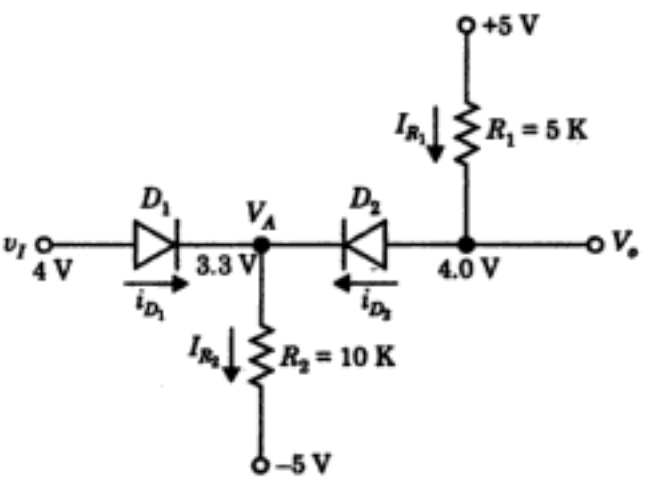


Fig. 2.17 Circuit for Ex. 2.9.

(ii) $V_I = 4$ V. It appears that here both D_1 and D_2 are ON. If I_{D1} and I_{D2} are +ve we are right. If D_1 and D_2 are both ON then for $V_I = 4$ V, $V_A = 4 - 0.7 = 3.3$ V, and $V_0 = V_A + 0.7 = 3.3 + 0.7 = 4.0$ V. When D_1 and D_2 are ON the values of V_A and V_o are shown in Fig. 2.17.

$$I_{R1} = I_{D2} = \frac{5 - V_o}{5} = \frac{5 - 4}{5} = 0.2 \text{ mA}$$

$$I_{R2} = \frac{3.3 - (-5)}{10} = 0.83 \text{ mA}$$

$$I_{D1} = I_{R2} - I_{R1} = 0.83 - 0.2 = 0.63 \text{ mA}$$

As both I_{D1} and I_{D2} are +ve, hence D_1 and D_2 are both ON and $V_o = 4$ V.

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2.11 SMALL SIGNAL DIODE MODEL (AC MODEL)

If we use large signals, we obtain ON/OFF behaviour of the diode depending on the condition that such large signals clearly exceed V_γ or are less than V_γ (the cut-in voltage). In such ON/OFF operation of the diode, the "large signals" are usually constant voltages or DC voltages. That is the reason we often call the ON/OFF models as the DC models. We now consider the case when a diode is already ON, due to application of a DC signal (a large signal as a DC voltage), and then we superimpose on this DC signal a small AC signal $v_S(t)$.

Figure 2.18(a) shows a circuit where the DC voltage is V_{AA} which is much higher than the diode's cut-in voltage V_γ. Suppose $v_s(t) = 0$ in Fig. 2.18(a), then the circuit will be similar to the one given in Fig. 2.11(a), where we discussed the load line. If $v_s(t)$ is not zero then we have the net voltage $v(t)$ given by

$$v(t) = V_{AA} + v_s(t) = V_{AA} + V_m \sin \omega t \tag{2.13}$$

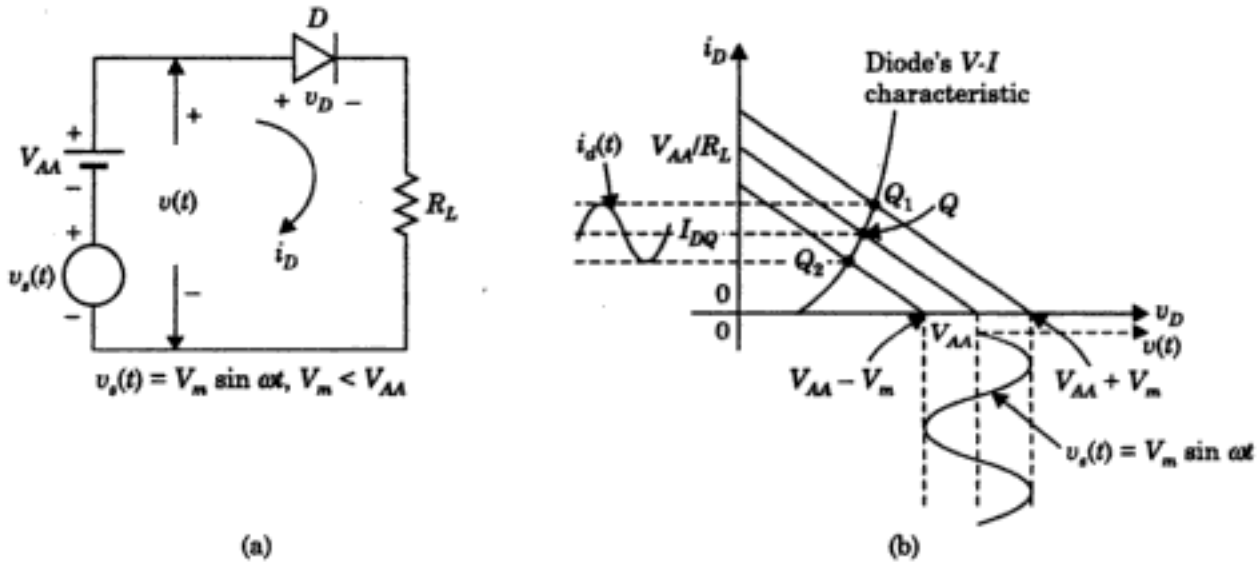


Fig. 2.18 (a) A diode D connected to DC voltage V_{AA} in series with an AC voltage v_s(t) and a load resistance R_L, (b) Load line variations due to $v(t)$ being $V_{AA} + v_s(t)$, assuming $v_s(t) = V_m \sin \omega t$ and $V_m < V_{AA}$.

The extreme values of $v(t)$ are $V_{AA} + V_m$ and $V_{AA} - V_m$. The load line corresponding to $v(t) = V_{AA}$ where point Q has been shown in Fig 2.18(b), with its two points (V_{AA}, 0) and (0, V_{AA}/R_L) if we ignore R_f compared to R_L. This load line cuts the diode's V-I curve at point Q. Such a point which we obtain by assuming AC signal zero is called the **Quiescent point**. This word has been derived from *Quietness*, i.e., situation when there is Quietness or no signal (because the signal is what varies, as $v_s(t)$, DC being constant does not constitute any signal in Communication Theory). As the net value of voltage $v(t)$ varies from V_{AA} to $V_{AA} + V_m$ and then to $V_{AA} - V_m$, the load lines run parallel to the Q-point load line and these two load lines corresponding to $V_{AA} + V_m$ and $V_{AA} - V_m$ intersect the diode V-I characteristic at points Q_1 and Q_2, respectively, as shown in Fig. 2.18(b). If we consider all the possible values of $v(t)$, and not only the extreme values, it is clear that the Q point will move on the diode's V-I characteristic between points Q_1 and Q_2. For small excursion, $V_{AA} - V_m$ to $V_{AA} + V_m$ of

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the voltage $v(t)$, the *V-I* characteristic of the diode between points Q_1 and Q_2 can be considered almost a straight line. Smaller the value of V_m, more accurate is the approximation of part Q_1Q_2 to a straight line. It is this aspect that we get accurate analysis only for very small signals. We do not use the full *V-I* characteristic of the diode because it is highly nonlinear (exponential of the form $I_S e^{V_D/\eta V_T}$) for calculation which becomes quite complex. However, a small linear part Q_1 to Q_2 of the diode characteristic enables us perform simple analysis of the diode performance.

Let the total current flow in the circuit [see Fig. 2.18(a)] be

$$\begin{aligned} i_D &= I_{DQ} + i_d(t) \\ &= I_{DQ} + I_{dm} \sin \omega t \end{aligned} \tag{2.14}$$

where I_{DQ} = DC current if $v(t) = V_{AA}$ and $v_s(t) = 0$

i_d = AC part of i_D that is superimposed due to $v_s(t)$

The value of I_{DQ} found by using the relation:

$$I_{DQ} = \frac{V_{AA} - V_\gamma}{R} \tag{2.15}$$

where $R = R_f + R_L$, (if R_f is not neglected). We obtained such a result in Eq. (2.12) and have simply replaced V_D by V_γ.

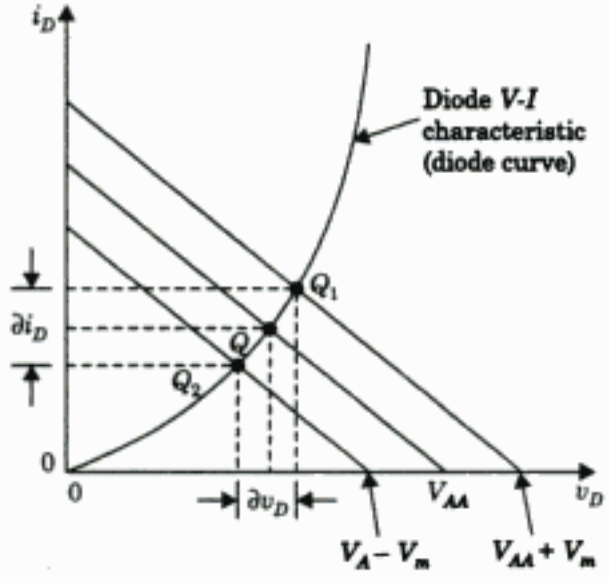


Fig. 2.19(a) Showing the concept of incremental conductance g_d.

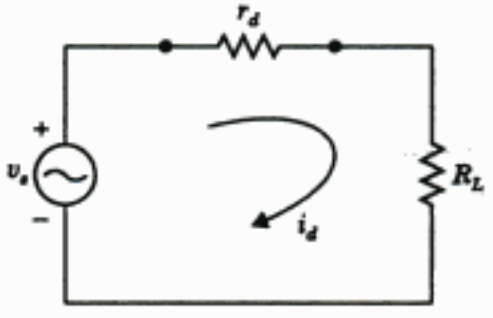


Fig. 2.19(b) AC small signal model.

To find the AC current i_d, we first define some parameters as follows:

Incremental conductance

$$g_d = \left.\frac{\partial i_D}{\partial v_D}\right|_{\text{at } Q \text{ point}} \text{ mho} \tag{2.16}$$

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or
$$g_d = \left.\frac{di_D}{dv_D}\right|_Q \text{ mho} \tag{2.17}$$

Incremental resistance

$$r_d = \frac{1}{g_d} = \left.\frac{dv_D}{di_D}\right|_Q \text{ ohm} \tag{2.18}$$

Around the Q-point (i.e., between Q_1 and Q_2), the V-I characteristic curve is assumed to be a straight line. The values ∂v_D and ∂i_D are shown in Fig. 2.19(a). If Q_1Q_2 is a straight line then $\partial i_D/\partial v_D$ is the slope of the Diode's V-I characteristic at point Q. Hence g_d equals the slope of $i_D - v_D$ curve at the quiescent point Q. Also, note that the slope (and, therefore, 1/slope) is not constant along the entire length of the $i_D - v_D$ curve. Hence we call g_d as the dynamic conductance and $1/g_d$, i.e., r_d, dynamic resistance. It is dynamic in the sense that it varies (dynamics means movement, variation in position) depending upon the location of the Q-point. We can choose the desired Q-point by applying voltage V_{AA} [$v_s(t)$ being zero here] by the DC model. Then we determine the dynamic resistance r_d at the Q-point. The diode offers resistance r_d to the AC signal. Thus, the AC model of the diode can be shown in Fig. 2.19(b).

2.11.1 Determination of r_d (or g_d) at the Q-point

It is desirable that we first understand the notations used in the derivation.

I_D or V_D indicate DC values of diode current and diode voltage.

i_d or v_d indicate AC values of diode current and diode voltage.

i_D or v_D indicate (DC + AC) values of diode current and diode voltage.

Let the values of diode current and diode voltage at Q-point be I_{DQ} and V_{DQ}, respectively. As point Q lies on the diode V-I characteristic, therefore,

$$I_{DQ} = I_S(e^{V_{DQ}/\eta V_T} - 1) \approx I_S e^{V_{DQ}/\eta V_T} \tag{2.19}$$

When we move along the diode curve, away from the Q-point, we have the current i_D and voltage v_D being (DC + AC) values

$$\therefore \quad i_D = I_D + i_d = I_S(e^{v_D/\eta V_T} - 1) \tag{2.20}$$

Differentiating both sides of Eq. (2.20) w.r.t. v_D and remembering that I_D is constant (being a DC current), we get

$$g_d = \frac{di_D}{dv_D} = 0 + I_S(e^{v_D/\eta V_T} - 0).\frac{1}{\eta V_T} \quad \text{[see also Eq. (2.17)]} \tag{2.21}$$

or
$$g_d = \frac{1}{\eta V_T} I_S e^{v_D/\eta V_T} \tag{2.22}$$

At Q-point g_d is found by replacing v_D by its Q-point value, i.e., by V_{DQ}. From Eq. (2.22), we get

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$$g_d\big|_{\text{at } Q} = \frac{1}{\eta V_T} I_S e^{V_{DQ}/\eta V_T}$$

$$= \frac{1}{\eta V_T} I_{DQ} \qquad \text{[using Eq. (2.19)]}$$

$$\therefore \qquad r_d = \frac{1}{g_d} = \frac{\eta V_T}{I_{DQ}} \qquad \text{at } Q\text{-point} \tag{2.23}$$

2.11.2 Rule to Analyze a Diode Circuit with DC + AC Input Voltages

Consider a diode circuit shown in Fig. 2.20a. The input signal consists of a DC voltage V_{AA} superimposed with an ac signal $v_s(t)$. We want to find the total current in the diode: We proceed as follows:

1. Draw its DC model by making $v_s = 0$, replacing the diode by R_f in series with cut-in voltage V_γ. Note the polarity of voltage V_γ, [See Fig. 2.20(b)]. Calculate I_{DQ} by the following relation:

$$I_{DQ} = \frac{(V_{AA} - V_\gamma)}{(R_f + R_L)}$$

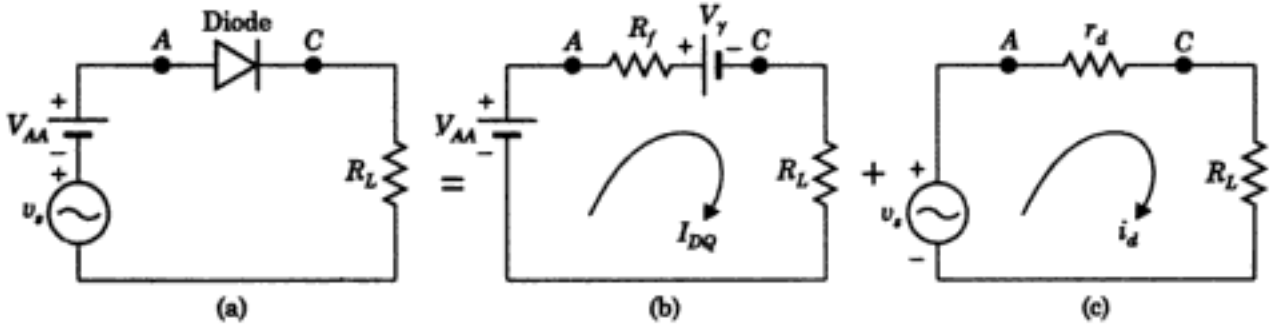


Fig. 2.20 (a) The given diode circuit with input DC + AC voltages, (b) its DC model to find I_{DQ}, (c) its AC model to find i_d.

2. Find r_d at Q-point by using Eq. (2.23), i.e.,

$$r_d\big|_Q = \frac{\eta V_T}{I_{DQ}}$$

3. Draw the AC model by replacing the diode by its dynamic resistance r_d (calculated in Step 2), only taking AC part of the signal, i.e., v_s and ignoring all DC voltages, viz. V_{AA} and V_γ. Then AC current i_d is given by [See Fig. 2.20(c)]

$$i_d = \frac{v_s}{(r_d + R_L)}$$

4. By superposition, the total diode current is given by

$$i_D = I_{DQ} + i_d$$

The voltage output at R_L is given by (i_D . R_L).

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Static Resistance: Besides the dynamic resistance r_d, there is also another parameter called Static Resistance (R_{stat}), and is defined as the ratio of DC voltage and DC current at the Q-point i.e.,

$$R_{stat} = \frac{V_{DQ}}{I_{DQ}} \tag{2.24}$$

EXAMPLE 2.10

The reverse bias saturation current for a P-N junction diode (Silicon type) is 1 μA at 300K. Calculate the dynamic and static resistance at 200 mV forward bias at 300K.

Solution Here $I_S = 1 \times 10^{-6}$ A, $\eta = 2$ (Silicon diode) $T = 300$K

For a diode, $i_D = I_S(e^{v_D/\eta V_T} - 1)$

At $T = 300$K, taking $V_T = 25$ mV, we get

$$i_D = 1 \times 10^{-6}(e^{200/2\times 25} - 1)$$
$$= 1 \times 10^{-6}(e^4 - 1)$$
$$= 10^{-6}(54.598 - 1)$$

or $I_{DQ} = i_D|_{T=300\,K} = 53.598 \times 10^{-6}$ A

Dynamic resistance is given by

$$r_d = \frac{dv_D}{di_D} = \frac{\eta V_T}{I_{DQ}}$$

or $$r_d = \frac{\eta V_T}{I_{DQ}} = \frac{2 \times 25 \times 10^{-3}}{53.598 \times 10^{-6}} = 0.9328\ \text{k}\Omega \quad \textbf{Ans.}$$

Now, Static resistance, $R_{stat} = \frac{v_D}{I_{DQ}}$

$$= \frac{0.2}{53.598 \times 10^{-6}} = 3.731\ \text{k}\Omega \quad \textbf{Ans.}$$

EXAMPLE 2.11

The circuit shown in Fig. 2.21(a) is used at 20°C with $V_{AA} = 9$ V, Given, $V_m = 0.2$ V and $R_L = 2$ kΩ. $V_\gamma = 0.6$ V, $R_f = 10$ Ω and $\eta = 2$. Determine:

(a) the alternating component of the voltage across R_L.

(b) the total voltage across R_L.

(c) the total current

Solution First draw DC and AC models as shown in Figs. 2.21(b) and (c). From the DC model shown in Fig. 2.21(b), we determine the bias levels (i.e., quiescent current)

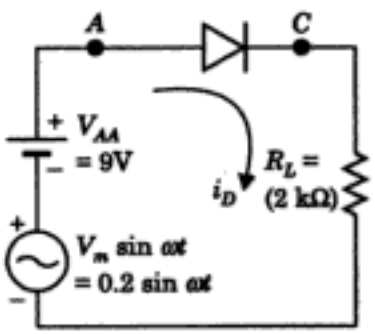


Fig. 2.21(a) Circuit for Ex. 2.11.

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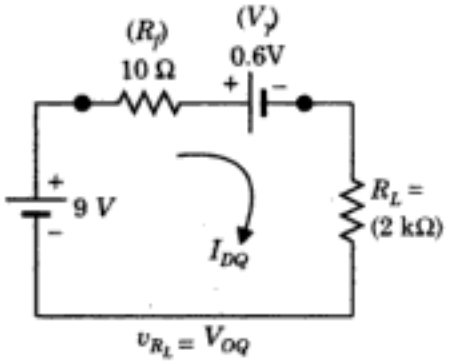


Fig. 2.21(b) DC model.

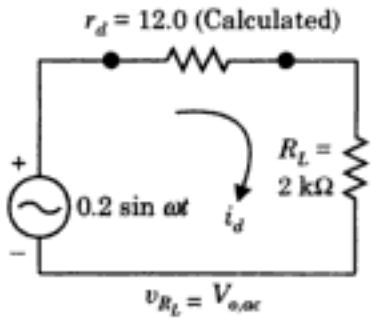


Figure 2.21(c) Incremental model (AC model).

(a) $$I_{DQ} = \frac{9 - 0.6}{R_L + R_f}$$

$$= \frac{8.4}{2000 + 10} = \frac{8.4}{2010} = 4.18 \text{ mA}$$

The dynamic resistance r_d is given by

$$r_d = \frac{\eta V_T}{I_{DQ}}$$

$$= \frac{2 \times 25 \text{ mV}}{4.18 \text{ mA}} = 11.96, \text{ say, } 12.0 \ \Omega$$

We use this value of r_d in the AC model (incremental model) shown in Fig. 2.21(c).

Clearly, $$V_{DQ} = I_{DQ} R_L$$ (from DC model)

$$= (4.18) \times (2) = 8.36 \text{ V}$$

and $$i_d = \frac{v_s}{(R_L + r_d)}$$

$$= 0.2 \frac{\sin \omega t}{(2000 + 12)} = 0.099 \sin \omega t$$

Now, $$v_{o,ac} = \frac{R_L}{R_L + r_d} (V_m \sin \omega t)$$

$$= \frac{2000}{2000 + 12} \times 0.2 \sin \omega t \text{ V}$$

Therefore, $v_{o,ac} = 0.199 \sin \omega t$ gives the alternating component of voltage across R_L. **Ans.**

(b) $$v_o(t) = V_{DQ} + v_{o,ac}$$

$$= (8.36 + 0.199 \sin \omega t) \text{ V}$$ **Ans.**

(c) The overall current i_D in the load resistance is given by

$$i_D = I_{DQ} + i_d$$

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$$= 4.18 + 0.099 \sin \omega t$$

$$= (4.18 + 0.099 \sin \omega t) \text{ mA}$$

EXAMPLE 2.12

In the circuit shown in Fig. 2.22(a), I is a DC current and v_s is a sinusoidal signal. Capacitor C is very large; its function is to couple the signal to the diode but block the DC current from flowing into the signal source.

(a) Use the diode small signal model to show that the signal component of the output voltage is:

$$v_o = v_s \frac{\eta V_T}{\eta V_T + IR_S}$$

(b) If v_s = 10 mV, find v_o for I = 1 mA, 0.1 mA and 1 μA. Let R_S = 1 kΩ and η = 2.

(c) At what value of I does v_o become one-half of v_s?

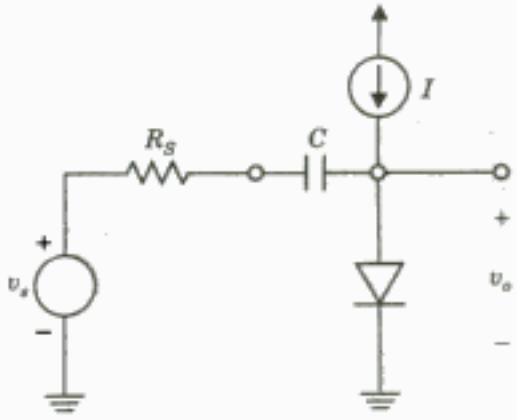


Fig. 2.22(a) Circuit for Ex. 2.12.

Solution (a) The small signal equivalent circuit is shown in Fig. 2.22(b) since C is effectively short-circuit for ac signals. Clearly,

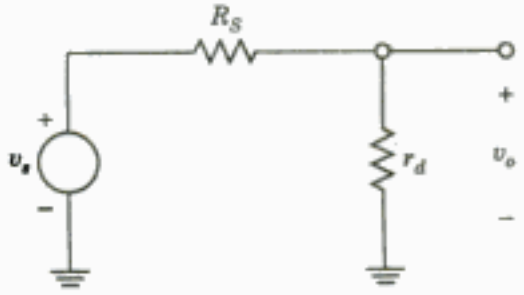


Fig. 2.22(b) AC equivalent circuit.

(a) $$v_o = v_s \cdot \frac{r_d}{R_S + r_d}$$

But $$r_d = \frac{\eta V_T}{I}$$

$\therefore$ $$v_o = v_s \cdot \frac{\eta V_T / I}{R_S + (\eta V_T / I)}$$

or $$v_o = v_s \frac{\eta V_T}{\eta V_T + IR_S}$$

(b) For v_s = 10 mV, I = 1 mA, 0.1 mA, 1 μA and R_S = 1 kΩ,

$$v_o|_{I=1\text{mA}} = (10 \times 10^{-3}) \frac{2 \times (25 \times 10^{-3})}{2 \times (25 \times 10^{-3}) \times (10^{-3})(10^3)}$$

$$= 10^{-2} \times \frac{50 \times 10^{-3}}{50 \times 10^{-3} + 1} = 0.476 \text{ mV} \quad \textbf{Ans.}$$

$$v_o|_{I=0.1\text{mA}} = 10^{-2} \times \frac{50 \times 10^{-3}}{50 \times 10^{-3} + 0.1} = 3.33 \text{ mV} \quad \textbf{Ans.} \quad (\because IR_S = 0.1)$$

$$v_o|_{I=1\mu\text{A}} = 10^{-2} \times \frac{50 \times 10^{-3}}{50 \times 10^{-3} + 10^{-3}} = 9.803 \text{ mV} \quad \textbf{Ans.} \quad (\because IR_S = 10^{-3})$$

(c) For $v_o = v_s/2$, we have

$$\frac{v_s}{2} = (v_s)\frac{2\times25\times10^{-3}}{2\times25\times10^{-3} + IR_S}$$

$$\therefore \quad \frac{1}{2}(50\times10^{-3} + IR_S) = 2\times25\times10^{-3}$$

or $$IR_S = 10^{-1} - 50\times10^{-3} = 10^{-3}(100 - 50) = 50\times10^{-3}$$

or $$I = \frac{50\times10^{-3}}{R_S} = \frac{50\times10^{-3}}{10^3}$$

$$= 50\times10^{-6}\ \text{A}$$

or $$I = 50\ \mu\text{A}$$ **Ans.**

Note that this circuit functions as a signal alternator with the attenuation factor controlled by the value of the DC current I.

2.12 CAPACITANCES IN A DIODE

There are two types of capacitances associated with a *pn*-junction diode. These capacitances must be added in the small signal model of a diode when it is used as a circuit element especially at high frequencies.

When a diode is forward-biased, the charge storage in the diode (outside depletion region) causes a diffusion capacitance, C_D. The small signal model of the diode is, therefore, modified by taking the diffusion capacitance C_D across the dynamic resistance, r_d as shown in Fig. 2.23.

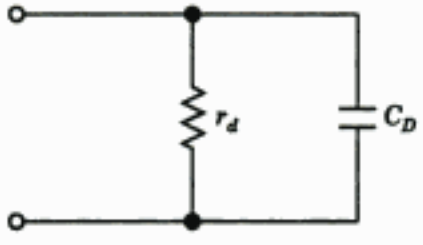


Fig. 2.23 Small signal models of diode for high frequencies with forward bias.

Under reverse-biased conditions, the space charge in the depletion region increases with an increase in reverse voltage. The capacitive effect is called transition capacitances or depletion capacitance, C_T. The small signal model of the diode under reverse-biased condition; is therefore, modified by placing C_T in parallel to reverse incremental resistance, r_r as shown in Fig. 2.24.

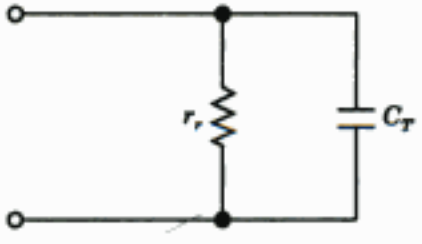


Fig. 2.24 Reverse-biased small signal diode model.

In fact, both the depletion and diffusion capacitances exist for forward as well as for reverse bias cases in diodes. Under forward-biased conditions, the value of C_T (the depletion capacitance) is small as compared to C_D (the diffusion capacitance) and, therefore, C_T may be neglected. Similarly, for reverse-biased case, C_D is small as compared to C_T and may be neglected. However, in computer aided design problems, both C_T and C_D are usually taken into account.

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2.12.1 Transition Capacitances (C_T)

We have earlier seen that when a diode is reverse-biased, majority carriers move away from the junction, thereby increasing the width of the depletion region where space charge exists. This increase in the mobile charges within the depletion region with increase in voltage can be viewed as a capacitive effect. This incremental capacitance C_T is called transition capacitance or depletion capacitance and is given by

$$C_T = \left| \frac{dQ}{dV} \right| \tag{2.25}$$

where dQ is the increase in charge due to an increase dV in reverse voltage. As the +ve ions exists on the n side and –ve ions on the p side, the junction behaves as a parallel plate capacitor and its value is given by

$$C_T = \frac{\varepsilon A}{W} \tag{2.26}$$

We shall derive the value of C_T for a step graded junction.

Step graded junction: For a step graded junction, there is an abrupt change, say, from acceptor ions on one side to donor ions on the other side of the junction. This type of junction is formed by placing a trivalent impurity (such as Indium) against n-type Ge and heating the combination for a short time. Some of the Indium atoms dissolve into the n-type Ge and converts it into p-type Ge. This type of step graded junction is called as alloy or fusion junction. Such a junction is usually formed between the emitter and the base of a planar transistor.

Figure 2.25(a) shows a step graded junction reverse-biased by applying an external voltage V_D. The charge density, ρ_v variation is shown in Fig. 2.25(b) where $N_A >> N_D$. It is not necessary that the concentration N_A and N_D be equal. In fact, it is often advantageous to have an asymmetrical (N_A, N_D wise) junction particularly in FETs. In this analysis, by assuming $N_A >> N_D$, the depletion width on the p-side can be neglected and this simplifies the analysis.

Assuming $N_A >> N_D$, we have the following:

$$N_A W_p = N_D W_n \tag{2.27}$$

because the net charge must be zero [i.e., W_p and W_n get so formed automatically when a junction is made, to satisfy Eq. (2.27)]. As $N_A >> N_D$, therefore,

$$W_p << W_n$$

$$\therefore \quad \text{Total width } W = W_p + W_n \approx W_n \tag{2.28}$$

We shall now determine the value of W for the step-graded junction diode.

As per the Poisson's relation, we have

$$\frac{d^2V}{dx^2} = -\frac{\rho_v}{\varepsilon} \tag{2.29}$$

Here ρ_v is the charge density (in coulombs/m^3) and is given by

$$\rho_v = qN_D \qquad \text{(on } n \text{ side)}$$

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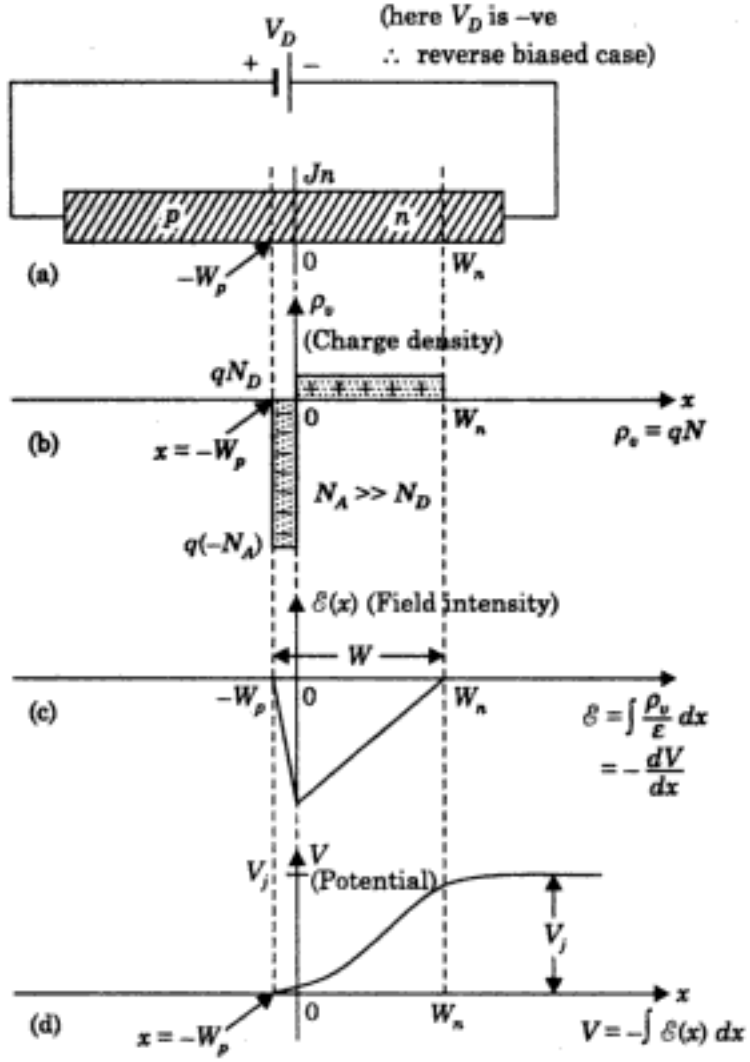


Fig. 2.25 (a) A reverse-biased step-graded *p-n* junction with $N_A >> N_D$, (b) The charge density ρ_v in the depletion regions ($-W_p$ to 0 and 0 to W_n), (c) Field intensity $\mathcal{E}(x)$ due to ρ_v, (d) Potential V.

Putting this value of ρ_v in Eq. (2.29), we get

$$\frac{d^2V}{dx^2} = -\frac{qN_D}{\varepsilon} \tag{2.30}$$

The electric lines of flux start on the +ve donor ions and terminate on the –ve acceptor ions. Hence there are no flux lines on RHS of the boundary $x = W_n$. In other words the electric field intensity $\mathcal{E}(x)$ is zero outside the depletion region, as shown in Fig. 2.25(c).

Integrating Eq. (2.30) w.r.t. x on both sides, we get

$$\mathcal{E}(x) = -\frac{dV}{dx} = \int \frac{qN_D}{\varepsilon} dx + K_1 \text{ (constant)}$$

$$= \frac{qN_D}{\varepsilon} x + K_1 \tag{2.31}$$

The constant K_1 in Eq. (2.31) is found by applying the following boundary conditions.

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$$\mathscr{E}(x) = 0 \quad \text{at} \quad x = W_n \qquad (\because \text{ no lines on RHS of } x = W_n)$$

$$\therefore \qquad 0 = \frac{qN_D}{\varepsilon} W_n + K_1$$

which gives $$K_1 = -\frac{qN_D}{\varepsilon} W_n$$

Thus, we get from Eq. (2.31) after putting $K_1 = (-qN_D/\varepsilon)W_n$ and assuming $W_n = W$,

$$\mathscr{E}(x) = -\frac{dV}{dx} = \frac{qN_D}{\varepsilon}(x - W) \tag{2.32}$$

Integrating Eq. (2.32) again w.r.t. x gives us

$$V = -\int \frac{qN_D}{\varepsilon}(x - W)\,dx$$

$$= -\frac{qN_D}{\varepsilon}\left(\frac{x^2}{2} - W.x\right) + K_2 \text{ (constant)} \tag{2.33}$$

The variation of the barrier potential V for the holes crossing from p to n is shown in Fig. 2.25(d).

We assume that $V = 0$ at $x = 0$. To be more rigorous V should be taken zero at $x = -W_p$. However, $W_p << W_n$ and the point $x = 0$ almost touches the $-W_p$ point.

Putting $V = 0$ at $x = 0$ in Eq. (2.33) gives us $K_2 = 0$. Hence Eq. (2.33) reduces to

$$V = -\frac{qN_D}{\varepsilon}\left(\frac{x^2}{2} - W.x\right) \tag{2.34}$$

The value of V at $x = W$ gives the barrier potential or the junction voltage, which is denoted by symbol V_j. For an open circuited junction diode, V_j has the value V_0 or V_γ which we calculated in Chapter 1 as $V_T \ln(N_A . N_D)/n_i^2$. Externally applied voltage alters the value of reverse bias across the junction, and the total junction reverse voltage V_j, is

$$V_j = V_\gamma - V_D = V_0 - V_D \tag{2.35}$$

Note that for V_D +ve (forward voltage) the net reverse bias across the junction decreases and for V_D –ve (reverse voltage), the net reverse bias across the junction increases.

The value of net junction voltage (reverse) is when $x = W$ in Eq. (2.34). This gives us [putting $x = W$ and calling V as V_j in Eq. (2.34)]

$$V_j = \frac{qN_D W^2}{2\varepsilon} \tag{2.36}$$

In other words, the depletion width W is proportional to square root of total junction voltage V_j (i.e. $W \propto \sqrt{V_j}$). Thus, the depletion width increases with higher (reverse) junction voltage V_j.

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2.12.2 Calculation of Transition Capacitance C_T (for step graded junction diode)

Depletion/transition capacitance given by Eq. (2.25) is

$$C_T = \frac{\varepsilon A}{W} \tag{2.37}$$

where ε = Permittivity of the semiconductor (F/m)
A = Cross-sectional area of the junction (m^2)
W = Depletion region width (m)

From Eq. (2.36) $$W = \left(\frac{2\varepsilon V_j}{qN_D}\right)^{1/2}$$

$\therefore$ $$C_T = \varepsilon A\left(\frac{qN_D}{2\varepsilon V_j}\right)^{1/2}$$

or $$C_T = A\left(\frac{q\varepsilon N_D}{2V_j}\right)^{1/2} \tag{2.37a}$$

Replacing V_j by $V_0 - V_D$ [due to Eq. (2.35)], we finally obtain

$$C_T = A\left(\frac{q\varepsilon N_D}{2(V_0 - V_D)}\right)^{1/2} \quad \text{[for step-graded junction diode]} \tag{2.38}$$

which is the same as mentioned earlier in Eq. (2.26). Note that V_D is –ve for reverse-biased diode. From Eq. (2.38), we can write

$$C_T\big|_{V_D=0} = A\left(\frac{q\varepsilon N_D}{2V_0}\right)^{1/2} = C_0 \quad \text{(say)} \tag{2.39}$$

where C_0 denotes transition capacitance of an open circuited junction diode.

$\therefore$ $$C_T = \frac{C_0}{\left(\frac{V_0 - V_D}{V_0}\right)^{1/2}} = C_0\left(1 - \frac{V_D}{V_0}\right)^{-1/2} \tag{2.40}$$

where V_D is +ve for forward bias and –ve for reverse-bias diode. Equation (2.40) shows that C_T varies if the applied diode voltage V_D is varied. This property makes the diode a useful device to obtain a voltage controlled variable capacitance.

EXAMPLE 2.13

Calculate the barrier capacitance of a Germanium *p-n* junction whose area is 1 mm by 1 mm and whose space charge thickness is 2×10^{-4} cm. The dielectric constant of Germanium (relative to free space) is 16.

Solution The depletion region capacitance is given by Eq. (2.25) as

$$C_T = \frac{\varepsilon A}{W}$$

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Solution Let $\rho(x) = qkx, \quad -\frac{W}{2} < x < \frac{W}{2}$ as shown in Fig. 2.27(b).

where q = charge density
k = a +ve constant

By Poisson's equation, therefore,

$$\frac{d^2V}{dx^2} = -\frac{\rho(x)}{\varepsilon} = \frac{-qkx}{\varepsilon}$$

$$\mathcal{E}(x) = -\frac{dV}{dx} = \int \frac{qkx}{\varepsilon}\,dx$$

$$\therefore \quad \frac{dV}{dx} = -\frac{qk}{\varepsilon}\cdot\frac{x^2}{2} + K_1$$

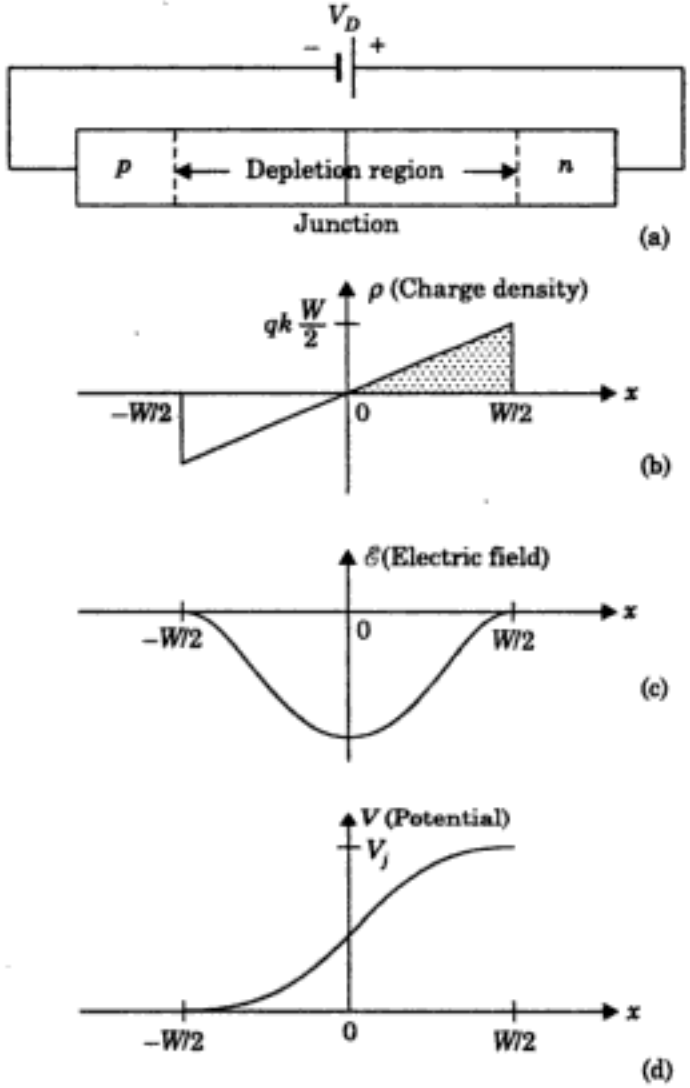


Fig. 2.27 (a) Reverse-biased, linearly graded p-n junction. (b), (c), (d). Variation of ρ, $\mathcal{E}(x)$ and V.

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When $x = \pm W/2$ and $dV/dx = 0$ then

$$K_1 = \frac{qk}{\varepsilon}\frac{W^2}{8}$$

$$\therefore \quad \frac{dV}{dx} = \frac{qk}{8\varepsilon}(-4x^2 + W^2)$$

Integrating again

$$V = \frac{qk}{8\varepsilon}\left[-\frac{4}{3}x^3 + W^2x\right] + K_2$$

At $x = 0$, $V = V_j/2$ (due to symmetry)

$$\therefore \quad V_{j/2} = \frac{qk}{8\varepsilon}\left[-\frac{4}{3}\times 0 + W^2 \times 0\right] + K_2$$

or $$K_2 = \frac{V_j}{2}$$

$$\therefore \quad V = \frac{qk}{8\varepsilon}\left[-\frac{4}{3}x^3 + W^2x\right] + \frac{V_j}{2}$$

At $x = W/2, \quad V = V_j$

$$\therefore \quad V_j = \frac{qk}{8\varepsilon}\left[-\frac{4}{3}\frac{W^3}{8} + W^2\frac{W}{2}\right] + \frac{V_j}{2}$$

or $$\frac{V_j}{2} = \frac{qk}{8\varepsilon}W^3\left(-\frac{1}{6} + \frac{1}{2}\right) = \frac{1}{24\varepsilon}qkW^3$$

$$\therefore \quad V_j = \frac{1}{12\varepsilon}qkW^3 \qquad \text{(i)}$$

With the reverse bias, as shown in Fig. 2.27, the barrier is increased.

$$\therefore \quad V_j = V_0 + V_D$$

where V_0 is the cut-in voltage and V_D the reverse bias

Thus, for a linearly graded junction diode,

$$W \propto V_j^{1/3}$$

To find transition capacitance C_T, we first find total charge contained on one side as

$$Q = \frac{1}{2}\cdot\left(\frac{W}{2}\cdot A\right)qk\frac{W}{2}$$ (Area of triangle dotted × Cross-sectional A in Fig. 2.27(b))

$$= \frac{1}{8}qkW^2A$$

Now, $$C_T = \frac{dQ}{dV}$$

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$$= \frac{dQ}{dW} \cdot \frac{dW}{dV}$$

$$= \frac{\left(\frac{1}{4} qkWA\right)}{\left(\frac{1}{12\varepsilon} \cdot 3qkW^2\right)}$$

$$\left(\text{determining } \frac{dQ}{dW} \text{ and } \frac{dW}{dV} \text{ from } (i) \text{ and } (ii)\right)$$

$$= \frac{1}{4} qkWA \cdot \frac{4\varepsilon}{qkW^2} = \frac{\varepsilon A}{W}$$

(as in the case of step-guided junction)

$$= \frac{\varepsilon A}{\left(\frac{12\varepsilon V_j}{qk}\right)^{1/3}}$$

$$= \varepsilon A \left(\frac{qk}{12\varepsilon}\right)^{1/3} V_j^{-1/3}$$

or $$C_T = \left[\frac{qk\varepsilon^2 A^3}{12}\right]^{1/3} V_j^{-1/3}$$

$$= \tilde{K} V_j^{-1/3}$$

where $$\tilde{K} = \left(\frac{qk\varepsilon^2 A^3}{12}\right)^{1/3}$$ **Ans.**

Or directly $$C_T = \frac{\varepsilon_A}{W} = \varepsilon A \cdot \left(\frac{1}{12\varepsilon V_j} qk\right)^{1/3}$$

$$= \left(\frac{qk\varepsilon^2 A^3}{12}\right)^{1/3} V_j^{-1/3}$$ **Ans.**

Diffusion capacitance (C_D): When the diode is forward biased, and there is no barrier to the movement of majority carriers, the holes diffuse from *p*-side to the *n*-side by crossing the junction. Consequently, in the vicinity of junction, on the *n*-side, we have greater hole concentration than normally exists (during non-conduction). As we move away from the junction, towards the *n*-type side, the amount of such excess holes decreases since the holes recombine with the majority carrier electrons on the *n*-side. Similar is the situation of electrons diffusing across the junction and going towards *p*-side under forward biased junction. Now, if we apply a signal (e.g. $V_m \sin \omega t$) which will increase the forward bias, say, by ΔV (during the time when $V_m \sin \omega t$ is +ve), there would be more diffusion of the majority carriers (when these go across the junction) due to increased forward bias. ***Increased diffusion***

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would cause a change ΔQ in the charge stored near the junction. This phenomenon can be described as a capacitive effect. Thus, the rate of change of injected charge with voltage is called the diffusion or storage capacitance, C_D and is given by

$$\text{Diffusion capacitance } C_D = \frac{\Delta Q}{\Delta V}$$

$$= \left.\frac{\Delta Q}{\Delta V}\right|_{\text{At operating point}} \tag{2.23}$$

In order to derive an expression for diffusion capacitance, we first discuss the minority carrier distribution in a diode as given in the next Section 2.14.

2.13 MINORITY CARRIER CONCENTRATION AND THE LAW OF THE JUNCTION

2.13.1 Forward-Biased Junction

Due to thermal voltage V_T some holes from p-side get injected to n-side and also some electron from n-side get injected to p-side. This makes the hole concentration and electron concentration maintained at values p_{n0} (on n-side) and $n_p(0)$ (on p-side) due to thermal equilibrium. Now, if we apply a forward voltage V_D across the diode additional holes get injected to n-side (from p-side) and similarly additional electrons get injected from n-side to p-side. The additional injected holes make their concentration increased from p_{n0} to $p_n(0)$ at $x = 0$ on n-side. However, these additional holes $p_n(0) - p_{n0}$ decrease as we go towards n-side due to recombination with plenty of majority carriers available on n-side. Similar is the fate of additional electrons $n_p(0) - n_{p0}$ on the p-side. The additional holes and electrons decay in their densities exponentially as shown by the curves $p_n(x)$ and $n_p(x)$ in Fig. 2.28(a). Their exponential decrease is such that they tend to reach the thermal equilibrium values p_{n0} and n_{p0} as $x \to \infty$ and $x \to -\infty$, respectively.

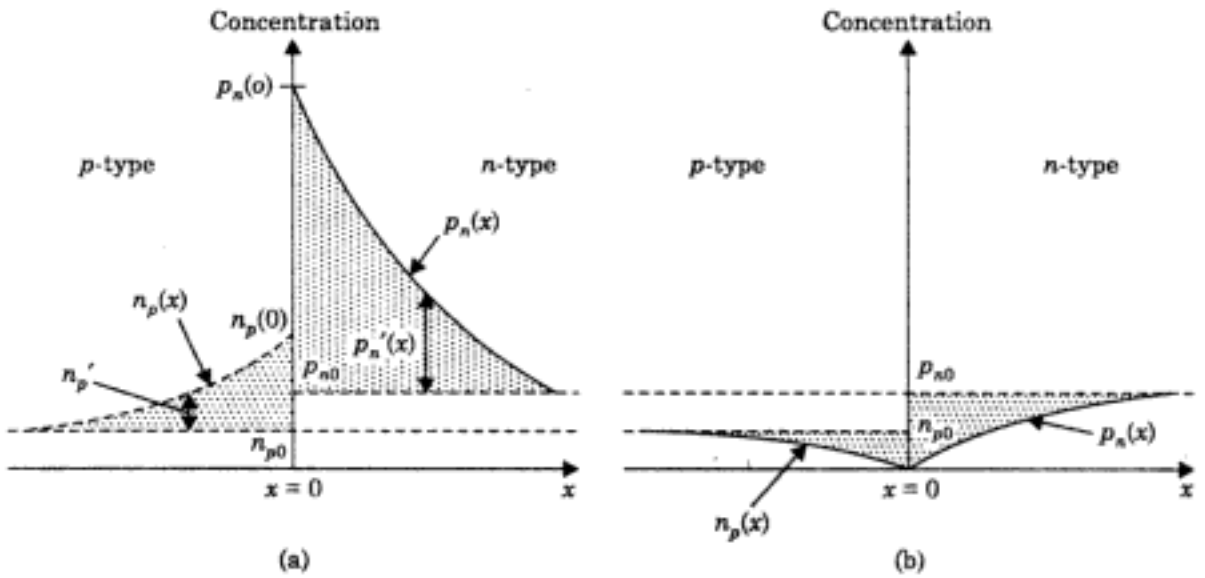


Fig. 2.28 (a) Minority carrier $p_n(x)$, $n_p(x)$ density for forward bias
(b) Minority carrier densities for reverse bias.

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Thus, we can mathematically express this decay, for excess holes, by an expression

$$p_n'(x) = p_n'(0)e^{-x/L_p} = p_n(x) - p_{n0} \tag{2.41}$$

where

$p_n'(x)$ = Excess/injected holes from p- to n-side at any point x
$p_n'(0)$ = Excess/injected holes at $x = 0$ i.e. the junction point
p_{n0} = Thermally generated holes in n-side (must remain constant barring disturbances of injection holes)
L_p = Diffusion length for holes in metres
τ_p = Mean lifetime of holes in seconds,
D_p = Hole diffusion constant (m^2/sec)

Also, we have the following relation [to be proved later, see Eq. (2.51)]

$$L_p = (D_p \tau_p)^{1/2} \tag{2.42}$$

where L_p = Mean free path for holes (m)

L_p is also called (mathematically found) the **mean free path** for a hole. After time τ_p, i.e., at $x = L_p$, the intensity of excess/injected holes $p_n'(x)$ becomes *36.7%* ($= e^{-1}$) of $p_n'(0)$. Figure 2.28(a) shows $p_n' = p_n - p_{n0}$ falling off exponentially with increase of x.

The behaviour of excess minority carriers $n_p'(x)$ (equalling $n_p(x) - n_{p0}$) is similar to that of $p_n'(x)$. Here, the corresponding diffusion length of electrons, mean life time of electrons and electron diffusion constant is, respectively L_n, τ_n and D_n. Also, $L_n = (D_n \tau_n)^{1/2}$ holds.

The law of the junction states that the net hole concentration $p_n(0)$ at $x = 0^+$ (on the n-side of the junction) is a function of forward bias voltage V_D applied across the junction, i.e.,

$$p_n(0) = p_{n0} e^{V_D/V_T} \tag{2.43}$$

Note that for no forward bias V_D applied, $p_n(0) = p_{n0}$ as directed by thermal equilibrium conditions. Similarly, if $n_p(0)$ is the electron concentration at $x = 0^-$ (i.e., on p-side), n_{p0} is the electron concentration at $x = 0^-$ due to thermal equilibrium voltage V_T and V_D is the forward voltage bias applied across the junction then the law of the junction holds for p-side also, i.e.,

$$n_p(0) = n_{p0} e^{V_D/V_T} \tag{2.44}$$

2.13.2 Reverse-Biased Junction

From the laws of the junction, given by Eqs. (2.43) and (2.44), if V_D is –ve and much greater than V_T (as is the usual case in practice) then

$$p_n(0) = n_p(0) = 0 \text{ at } x = 0$$

i.e. the concentrations of minority carriers (p on n-side and n on p-side) is identically zero at $x = 0$ (i.e. at the junction). We can explain this physically also. With reverse-biased junction, the depletion region, which is almost at the junction, has +ve ions on n-side and –ve ions on p-side. Under the influence of reverse bias (+ve on n-side and –ve on p-side) the minority carriers in n and p regions get pushed towards the junction. As soon as these minority carriers, say, holes from n-side cross the junction, these have to pass through the

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depletion region on p-side, which has –ve ions, and these get absorbed. Similarly, the minority carriers, electrons from p-side get absorbed in the depletion region on n-side (which has +ve ions). In short, the concentration of minority carriers, under the reverse bias condition is zero at the junction $x = +0$ or $x = -0$. This is shown in Fig. 2.28(b). However, the steady state, i.e., thermal equilibrium like conditions must hold as we move away from the junction $x = 0$ towards end of p-side ($x = -\infty$) and towards the end of n-side ($x = +\infty$), so the curves $p_n(x)$ and $n_p(x)$ must exponentially rise from zero to the values p_{n0} and n_{p0}, respectively as seen in Fig. 2.28(b).

2.14 CALCULATION OF DIFFUSION CAPACITANCE C_D

Let us first understand how much charge Q is produced by a forward conducting diode.

The total current due to both a potential gradient and a concentration, say, for holes is given by Eq. (1.40)

$$I_p = J_p A = A\left[\underbrace{q\mu_p p\varepsilon}_{\text{Drift current part}} - \underbrace{qD_p \frac{dp}{dx}}_{\text{Diffusion current part}}\right] \tag{2.45}$$

Under forward biased condition the total current is given by

$$\text{Total diode current, } I = I_p(0) + I_n(0) \tag{2.46}$$

where $I_p(0)$ = Current due to holescrossing p to n side

$I_n(0)$ = Current due to electrons n to p side

Theoretically, it can be shown that the minority-carrier drift current crossing the junction is negligible as compared with the minority-carrier diffusion current.

Assume p-side heavily doped w.r.t. n-side so that the current I crossing the junction is entirely due to holes from p- to n- side. From Eq. (2.46),

$$\therefore \quad I = I_p(0) + I_n(0)$$

$$\approx I_p(0) \qquad [\text{for } I_n(0) << I_p(0)]$$

i.e., $$I = I_p(0) \tag{2.47}$$

But $$I_p(x) = A\left[q\mu_p p\varepsilon - qD_p \frac{dp}{dx}\right]$$

$$\approx -AqD_p \frac{dp_n}{dx} \qquad \text{(neglecting drift current w.r.t. the diffusion current)}$$

$$= -AqD_p\left[\frac{d}{dx}(p_{n0} + p_n'(0)\, e^{-x/L_p})\right]$$

[due to Eq. (2.41) $p_n(x) = p_{n0} + p_n'(0)e^{-x/L_p}$]

where p_{n0} is a constant: thermally generated holes.

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Thus, $$I_p(x) = -AqD_p\left[p_n'(0).e^{-x/L_p}\left(-\frac{1}{L_p}\right)\right]$$

or $$I_p(x) = \frac{AqD_p\,p_n'(0)}{L_p}e^{-x/L_p} \tag{2.48}$$

As $$I = I_p(x)\big|_{x=0} = \frac{AqD_p\,p_n'(0)}{L_p}\text{ Amp} \tag{2.49}$$

We have assumed current mainly due to holes crossing to *n*-side (because of heavy doping of *p*-side as compared to the *n*-side). Thus, *the minority carriers* (excess minority carrier, i.e., holes) *produce charge Q only on n-side.* On the *n*-side, since excess minority carriers obey

$$p_n'(x) = p_n'(0)\,e^{-x/L_p} \qquad \text{[due to Eq. (2.41)]}$$

Therefore, Charge $$Q = \int_0^\infty Aq\,p_n'(x)\,dx \qquad \text{(due to excess minority carriers)}$$

$$= \int_0^\infty Aq\;p_n'(0)\,e^{-x/L_p}\,dx$$

$$= Aq\,p_n'(0)\left[\frac{e^{-x/L_p}}{-1/L_p}\right]_0^\infty$$

i.e., $$Q = -AqL_p\,p_n'(0)\;(0-1)$$

or $$Q = AqL_p\,p_n'(0) \tag{2.50}$$

Dividing Eq. (2.49) by Eq. (2.50), to eliminate $p'(0)$, we have

$$\frac{I}{Q} = \frac{AqD_p p_n'(0)}{L_p} \times \frac{1}{AqL_p p_n'(0)}$$

$$= \frac{D_p}{L_p^2} = \frac{1}{\tau_p}$$

$\therefore$ $$I = \frac{Q}{\tau_p} \quad \text{and} \quad \tau_p = \frac{L_p^2}{D_p} \tag{2.51}$$

D_p = Hole diffusion constant (m^2/s)

L_p = Mean free path for holes (m)

τ_p = Mean life time for holes (sec)

Q = Charge, due to minority carriers (holes) in *n*-side, in Coulomb

I = Diode current in A (neglecting electron current $I_n(0)$ as *p*-side is heavily doped w.r.t. *n*-side)

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Relation (2.51) is called 'charge-control description of a diode' relation. It states that the current I supplies the minority carriers at the rate at which these carriers are disappearing because of the process of recombination, in the steady state. I is linearly related to Q through the constant τ_p. If Q is +ve, the diode is forward biased and if Q is –ve, the diode is reverse biased.

2.14.1 Diffusion Capacitance C_D

In a forward-biased diode, the minority carrier storage (say, holes in n-side) can be described by *storage* or *Diffusion Capacitance* C_D.

As
$$C_D = \frac{dQ}{dV}$$
$$= \frac{d(I\tau)}{dV} \qquad [\because\ Q = I\tau \text{ from Eq. (2.51)}] \qquad (2.52)$$
$$= \tau \frac{dI}{dV}$$

$\therefore$
$$C_D = \tau g_d = \tau \frac{1}{r_d} \qquad \text{[see Eqs. (2.17) and (2.18)]}$$

Now, Dynamic resistance of a diode $r_d = \dfrac{dV}{dI}$

But
$$r_d = \frac{1}{g_d} = \frac{\eta V_T}{I_{DQ}} \qquad \text{[due to Eq. (2.22)]} \qquad (2.53)$$

Using Eq. (2.53) in Eq. (2.52), we obtain

$$C_D = \frac{\tau I_{DQ}}{\eta V_T} = \frac{\tau}{r_d} \qquad (2.54)$$

where I_{DQ} = Steady state quiescent current (in A)

V_T = thermal voltage = $\dfrac{T}{11{,}600}$ volts, T in kelvin

η = 2 for Silicon and 1 for Germanium transistors

We assumed that electron current $I_n(0)$ is zero for deriving Eq. (2.54). If the hole current $I_p(0)$ and the electron current $I_n(0)$ are both to be considered, then $C_D = C_{D_p} + C_{D_n}$, where C_{D_p} is given by Eq. (2.54) for the hole current. C_{D_n} would be obtained from a similar expression.

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EXAMPLE 2.18

Given a forward-biased Silicon diode with $I = 1$ mA. If the diffusion capacitance is $C_D = 1\ \mu$F, what is the diffusion length L_p? Assume that the doping of the p-side is much greater than that of the n-side.

Solution We know that

$$L_p = (D_p \tau_p)^{1/2} \qquad \text{[From Eq. (2.51)]} \qquad \text{(i)}$$

$$C_D = \frac{\tau I}{\eta V_T} \qquad \text{[From Eq. (2.54)]} \qquad \text{(ii)}$$

and

$$V_T = \frac{T}{11{,}600} \qquad \text{(iii)}$$

where L_p = Diffusion length for holes (m)

D_p = Diffusion constant (m^2/s) for holes

(= 47 for Ge and 13 for Si)

τ_p = Mean life time of the hole (seconds)

V_T = volt equivalent of temperature T (= 26 mV for $T = 300$ K)

η = a constant in $I = I_0(e^{V/\eta V_T} - 1)$

($\eta = 1$ for Ge, $\eta = 2$ for Si)

From Eq. (i),

$$\tau_p = \frac{L_p^2}{D_p}$$

Using $\tau = \tau_p = L_p^2 / D_p$ in Eq. (ii), we get

$$C_D = \frac{L_p^2}{D_p} \cdot \frac{I}{\eta V_T}$$

$$\therefore \quad L_p^2 = \frac{C_D D_p \eta V_T}{I}$$

$$= \frac{(1 \times 10^{-6})(13) \times (2)(26 \times 10^{-3})}{1 \times 10^{-3}}$$

$$= (26)^2 \times 10^{-6}$$

or $L_p = 26 \times 10^{-3}$ m = 2.6 cms. **Ans.**

2.15 SWITCHING TIME OF THE JUNCTION DIODE

The transient response of a diode, driven from an ON to an OFF state or from an OFF state to an ON state, is an important parameter of a diode which limits its operation at high frequency. Transient time is the time that elapses before the diode reaches to its new state.

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Consider a simple diode circuit shown in Fig. 2.29(a). In input signal, v_i shown in Fig. 2.29(b) is applied which changes from $+V_F$ to $-V_R$ at the time $t = t_1$. We assume that R_L is much larger than the diode forward resistance R_f (i.e., $R_L >> R_f$), also assume that the forward voltage V_F (which v_i assumes) is much greater than the cut-in voltage V_γ (i.e., $V_F >> V_\gamma$). The input voltage v_i is applied much before we reckon time $t = t_1$. This is to ensure that at $t = t_1$, the diode is conducting in the forward direction and current $i_D \approx V_F/R_L$, direction of i_D is shown in Fig. 2.29(a). During the forward conduction of the diode (forward bias) the majority carriers cross the junction and diffuse across the junction. Figure 2.29(c) shows the excess minority carriers (i.e., holes having crossed the junction to the n-side). The value $p_n'(o)$ shows the excess minority carriers at the junction on n-side and equals overall concentration $p_n(0)$ minus the thermal equilibrium concentration p_{n0} (when there is no v_i).

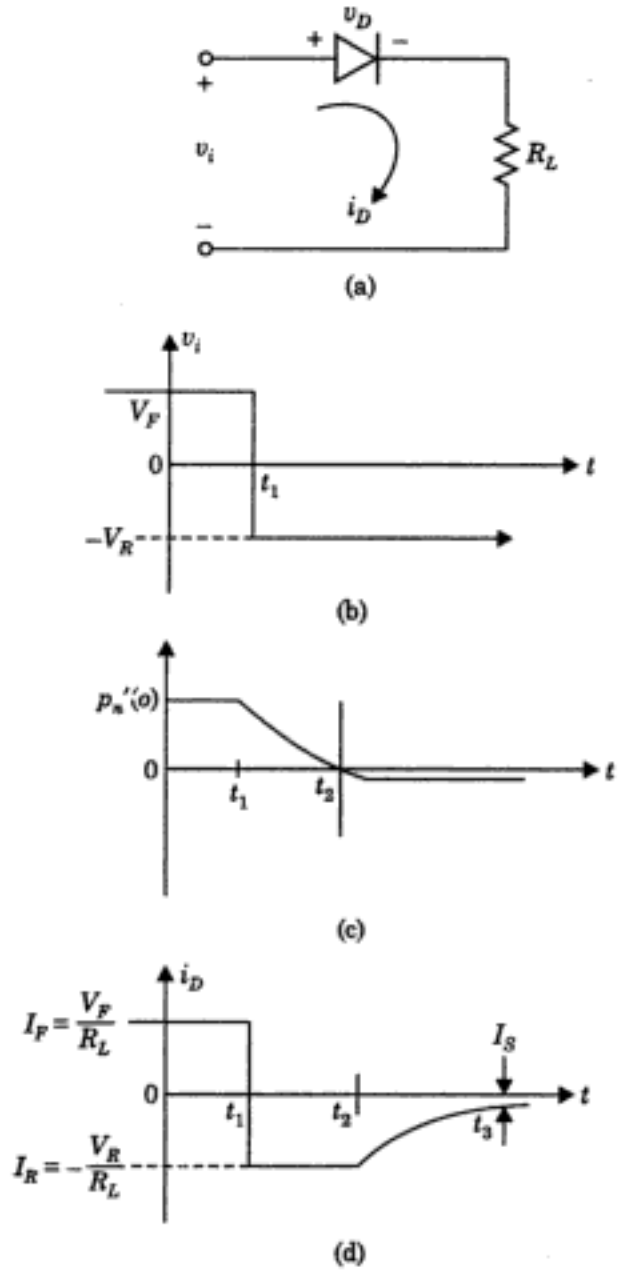


Fig. 2.29 (a) A diode D with a resistor R_L and input voltage v_i, (b) Input voltage v_i which changes abruptly from $+ V_F$ to $- V_R$ at $t = t_1$, (c) Excess carrier density at the junction, Note that $p_n'(0) = p_n(0) - p_{n0}$ (see Fig. 2.28), (d) The diode current.

At time $t = t_1$, as v_i changes its value from $+V_F$ to $-V_R$, it amounts to reverse biasing the diode. A reverse-bias diode should pass I_S as the reverse current when in equilibrium and when the proper depletion region has been formed. As long as there are excess minority carriers near the junction, these tend to cross the junction from where they had come, due to reverse voltage V_R. (Recollect that a forward bias helps majority carriers to go towards the junction and a reverse bias helps minority carriers to go towards the junction). This causes a reverse current of $-V_R/R_L$ since the diode having no depletion region, but having sufficient minority carriers near the junction, has low resistance. The ohm's law allows maximum current of magnitude V_R/R_L shown as I_R in Fig. 2.29(d). As long as these stored minority carriers can supply sufficient number of holes, necessary to make up current V_R/R_L, the reverse current remains constant as shown in Fig. 2.29(d) from time t_1 to t_2. Having drained most of the minority carriers to support current V_R/R_L, at time t_2

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their concentration is low and unable to continue passing current V_R/R_L. Thus, from t_2 onwards the current i_D decays from its value $(-V_R/R_L)$ to $(-I_S)$ at time t_3. When $i_D = -I_S$ the diode has passed on to OFF mode. We define

Storage time $t_s = t_2 - t_1$, where $i_D = -V_R/R_L$ (constant)

Transition time $t_t = t_3 - t_2$, when i_D decays from $-V_R/R_L$ to $-I_S$

Reverse recovery time $t_{rr} = t_s + t_t$ (2.55)

Thus, t_{rr} is the time interval which elapses between the time of switching the signal v_i to reverse voltage and the time the diode actually having assume OFF state. In general the storage time t_s is much greater than the transition time t_t. If we wish to have low reverse recovery time t_{rr}, we should aim at decreasing t_s. In point contact diodes, the value of t_s is very small. Commercial switching-type diodes are available with t_{rr} much less than a nanosecond (10^{-9} second) and also there are diodes where t_{rr} is as high as 1 microsecond (10^{-6} second). The diodes with low t_{rr} are meant for the memory devices and should pass very small current during forward conduction. The diodes with large t_{rr} are used for large current and where high frequency operation is not important.

When a diode is OFF and we apply a forward voltage to switch it ON, some time elapses before the diode comes to ON state. This time is called **forward recovery time** t_{fr}. In general t_{fr} is reckoned as the time required for the diode to change the current from 10% to 90% of its final value when the diode is switched ON from OFF state. The forward recovery time t_{fr} is much lower than the reverse recovery time t_{rr} and, therefore, may be ignored for approximate calculations.

One of the methods to realize a diode having low t_{rr}, is to minimise its storage time t_s. This is done in Schottky Barrier diode as explained in the next Section 2.17.

2.16 SCHOTTKY BARRIER DIODES

The junction formed by a metal and extrinsic semiconductor (i.e., *p*-type or *n*-type) can be either rectifying or ohmic. Figure 2.30(a) shows two types of contacts made by Al with *n*-type silicon. If Al is deposited on a heavily doped (n^+) silicon, as in contact 2, the formation of a *p-n* junction is prevented and we get a non-rectifying or an ohmic contact. However, if Al is directly deposited on the *n*-type silicon (contact 1), we obtain a rectifying contact called Schottky diode. Figure 2.30(b) compares the V-I characteristics of a Schottky diode with the ordinary silicon diode. It is seen that

(i) cut-in voltage V_γ is lower in Schottky diode,

(ii) the reverse current is greater in the Schottky diode.

Both these features result from the high electron concentration in the metal (Alumnium). With greater number of carriers available, comparable currents are obtained at lower cut-in or other voltage v_D. Similarly, this large number of carrier makes the saturation current higher.

The Schottky diodes are principally used in *IC* for fast switches (than the junction diodes). As it is a majority-carrier device (there are no minority carriers in the metal), the storage time t_s is negligible. The reverse recovery time $t_{rr} \approx t_t$ since $t_s \approx 0$. Thus, for fast switching operations the Schottky diodes are particularly useful.

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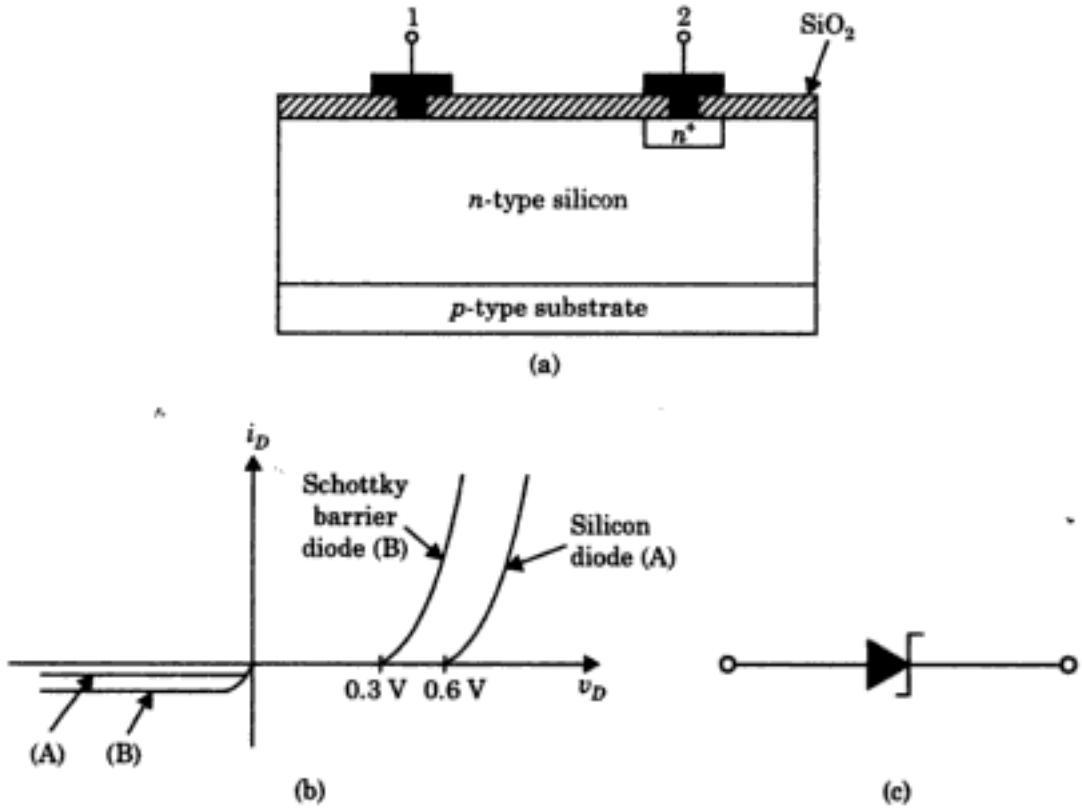


Fig. 2.30 (a) Structure showing metal to semiconductor contacts (b) *V-I* characteristics of Schottky barrier diode and Silicon diode (c) Circuit symbol (Note *S*-type marking on cathode).

2.17 ZENER DIODES

The avalanche multiplication and zener breakdown are the two processes which produce the breakdown region in the reverse-biased characteristics of the diode shown in Fig. 2.31(a). The diodes having adequate power dissipation capabilities to operate in the breakdown region are commonly called **zener diodes** (The term **zener diode** is used independently of the breakdown mechanism). The zener diodes give nearly constant voltage, V_Z for large changes in the diode current and thus are extensively used in Voltage Regulators.

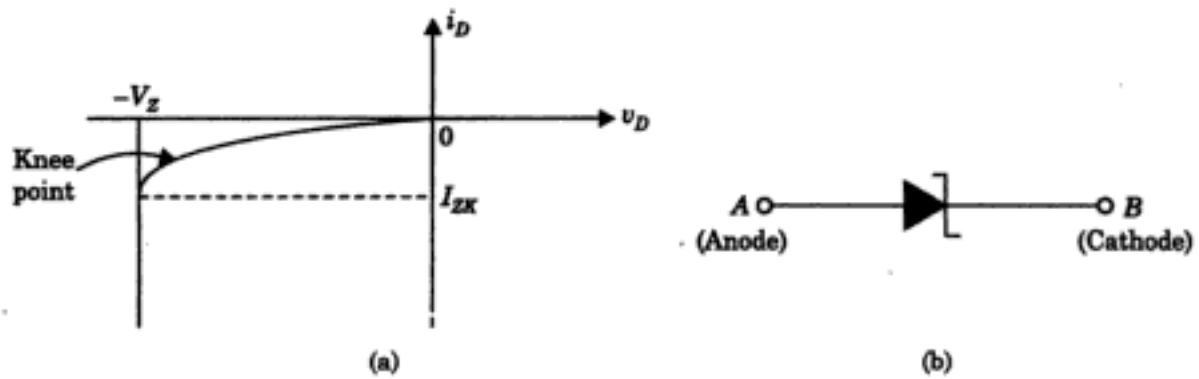


Fig. 2.31 (a) Reverse-bias characteristic showing breakdown region for a zener diode, (b) Zener diode symbol (Note the *Z*-type marking on cathode).

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2.17.1 Avalanche Multiplication

Consider a reverse-biased diode. A thermally generated carrier (forming part of the reverse saturation current I_S) falls down the junction barrier voltage since electrons on p-side and holes on n-side (which form the minority carriers in their respective region) are assisted by a reverse bias. In fact the depletion region barrier voltage V_0 assists the minority carriers alongwith the externally applied reverse bias, to fall towards the junction. If the value of V_0 plus the reverse bias (applied externally) is sufficiently high then the thermally generated carriers acquire energy and gain velocity from the applied reverse voltage. These sufficiently high velocity carriers collide with a crystal ion, impart this ion sufficient energy and consequently disrupt its covalent bond. In addition to the original carriers (which disrupted the covalent bond), a new electron-hole pair is also generated. This additionally generated carriers may also pick up sufficient energy and generate still other electron-hole pairs by collision by disrupting other covalent bonds. This process results in a large reverse current and the diode is said to have avalanche breakdown.

2.17.2 Zener Breakdown

Here, the breakdown of the covalent bonds takes place not by collision (as in avalanche breakdown) but by producing sufficient high electric field at the junction. A sufficient strong force may be exerted on the covalently-bound electrons such that the strong field tears off the covalent bonds. In tearing process, we have generated an electron-hole pair. These newly created electron-hole pairs increase the reverse current. Note that the Zener breakdown does not involve collision of carriers with the crystal ions.

Zener breakdown occurs at about the field intensity of 2×10^7 V/m. This value is achievable by a reverse voltage of 6 V using heavily doped junctions. For lightly doped diodes, the breakdown voltage is higher, and there the avalanche multiplication is predominant.

Silicon diodes operated in avalanche breakdown for maintaining voltages *from a few volt to several hundred volts* and with *power ratings upto 50 W* are available.

Though the end results of both the avalanche breakdown and the zener breakdown are the same (generation of very high currents) but there are few vital differences in these processes, as follows:

2.17.3 Comparison between Zener Effect and Avalanche Effect

Zener effect	*Avalanche effect*
1. Caused by *field ionization.*	1. Caused by *impact ionization.*
2. Direct bond rupture occurs due to high electric field at the junction.	2. Due to high fields, the charge carriers acquire high velocities, i.e. high energies sufficient to ionize the electron-hole pairs. The carriers, thus liberated, ionize further electron-hole pairs. It is a cumulative effect.

(contd.)

Zener effect	*Avalanche effect*
3. Zener effect occurs at approximately 2×10^7 V/m. This value is reached at voltages below about 6 V.	3. Avalanche effect occurs at voltages usually above 7 V.
4. Zener diodes have lower resistance. (Zener diodes are heavily doped)	4. Avalanche diodes have higher resistances. (Avalanche diodes are not heavily doped)
5. They have soft knee.	5. They have harder/sharper knee.
6. For reference voltage below 6 V (and hence zener breakdown), the temperature coefficient is negative.	6. For reference voltage above 6 V, (and hence Avalanche breakdown), the temperature coefficient is positive.

2.17.4 Zener Diode Models

The zener diode characteristic shown in Fig. 2.31(a) may be approximated by a piece-wise linear *V-I* relationship (as was done for a forward-biased diode). Figure 2.32(a) gives the DC model where R_Z represents the static resistance. When the breakdown is virtually vertical [Fig. 2.31(a)], then $R_Z = 0$.

The small-signal model, is shown in Fig. 2.31(b) where,

$$\text{Dynamic resistance } r_z = \frac{\Delta V_Z}{\Delta I_Z} \tag{2.56}$$

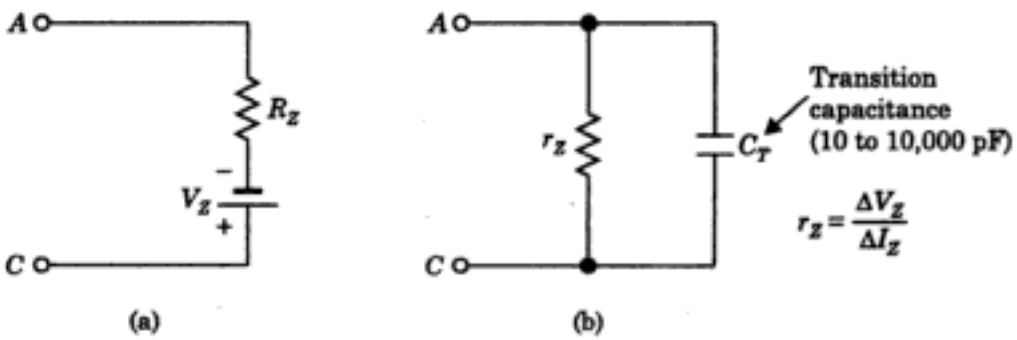


Fig. 2.32 (a) DC model of the zener diode, (b) Small signal model of the zener diode.

Ideally, $r_Z = 0$, corresponding to the vertical characteristic. Practically, r_Z is a few ohms. However, for currents below I_{ZK}, r_Z may be a few hundred ohms. As zener diode operates in the reverse-bias, the transition capacitance, C_T must also be taken into account in the small-signal model as shown in Fig. 2.32(b) and is proportional to the cross-sectional area of the diode. C_T may vary from 10 to 10,000 pF for high-power avalanche diodes.

2.17.5 A Simple Zener Regulator

A zener diode regulator circuit shown in Fig. 2.33(a) is used to maintain a constant output voltage, $V_0 = V_Z$ for varying load R_L and for unregulated source voltage $V_S > V_Z$. The equivalent circuit is shown in Fig. 2.33(b). It can be seen that

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$$I_S = I_L + I_Z$$

$$\therefore \quad I_Z = I_S - I_L = \frac{V_S - V_Z}{R_S} - \frac{V_Z}{R_L} \qquad (\because\ V_0 = V_Z = I_L R_L) \qquad (2.57)$$

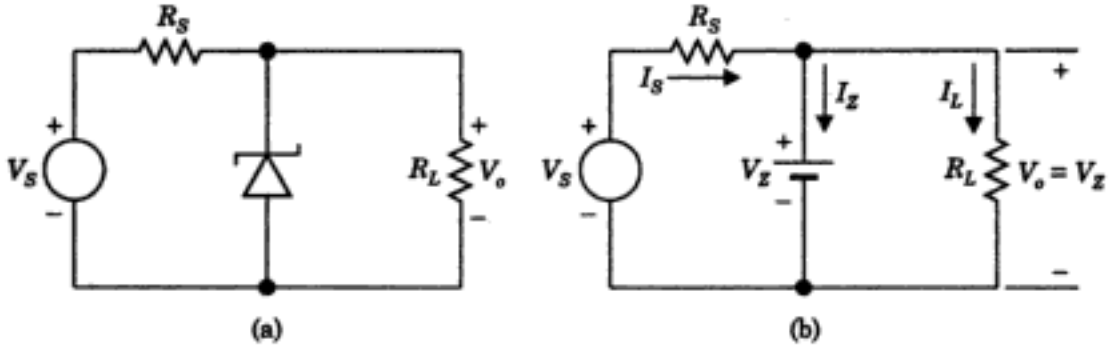


Fig. 2.33 (a) Simple zener regulator circuit, (b) Its equivalent circuit diagram.

If V_S is constant, I_Z varies with variation of load R_L. Also, for V_S constant, $I_S = (V_S - V_Z)/R_S$ is constant. As I_L increases, I_Z decreases and vice versa. A zener diode is specified by low as well as high current limitations. The high current limitation is determined by the power dissipation capability of the zener diode. The limitation of lower limit zener current is I_{ZK}. For $I_Z < I_{ZK}$ (the knee point zener current) the regulation is poor and the output voltage deviates from V_Z. For a given diode, the limits on I_Z also restrict the minimum and maximum values of the source voltage V_S.

Generally, the value of knee current I_{ZK} is specified by the manufacturers. However, as a rule of thumb choose I_{ZK} to be 5 to 10% of the maximum rated current, in case I_{ZK} is not specified.

2.17.6 Rule to Solve Numericals for Zener Voltage Regulators Designs

Let V_S have values $V_{S\,\min}$ to $V_{S\,\max}$. (minimum to maximum DC voltage). Let zener diode with V_Z voltage have $I_{Z\,\min}$ and $I_{Z\,\max}$ as the limiting current (minimum to maximum zener currents). Let the load currents vary from $I_{L\,\min}$ to $I_{L\,\max}$. Then

1. Ensure that $V_{S\,\min}$ is greater than V_Z (the required regulated output voltage).
2. Ensure that the range $(I_{Z\,\max} - I_{Z\,\min})$ is greater than $(I_{L\,\max} - I_{L\,\min})$
3. Use the relations:

$$\frac{(V_{S\,\max} - V_Z)}{R_S} = I_{Z\,\max} + I_{L\,\min} \qquad (2.58a)$$

$$\frac{V_{S\,\min} - V_Z}{R_S} = I_{Z\,\min} + I_{L\,\max} \qquad (2.58b)$$

Zener maximum power rating $\quad P_Z = I_{Z\,\max} \cdot V_Z \qquad (2.58c)$

These three relations must be satisfied, for the given design. Voltage regulator design problems are given in Chapter 3.

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EXAMPLE 2.19

(a) Two p-n Silicon diodes are connected in series as shown in Fig. 2.34(a). A 5 V battery is impressed upon this series arrangement. Find the voltage across each junction at room temperature (300 K). Assume the magnitude of zener voltage is greater than 5 V.

(b) If the magnitude of the zener voltage is 4.9 V, what will be the current in the circuit. The reverse saturation current is 5 μA.

Solution: Assume $\eta V_T = 0.026$ V

(a) We have Zener voltage greater than 5 V.

In Fig. 2.34(a) as per connections, diode D_1 is forward biased and D_2 is reverse biased. The diode D_1 passes the same current as the reverse biased current of D_2.

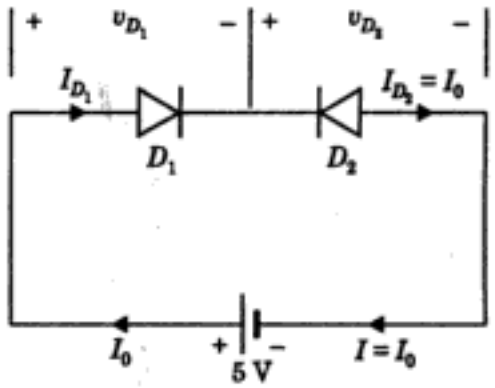


Fig. 2.34(a) Circuit for Ex. 2.19(a).

i.e., $$I_{D_1} = I_0 = 5\,\mu A$$

To cause 5 μA in D_1, we satisfy the relation:

$$I_{D_1} = I_o = I_o(e^{v_{D_1}/\eta V_T} - 1)$$

$$\therefore \quad e^{v_{D_1}/\eta V_T} - 1 = 1$$

$$e^{v_{D_1}/0.026} = 2$$

$$v_{D_1} = 0.026 \times \ln 2 = 0.0173 \text{ V} \quad \textbf{Ans.}$$

or $$v_{D_2} = 5 - v_{D_1} = 4.9827 \text{ V} \quad \textbf{Ans.}$$

[*To check, what current voltage v_{D_2} causes in D_2*]

D_2 is reverse biased, therefore,

$$I_{D_2} = I_0(e^{-4.9827/0.026} - 1)$$

$$= I_0(5.89 \times 10^{-84} - 1) \approx I_0(0 - 1)$$

$$= -I_0$$

Thus, our assumption of $I_{D_1} = I_0$ was justified.

(b) Refer to Fig. 2.34(b). Here, applied voltage is 5 V, but for diode D_2 the zener voltage is 4.9 V. (Given)

Thus, 4.9 V gets locked for D_2, therefore,

$$v_{D_1} = 5 - 4.9 = 0.1 \text{ V}$$

$$I_{D_1} = I_0(e^{0.1/0.026} - 1)$$

$$= (5\ \mu A)(46.81 - 1)$$

$$= 229\ \mu A \quad \textbf{Ans.}$$

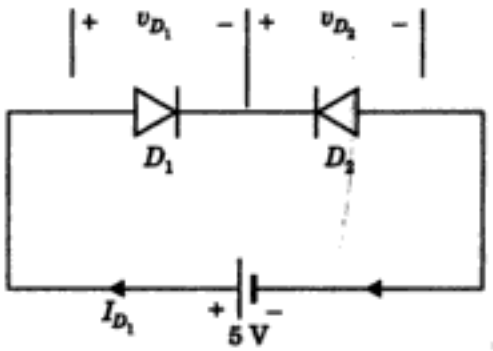


Fig. 2.34(b) Here $v_{D_2} = V_Z = 4.9$ V, $v_{D_2} = 4.9$ V (Zener volt) and $v_{D_1} = 0.1$ V.

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Hence, diode D_1 passes forward current $I = I_{D_1} = 229\ \mu A$ and this is also the reverse current for diode D_2.

SUMMARY

- A *p-n* junction diode is formed by a single crystal having one side doped by *p* (acceptor) material and the other side doped by *n* (donor) material.
- The doping concentration may be equal or different on *p* and *n* sides.
- Near the junction some holes of *p*-side and an equal number of electrons of *n*-side recombine. This leaves –ve ions on *p*-side and +ve ions on *n*-side.
- The area depleted of charge carriers and having only ions is called the **depletion region**.
- The potential difference due to charges (in depletion region) on opposite side of the junction causes a barrier voltage V_γ which prevents further recombinations of holes and electron. The barrier voltage is also denoted by V_0 or V_B.
- By forward biasing, i.e., +ve on *p*-side and –ve on *n*-side, the barrier voltage decreases and the width of the depletion region decreases.
- It is possible to fully neutralize the effect of barrier by applying forward bias equal to V_γ. This renders the depletion width to zero.
- If we apply reverse bias (–ve on *p*-side and +ve on *n*-side of the junction), the depletion region increases.
- If we short circuit the *p* and *n* terminals, no current flows in the diode.
- The volt-ampere characteristics of a *p-n* junction diode is given by $I_D = I_S(e^{V_D/\eta V_T} - 1)$, where I_S is called the reverse saturation current and $V_T = T/11{,}600$ volt.
- For forward bias, V_D, $I_D \approx I_S e^{V_D/\eta V_T}$, and for reverse bias, $I_D \approx -I_S$.
- I_S is temperature dependent. I_S doubles for every 10°C rise of temperature.
- As temperature increases, diode voltage, V_D should be reduced at the rate of 2.2 mV/°C mV/°C for maintaining a constant I_D.
- The load line is $V_{AA} = I_D R + V_D$ and is a straight line. The Quiescent point *Q* is the intersection of load line and the diode characteristics $I_D = I_S e^{V_D/\eta V_T}$.
- For drawing a DC model (large signal model) the diode is replaced by a barrier voltage V_γ and forward resistance R_f. $V_\gamma \approx 0.5$ to 0.6 V for Silicon and 0.2 to 0.3 V for Germanium *p-n* junction diodes.
- Reverse biased diode behaves as an open switch or high conduction resistance R_r where $R_r \to \infty$, and a small conduction current equalling I_S.
- For drawing small signal (AC model), forward resistance R_f is ignored and diode is replaced by its dynamic resistance r_d.

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- Incremental conductance $g_d = \left.\frac{di_D}{dV_D}\right|_Q$ and $r_d = \frac{1}{g_d}$, $r_d = \frac{\eta V_T}{I_{DQ}}$ at Q-point.
- For forward-biased diodes, diffusion capacitance is given by

$$C_D = \frac{\tau I_{DQ}}{\eta V_T} = \frac{\tau}{r_d}$$

where τ is mean carrier time in seconds.

- Reverse-biased junction diodes exhibit transition capacitance given by

$$C_T = \frac{\varepsilon A}{W}$$

where W is the depletion width and A is the area of cross-section of the junction.

- Switching times are important parameters for choice of diodes especially at high frequency and use of diodes in memory matrix.
- Reverse recovery time $t_{rr} = t_s + t_t$ where t_s is the storage time and t_t is the transition time.
- Schottky barrier diode is formed by a metal and extrinsic (p- or n-type) semiconductor material. The storage time t_s is very small for Schottky diodes, and such diodes are more suitable for the operation at high frequency.
- Avalanche multiplication and zener breakdown cause the same end result, resulting high currents, and keeping voltage constant across the zener diode (V_Z).
- Zener diodes are extensively used in voltage regulators.
- Voltage regulation is possible if the input unregulated DC voltage V_{dc} exceeds V_Z and $(I_{Z\,max} - I_{Z\,min})$ exceeds $(I_{L\,max} - I_{L\,min})$.

REVIEW QUESTIONS

2.1 In a p-n junction, where is the magnitude of the electric field intensity maximum?

2.2 What is the depletion region? What constitutes the space charge? (a) holes and electrons (b) donor and acceptor ions.

2.3 What external polarity means forward bias?

(i) positive on p-side and negative on n-side

(ii) positive on n-side and negative on p-side?

2.4 What happens to the width of the depletion region when we apply reverse bias to the p-n junction diode?

2.5 Can we directly measure the barrier voltage V_γ?

2.6 Explain the significance of each parameter in the equation $I_D = I_S(e^{V_D/\eta V_T} - 1)$.

2.7 Why does I_S in the above equation act as a scale factor for the diode current I_D?

2.8 How does I_S (the reverse saturation current) vary with temperature variation?

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2.9 At constant current I_D, how does the diode voltage V_D vary with temperature?

2.10 What parameters are different in Germanium and Silicon diodes? Give their typical values.

2.11 Why do we say that the volt-ampere characteristics of an ideal diode resemble a switch?

2.12 What is a load line? How is it drawn? How do we obtain the Quiescent point Q?

2.13 Under forward-biased conditions, how do the following parameters vary if the diode current is increased?

(a) the resistance r_d (b) diffusion capacitance C_D.

2.14 Why do we use DC model and AC model separately for the diode to determine its total current i_D?

2.15 Why does the depletion capacitance C_T decrease with the increase of reverse bias?

2.16 Explain the physical mechanism which produces (a) avalanche breakdown, (b) zener breakdown.

2.17 Draw a typical volt-ampere characteristics of a zener diode. Why is the knee on the curve so important?

NUMERICAL PROBLEMS

P2.1 Assuming that the diodes in the given circuits [see Fig. 2.35(a) and (b)] are ideal, find the values of the labelled voltages and currents.

[***Ans.*** (a) I = 1 mA, I_{D_2} = 1 mA, I_R = 2 mA]

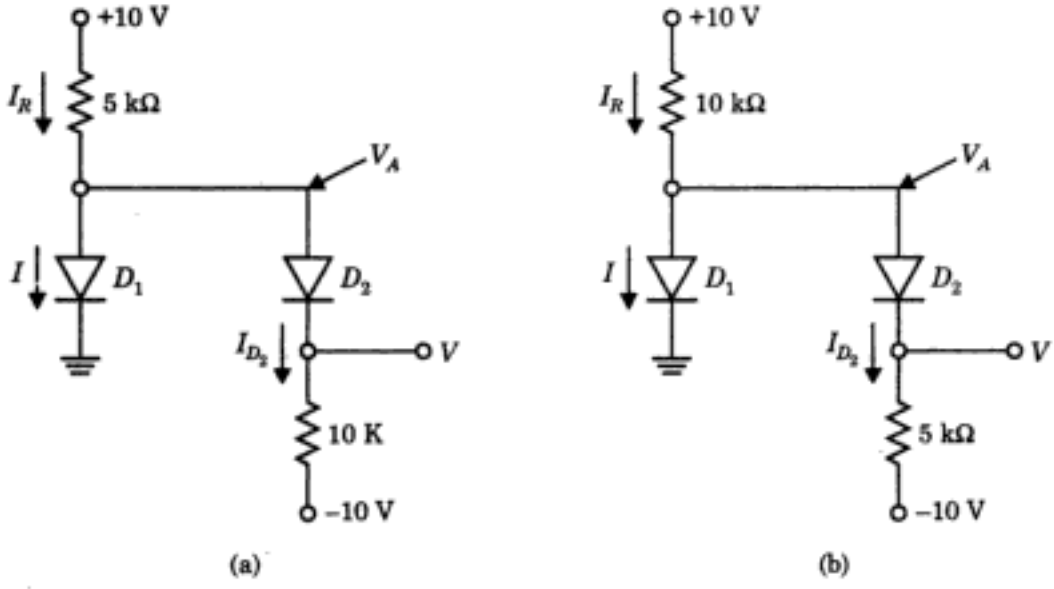


Fig. 2.35 Circuits for P2.1

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P2.2 A Silicon diode is operated at a constant forward voltage of 0.7 V. What is the ratio of the maximum to minimum current in the diode over a temperature range –55°C to +100°C.

[***Ans.*** I_{max}/I_{min} = 46340]

P2.3 For a forward-biased *p-n* junction, find the diode voltage V_D at which the diode current I_D assumes 290% of the maximum reverse saturation current at room temperature.

[***Ans.*** If $\eta = 1$ (i.e., Ge), V_D = 34 mV; if $\eta = 2$ (i.e., Si), V_D = 68 mV]

P2.4 Discuss the dependence of dynamic resistance of a diode on temperature. If the reverse saturation current of a *p-n* junction diode is 1 μA at 300 K, find its dynamic resistance at 150 mV forward bias.

[***Ans.*** r_d = 62 Ω; R_{stat} = 7.86 K for Si and 373 Ω for Ge]

P2.5 An ideal Silicon Diode has a static resistance of 4.57 Ω while conducting 43.8 mA at T = 300 K. Find the dynamic resistance of the diode for a forward voltage of 0.1 V.

[***Ans.*** r_d = 8.125 Ω for Si and r_d = 27.8 for Ge diodes]

P2.6 A diode is mounted on a chasis in such a manner that for each degree of temperature rise above ambient, 0.1 mW is thermally transferred from the diode to its surroundings (The thermal resistance of the mechanical contact between the diode and its surroundings is 0.1 mW/°C). The ambient temperature is 25°C. The diode temperature is not to be allowed to increase by more than 10°C above ambient. If the reverse saturation current is 5 μA at 25°C and increases at the rate of 0.07/°C, what is the maximum reverse-biasing voltage that can be maintained across the diode.

[***Ans.*** V = 100 V reverse biased]

P2.7 Determine the current I_D and the diode voltage V_D for the current shown in Fig. 2.36 with V_{DD} = 10 V, R = 1.5 kΩ. Assume that the diode has a current of 1 mA at a voltage of 0.7 V, and that its voltage drop changes by 0.1 V for every decade change in current.

[***Ans.*** I_D = 6.1475 mA, V_D = 0.7788 V]

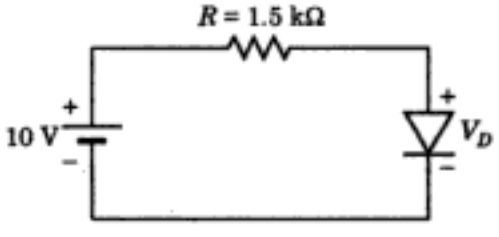


Fig. 2.36 Circuit for P2.7.

P2.8 It is predicted that, for Ge, the reverse saturation current should increase by 0.11/°C. It is found experimentally in a particular diode that at reverse voltage of 10 V, the reverse saturation current is 5 μA and the temperature dependence is only 0.07/°C. Find the leakage resistance shunting the diode.

[**Hint:** Equivalent circuit of Fig. 2.37(a) is shown in Fig. 2.37(b) with leakage resistance (R)

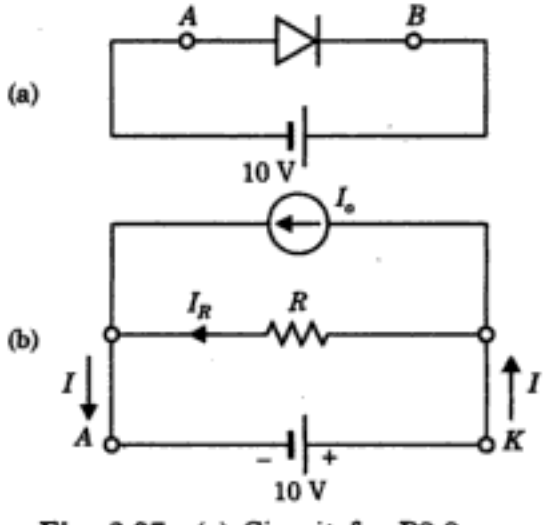


Fig. 2.37 (a) Circuit for P2.8
(b) Equivalent circuit.

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Use relations:

$$I = I_R + I_0$$

$$\frac{dI}{dT} = \frac{dI_0}{dT} \qquad [\text{as } I_R \text{ is independent of } T]$$

$$\frac{1}{I}\frac{dI}{dT} = 0.07$$

$$\frac{1}{I_0}\cdot\frac{dI_0}{dT} = 0.11$$

[***Ans.*** R = 5.5 MΩ]

P2.9 Reverse-biased diodes are frequently employed as electrically controlled variable capacitors. The transition capacitance of an abrupt junction diode is 20 pF at 5 V. Compute the decrease in capacitance for a 1.0 V increase in bias.

[***Ans.*** The result of Example 2.16, i.e., $C_T = \dfrac{AqN_AN_D\varepsilon}{2(N_A+N_D)^{1/2}}\cdot\dfrac{1}{\sqrt{V}}$. Increase of reverse voltage from 5 V to 6 V (reverse bias) decreases the transistor capacitance from 20 pF to 18.25 pF)

P2.10 The zero-voltage barrier height at an alloy-Germanium p-n junction is 0.2 V. The concentration N_A of acceptor atoms in the p-side is much smaller than the concentration of the donor atoms in the n-material and $N_A = 3 \times 10^{20}$ atoms/m^3. Calculate the width of the depletion layer for an applied reverse voltage of (a) 10 V (b) 0.1 V and (c) for a forward bias of 0.1 V (d) If the cross-sectional area of the diode 1 mm^2, evaluate the space-charge capacitance corresponding to the values of applied voltage in (a) and (b).

[***Ans.*** (a) 7.75 μm; (b) 1.329 μm; (c) 0.767 μm; (d) 18.25 pF for (a); and 106 pF for (b)]

P2.11 Prove that the reverse saturation current (I_S) in a p-n junction diode is given by

$$I_S = Aq\left(\frac{D_p}{L_pN_D} + \frac{D_n}{L_nN_A}\right)n_i^2$$

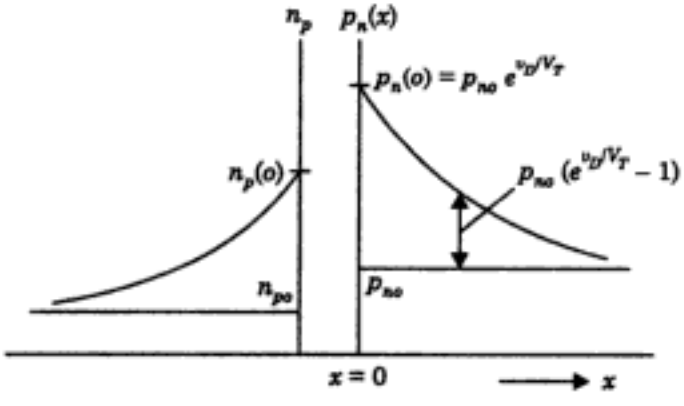


Fig. 2.38(a)

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[**Hint:** For forward conduction of the diode, the total diode current

$$I_D = I_{pn}(0) + I_{np}(0)$$

$I_{pn}(0)$: diffusion of holes in N-side; $I_{np}(0)$: diffusion of electrons on P-side

We know that

$$I_{pn}(x)\Big|_{x=0} = -Aq D_p \frac{dp}{dx}\Big|_{x=0}$$

$$= -Aq D_p \frac{d}{dx}(p_{n0} e^{V_D/V_T} - p_{n0}) e^{-x/L_p}\Big|_{x=0} \quad \left(\begin{matrix}\text{due to law of}\\ \text{the junction}\end{matrix}\right)$$

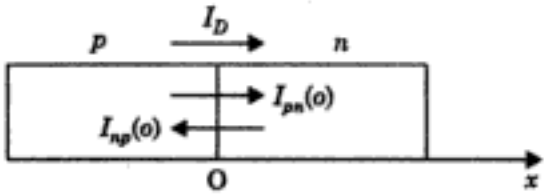


Fig. 2.38(b)

$$= -Aq D_p \frac{d}{dx}(p_{no}(e^{V_D/V_T} - 1)) e^{-x/L_p}$$

$$\therefore \quad I_{pn}(0) = +Aq p_{n0} \frac{D_p}{L_p}(e^{V_D/V_T} - 1)$$

[At $x = 0$, hole current direction is $\rightarrow$ as shown in Fig. 2.38(b)]

Similarly, we get:

$$I_{np}(0) = +Aq n_{po} \frac{D_n}{L_n}(e^{V_D/V_T} - 1) \qquad \text{(electronic current } \leftarrow\text{)}$$

Total diode current is, therefore,

$$I_D = I_{pn}(0) + I_{np}(0) = Aq(e^{V_D/V_T} - 1)\left[\frac{p_{n0}D_p}{L_p} + \frac{n_{p0}D_n}{L_n}\right]$$

$$= \underbrace{Aq\left(\frac{p_{n0}D_p}{L_p} + \frac{n_{p0}D_n}{L_n}\right)}_{\triangleq I_S}(e^{V_D/V_T} - 1) \quad [\text{From } I_D = I_S(e^{V_D/V_T} - 1)]$$

$$\therefore \quad I_S = Aq\left(\frac{p_{n0}D_p}{L_p} + \frac{n_{p0}D_n}{L_n}\right)$$

$$= Aq\left(\frac{(n_i^2/N_D).D_p}{L_p} + \frac{(n_i^2/N_A)D_n}{L_n}\right) \qquad \left(\because\ p_{n0} = \frac{n_i^2}{N_D}, n_{p0} = \frac{n_i^2}{N_A}\right)$$

$$\therefore \quad I_S = Aq\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right) n_i^2 \quad \textbf{Ans.}$$

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CHAPTER 3

Applications of Diodes

3.1 INTRODUCTION

In Chapter 2 we have studied some important properties of *p-n* junction diodes. The diodes form a useful subset of passive components used in electronic circuits. Their property of conduction only when these are forward biased can be gainfully exploited for waveshaping as well as for other several applications. In this chapter, we shall discuss the following topics, where the diodes are used:

3.1 Rectifiers–halfwave and fullwave rectifiers, Bridge rectifier, Rectifier meter.

3.2 Capacitor filters used in Rectifier circuits.

3.3 Voltage multiplier circuits—including voltage doubler, voltage tripler and voltage quadrupler etc.

3.4 Zener voltage regulator.

3.5 Clipping and clamping circuits.

The chapter contains a large number of solved examples. The difficult problems are provided with hints.

3.2 RECTIFIERS

A rectifier is a circuit which converts AC voltage to DC voltage. In a large number of electronic/electrical circuits, we require DC voltage for operation. We can convert AC voltage to DC voltage by using diodes. The diode may be a *p-n* junction (for small currents) or a valve type (for large currents). We shall, however, use *p-n* junction diodes in circuits discussed in this chapter.

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3.2.1 Half-wave Rectifier

We know that the approximate model of a diode is as given below:

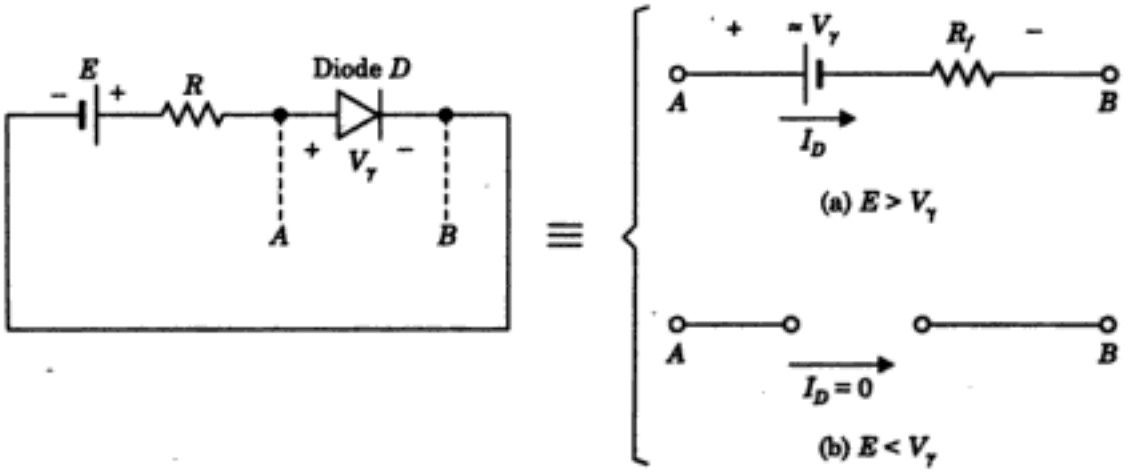


Fig. 3.1 ON/OFF property of a diode (a) diode D is ON (conducts) for E greater than V_γ (b) diode D is OFF (open circuit) for E less than V_γ.

Suppose that a supply voltage E is applied across the diode D through a resistor R, as shown in Fig. 3.1. The diode D is supposed to have cut-in voltage V_γ implying that when voltage E is greater than V_γ, D will conduct as shown in Fig. 3.1(a). In this case the diode D is replaced by a voltage source in series with forward conducting diode resistance (= R_f). Voltage V_{AB} in Fig. 3.1(a) is approximately V_γ. Note that $V_\gamma = 0.7$ V for Silicon diodes and $V_\gamma = 0.3$ V for Germanium diodes. When diode D conducts [Fig. 3.1(a)], the diode current I_D is given by

$$I_D = \frac{E - V_\gamma}{R + R_f} \tag{3.1}$$

Thus, if $R_f << R$, $I_D \approx (E - V_\gamma)/R$. The resistor R acts as a safety against passage of high current through the diode (because if $R = 0$ and R_f is very very small, $I_D = (E - V_\gamma)/R_f$ may be very high which may damage the diode D).

On the other hand, if E is less than V_γ, diode D cannot conduct. Its equivalent circuit is shown in Fig. 3.1(b), with $I_D = 0$ and $V_{AB} = E$.

Now, consider a half-wave rectifier circuit shown in Fig. 3.2(a), i.e., a diode D supplied by an AC voltage v_s and load resistance R_L in series with D and v_s. Let

$$v_s = V_{\max} \sin \omega t$$

We assume $V_\gamma = 0$ and $R_f = 0$ here for simplicity. When diode D is ON then

$$i = \frac{v_s}{R_L} = \frac{V_{\max} \sin \omega t}{R_L} \tag{3.2}$$

The current i has half cycles in the range 0 to π, 2π to 3π and so on, i.e., for generic angle range $(2k\pi) \le \omega t \le (2k + 1)\pi$. The Fourier analysis of the current i is given by

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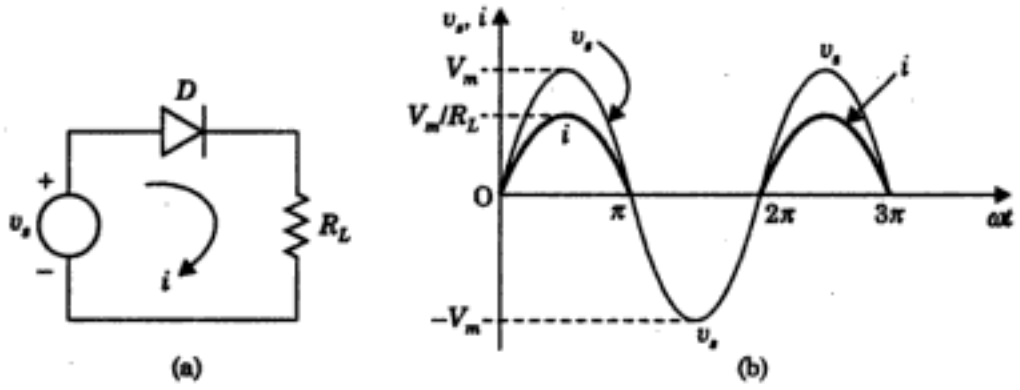


Fig. 3.2 (a) Half-wave rectifier, (b) Current and voltage waveforms.

$$i = \left[a_0 + \sum_{n=1}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t) \right] . \frac{V_{max}}{R_L} \tag{3.3}$$

where

$$\left.\begin{aligned} a_o &= \frac{1}{2\pi} \int_0^{\pi} \sin\theta \, d\theta, \quad a_n = \frac{1}{\pi} \int_0^{\pi} \sin\theta \, . \cos n\theta \, d\theta \\ b_n &= \frac{1}{\pi} \int_0^{\pi} \sin\theta \, . \sin n\theta \, d\theta \end{aligned}\right\} \tag{3.4}$$

It may be seen that a_0 when calculated by Eq. 3.4 comes out to be $1/\pi$. Clearly, the average value of the current i is $\left(\frac{V_{max}}{R_L}\right)\Big/\pi$, since the AC components in the summation sign on RHS of Eq. (3.3) have zero average values. It is, therefore, important to note that the average value of the output current i in the load resistor R_L is not zero (but is equal to $V_{max}/\pi R_L$) though the average value of the input voltage v_s is zero. This is the basis of the rectifier circuit whereby we aim at obtaining a DC voltage and DC current (which have non-zero average values), from AC voltage (which has zero average value).

Now we consider the circuit of a half-wave rectifier using a non-ideal diode (i.e., $V_\gamma \neq 0$ and $R_f \neq 0$), as shown in Fig. 3.3. To make calculations easy, we first take the case of diode having $V_\gamma = 0$ but $R_f \neq 0$ for simplicity. We shall take $V_\gamma \neq 0$ and also $R_f \neq 0$ after discussing the operation of full-wave rectifier.

Let v_i = Input sinusoidal voltage = $V_{max} \sin \omega t$, i.e., peak value = V_{max}

V_γ = Cut-in voltage, say, zero here

D = Ideal diode

R_f = Forward resistance of diode when D is ON ($R_f \neq 0$)

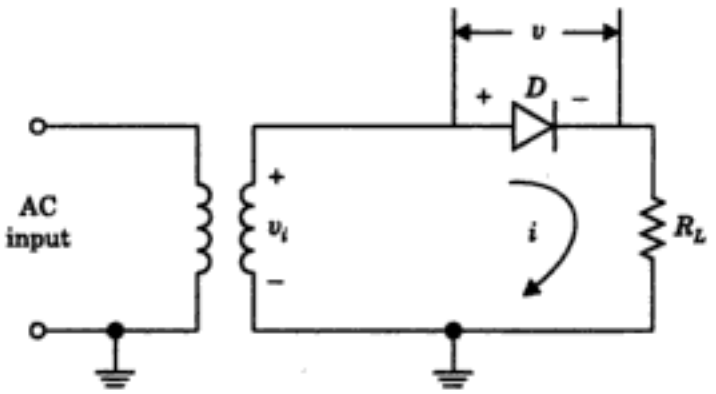
During conduction of the diode

$$i = \frac{v_i}{R_f + R_L}, \quad \therefore \quad I_{max} = \frac{V_{max}}{R_f + R_L} \tag{3.5}$$

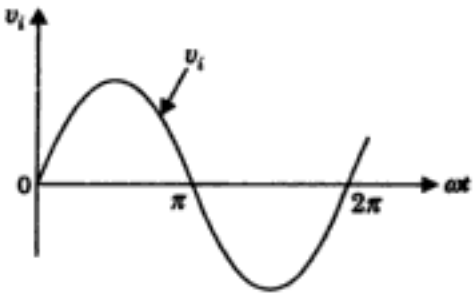
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Thus,
$$i = \begin{cases} I_{max} \sin \alpha, & 0 \le \alpha \le \pi \\ 0, & \pi \le \alpha \le 2\pi \end{cases} \tag{3.6}$$

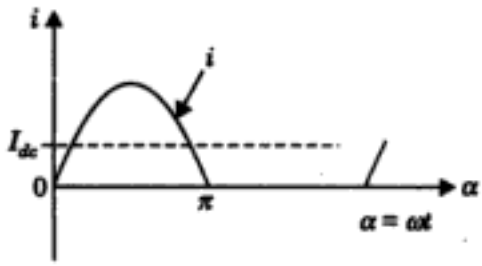
where $\alpha = \omega t$.



(a)



(b)



(c)

Fig. 3.3 (a) Basic half-wave rectifier, (b) Transformer O/P sinusoidal voltage, (c) Diode and load current i.

A DC ammeter constructed to read the average current passing through it would read

$$I_{dc} = \text{Average of } i = \frac{1}{2\pi}\int_0^{2\pi} i\, d\alpha \tag{3.7}$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_{max} \sin \alpha\, d\alpha + \int_0^{2\pi} (0)\, d\alpha\right] \quad (\because\ i = 0, \text{ for } \pi \le \alpha \le 2\pi)$$

$$= \frac{I_{max}}{2\pi}\left[-\cos \alpha\right]_0^{\pi} = \frac{I_{max}}{\pi}$$

$\therefore$
$$I_{dc} = \frac{I_{max}}{\pi} \quad \text{for half-wave rectifier} \tag{3.8}$$

$$\text{Output voltage } V_{dc} = I_{dc}R_L = \frac{I_m R_L}{\pi} \tag{3.9}$$

Diode Voltage: The average of v must be found, to find the reading of a DC voltmeter placed across the diode D with polarity as shown in Fig. 3.4.

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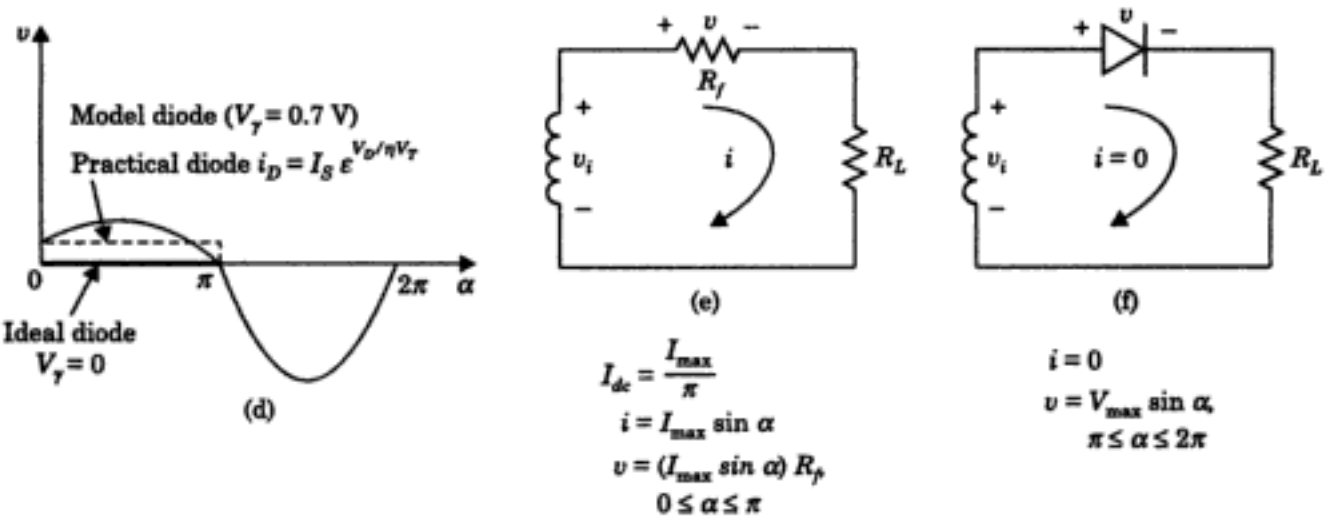


Fig. 3.3 (d) Voltage v across the diode during conduction ($\alpha = 0$ to π) and non-conduction ($\alpha = \pi$ to 2π) and (e) Equivalent circuit when Diode is ON, (f) Equivalent circuit when Diode is OFF.

We can write the voltage v across the diode (assuming an ideal diode with $V_\gamma = 0$) as:

$$v = \begin{cases} (I_{max} \sin \alpha) R_f, & 0 \le \alpha \le \pi \quad (D \text{ conducts}) \\ V_{max} \sin \alpha, & \pi \le \alpha \le 2\pi \quad (D \text{ OFF}) \end{cases}$$

Average DC voltage across the diode, defined as V'_{dc} is, therefore, given by

$$V'_{dc} = \frac{1}{2\pi} \int_0^{2\pi} v(t)\, d\alpha$$

$$= \frac{1}{2\pi} \left[\int_0^{\pi} (I_{max} R_f \sin \alpha)\, d\alpha + \int_{\pi}^{2\pi} V_{max} \sin \alpha\, d\alpha \right]$$

$$= \frac{1}{2\pi} \left\{ I_{max} R_f \left[-\cos \alpha \right]_0^{\pi} + V_{max} \left[-\cos \alpha \right]_{\pi}^{2\pi} \right\}$$

$$= \frac{1}{2\pi} \left[I_{max} R_f (1+1) - V_{max} (1+1) \right]$$

$$= \frac{1}{\pi} \left[I_{max} R_f - V_{max} \right]$$

$$= \frac{1}{\pi} \left[I_{max} R_f - I_{max} (R_f + R_L) \right] \qquad \left(\because I_{max} = \frac{V_{max}}{R_f + R_L} \right)$$

$$= -\frac{I_{max} R_L}{\pi} \qquad \text{[from Eq. (3.5)]}$$

Thus, Average DC voltage across diode $V'_{dc} = -\dfrac{I_{max} R_L}{\pi}$

$$= -V_{dc} \tag{3.10}$$

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This result is obvious because average DC voltage around the complete circuit is zero (average of $v_i = V_{max} \sin \alpha$ is zero).

AC Current (Voltage): We note that the output current i (and voltage iR_L) is not a pure DC. It contains a non-zero DC value plus ac components as given by Fourier analysis (see Eq. 3.3). We wish to determine the root-mean square (rms) value of such a current i and that of voltage v. A root-mean-square current is defined as:

$$I_{rms} = \left(\frac{1}{2\pi}\int_0^{2\pi} i^2\, d\alpha\right)^{1/2}, \quad i = I_{max} \sin \alpha \tag{3.11}$$

and a root mean square voltage is defined as:

$$V_{rms} = \left(\frac{1}{2\pi}\int_0^{2\pi} v^2\, d\alpha\right)^{1/2}, \quad v = V_{max} \sin \alpha \tag{3.12}$$

For input voltage,

$$v_i = V_{max} \sin \alpha$$

Then

$$V_{rms} = \left(\frac{1}{2\pi}\int_0^{2\pi} V_{max}^2 \sin^2 \alpha\, d\alpha\right)^{1/2}$$

$$= \left(\frac{1}{2\pi}\int_0^{2\pi} \frac{V_{max}^2}{2}(1 - \cos 2\alpha)\, d\alpha\right)^{1/2}$$

$$= \left(\frac{1}{2\pi}\frac{V_{max}^2}{2}\left[\alpha - \frac{\sin 2\alpha}{2}\right]_0^{2\pi}\right)^{1/2}$$

$$= \left(\frac{V_{max}^2}{2}\right)^{1/2}$$

$$\therefore \quad V_{rms} = \frac{V_{max}}{\sqrt{2}} \quad \text{for a sinusoidal input voltage} \tag{3.13}$$

(This is a well known result for a pure sine wave voltage)

For output current, as given by Eq. (3.6) for half-wave rectifier

$$i = \begin{cases} I_{max} \sin \alpha, & 0 \le \alpha \le \pi \\ 0, & \pi \le \alpha \le 2\pi \end{cases}$$

Then

$$I_{rms}\big|_{\text{half-wave rectifier}} = \left(\frac{1}{2\pi}\int_0^{\pi} I_{max}^2 \sin^2 \alpha\, d\alpha\right)^{1/2}$$

$$= \left(I_{max}^2 \cdot \frac{1}{4}\right)^{1/2}$$

$$\therefore \quad I_{rms} = \frac{I_{max}}{2};\ V_{rms} = \frac{I_{max.}\, R}{2} \quad \text{for half-wave rectifiers} \tag{3.14}$$

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Regulation: The variation of DC output voltage as a function of DC load is called the regulation. The percentage regulation is defined as:

$$\% \text{ regulation} = \frac{V_{\text{no load}} - V_{\text{load}}}{V_{\text{load}}} \times 100 \tag{3.15}$$

'No load' refers to zero load current and 'load' refers to normal load current. For an ideal power supply, the output voltage is independent of the load, i.e., its regulation is zero percent. For the case of half-wave rectifier if we assume $V_\gamma = 0$, then

$$I_{dc} = \frac{I_{\max}}{\pi} = \frac{V_{\max}/\pi}{R_f + R_L} \tag{3.16}$$

and

$$V_{\text{load}} = I_{dc} R_L$$

$$= \frac{V_{\max}}{\pi}\left(\frac{1}{R_f + R_L}\right).R_L$$

$$= \frac{V_{\max}}{\pi}\left(1 - \frac{R_f}{R_f + R_L}\right)$$

$$\therefore \quad V_{\text{load}} = \frac{V_{\max}}{\pi} - I_{dc} R_f \qquad \left[\because \frac{V_{\max}/\pi}{R_f + R_L} = I_{dc} \text{ from Eq. (3.16)}\right] \tag{3.17}$$

Thus, the V_{load} voltage varies with variation of load current I_{dc} due to the presence of resistance R_f. Had R_f been zero, V_{load} would have remained constant at $V_{\max}/\pi$, and the resultant DC voltage source would have performed like an ideal voltage source. However, due to the presence of R_f, the output voltage V_{load} decreases for higher load currents.

Equation (3.17) shows that we can model it as a Thevenin's equivalent power supply as shown in Fig. 3.4.

$$V_{\text{load}} = \frac{V_{\max}}{\pi} - I_{dc}\, R_f$$

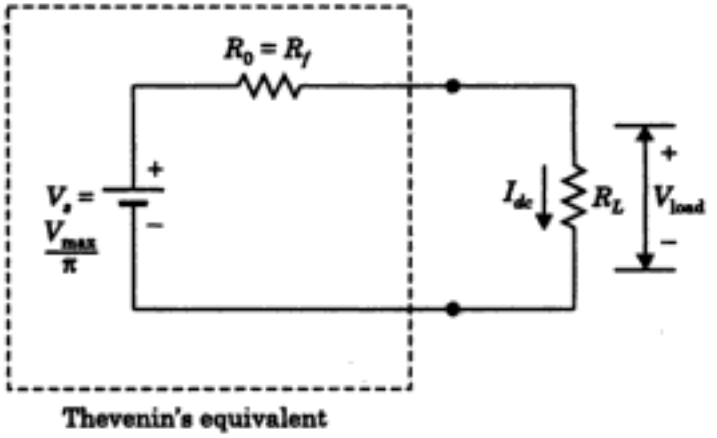


Fig. 3.4 The Thevenin's equivalent of a power supply used to determine the load voltage and the current for the half-wave rectifier. V_s represents source DC voltage and R_0 the source output resistance.

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In practice, the resistance R_0 should include the resistance R_f as well as the secondary winding resistance of the transformer, i.e.

$$R_0 = R_f + R_s$$

where R_f = Diode forward resistance

R_s = Secondary winding's resistance.

3.2.2 A Full-wave Rectifier

A full-wave rectifier comprises two half-wave rectifiers as shown in Fig. 3.5. Conduction takes place through one diode during one half of the power cycle and through the other during the second half of the cycle.

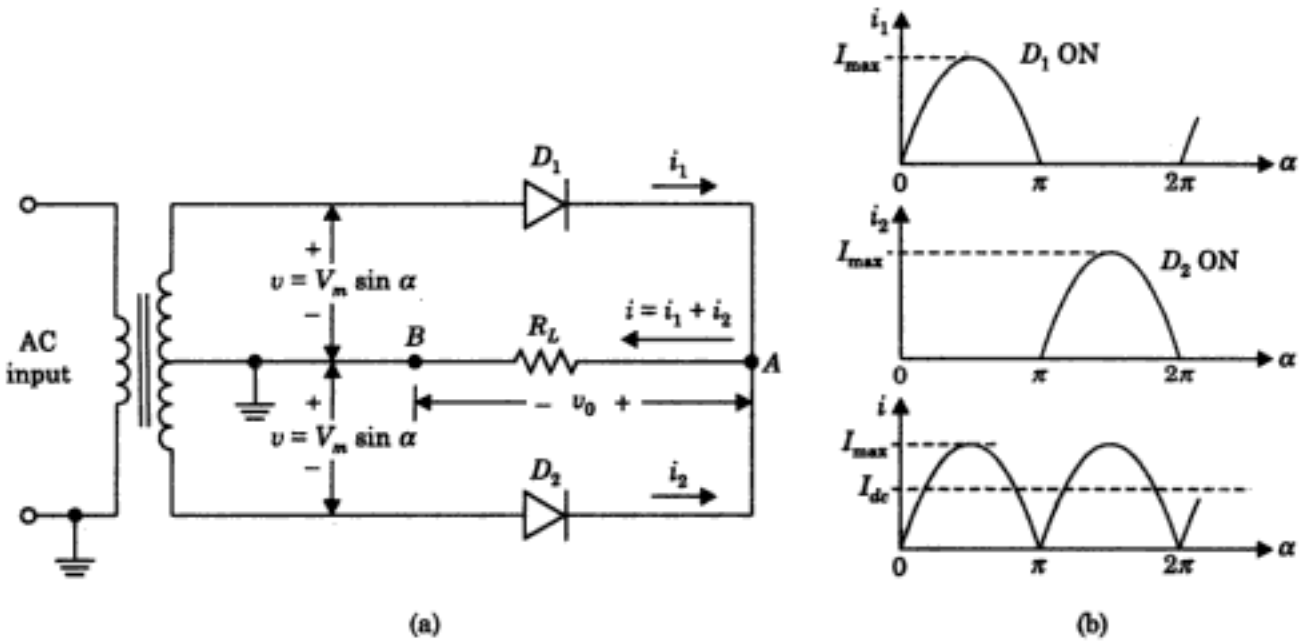


Fig. 3.5 (a) A full-wave rectifier circuit, (b) The diode currents i_1 and i_2 and the load current i. The output voltage $v_0 = iR_L$.

Note that when $v = V_m \sin \alpha$ is positive, diode D_1 is ON and D_2 is OFF and i_1 flows for $\alpha = 0$ to π, and $i_2 = 0$. Similarly, when $v = V_m \sin \alpha$ is negative, diode D_1 is OFF and D_2 is ON, $i_1 = 0$ and i_2 flows for $\alpha = \pi$ to 2π. The current i_1 and i_2 are shown in Fig. 3.5(b). Both the currents i_1 and i_2 flow through the load resistance R_L, hence $i = i_1 + i_2$ as shown in Fig. 3.5(b).

$$\text{Load current } i = i_1 + i_2 \tag{3.18}$$

and Average of i = Average of i_1 + Average of i_2

$$\therefore \quad I_{dc} = \frac{I_{max}}{\pi} + \frac{I_{max}}{\pi} = \frac{2I_{max}}{\pi} \tag{3.19}$$

where $$I_{max} = \frac{V_{max}}{(R_f + R_L)}$$

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Clearly, for full-wave rectifier

$$I_{dc} = \frac{2I_{max}}{\pi}$$

and
$$V_{load} = I_{dc}R_L = \frac{2I_{max}}{\pi}R_L \tag{3.20}$$

where
$$I_{max} = \frac{V_{max}}{(R_f + R_L)} \tag{3.20a}$$

Clearly,
$$I_{rms} = \frac{I_{max}}{\sqrt{2}} \tag{3.20b}$$

The DC output voltage of a full-wave rectifier is twice that of the half-wave circuit. If we assume $V_\gamma = 0$ then

$$V_{load} = \frac{2R_L}{\pi} I_{max} \qquad \left(\because I_{dc} = \frac{2I_{max}}{\pi}\right)$$

$$= \frac{2R_L}{\pi} \frac{V_{max}}{(R_f + R_L)}$$

$$\left(\because I_{max} = \frac{V_{max}}{R_f + R_L}\right)$$

$$= \frac{2V_{max}}{\pi} - \frac{2V_{max}}{\pi} \frac{R_f}{R_f + R_L}$$

$$= \frac{2V_{max}}{\pi} - \frac{2}{\pi} I_{max}R_f$$

$$= \frac{2V_{max}}{\pi} - I_{dc}R_f$$

$$\therefore \quad V_{load} = \frac{2V_{max}}{\pi} - I_{dc}R_f \tag{3.21}$$

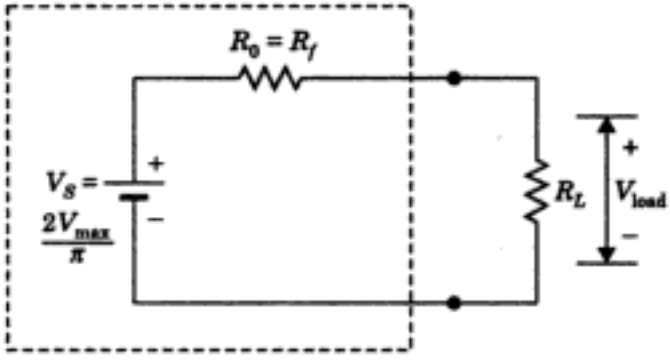


Fig. 3.6 The Thevenin's equivalent of a power supply used to determine the load voltage V_{load} and the current for the full-wave rectifier. V_s represents the source DC voltage and R_0 its output resistance.

The equivalent Thevenin's circuit is shown in Fig. 3.6. If we do not ignore transformer secondary winding resistance (R_S), then we replace R_f by $(R_f + R_S)$ in Eq. (3.21). Note that R_S is secondary winding resistance of half secondary part of the transformer since at one time only one diode is ON causing conduction current in half part of the secondary winding. As for the half wave rectifier case, the regulation is improved if R_0 is lower.

EXAMPLE 3.1

Show that the maximum DC output power $P_{dc} = V_{dc}I_{dc}$ in a half-wave single phase circuit occurs when the load resistance equals the diode resistance R_f.

Solution For half-wave rectifier Thevenin's equivalent shown in Fig. 3.7:

$$I_{dc} = \frac{V_{max}}{\pi(R_f + R_L)}$$

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$$\therefore \quad P_{dc} = I_{dc}^2 R_L = \frac{V_{max}^2}{\pi^2 (R_f + R_L)^2} . R_L$$

To have P_{dc} maximum, if we vary, say R_L, keeping R_f constant we let

$$\frac{dP_{dc}}{dR_L} = 0$$

As $$\frac{dP_{dc}}{dR_L} = \left(\frac{V_{max}^2}{\pi^2}\right) \frac{1.(R_f + R_L)^2 - R_L . 2(R_f + R_L)}{(R_f + R_L)^4}$$

Putting $\frac{dP_{dc}}{dR_L} = 0$ gives us

$$(R_f + R_L)^2 = 2R_L(R_f + R_L)$$

i.e., $$R_f + R_L = 2R_L$$

$$\therefore \quad R_L = R_f \quad \textbf{Ans.}$$

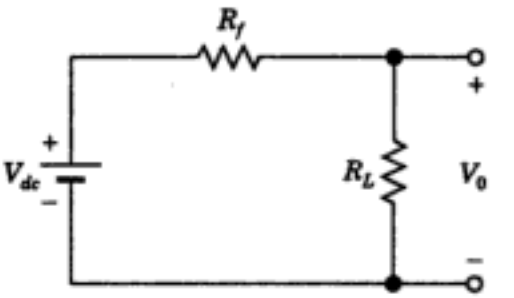


Fig. 3.7 Equivalent circuit, Ex. 3.1. $V_{dc} = V_{max}/\pi$ here.

Note: The answer is obvious if we use Maximum Power Transfer Theorem. For full-wave rectifiers too, the same condition holds true.

Effect of cut-in voltage V_γ: If the effect of cut-in voltage V_γ is not ignored, we may represent such a non-ideal diode by R_f in series with V_γ in series with ideal diode as shown in Fig. 3.8. Here, the conduction commence, when $\theta = \theta_1$ (θ_1 is called the ignition angle):

$$V_\gamma = V_{max} \sin \theta_1$$

$$\therefore \quad \sin \theta_1 = \frac{V_\gamma}{V_{max}}$$

The extinction results at θ_2 such that $\theta_2 = \pi - \theta_1$ (due to symmetry in Fig. 3.8b)

Thus, **Ignition angle** $\theta_1 = \sin^{-1} \frac{V_\gamma}{V_{max}}$ (3.22a)

Extinction angle $\theta_2 = \pi - \theta_1$ (3.22b)

The average current I_{dc} is found to be (see Example 3.2)

$$I_{dc} = \frac{V_{max}}{\pi(R_f + R_L)} \cos \theta_1 - \frac{\pi - 2\theta_1}{2\pi} \frac{V_\gamma}{R_f + R_L} \quad \text{(half-wave rectifier)} \quad (3.23)$$

$$I_{dc} = \frac{2V_{max}}{\pi(R_f + R_L)} \cos \theta_1 - \frac{\pi - 2\theta_1}{\pi} \frac{V_\gamma}{R_f + R_L} \quad \text{(full-wave rectifier)} \quad (3.24)$$

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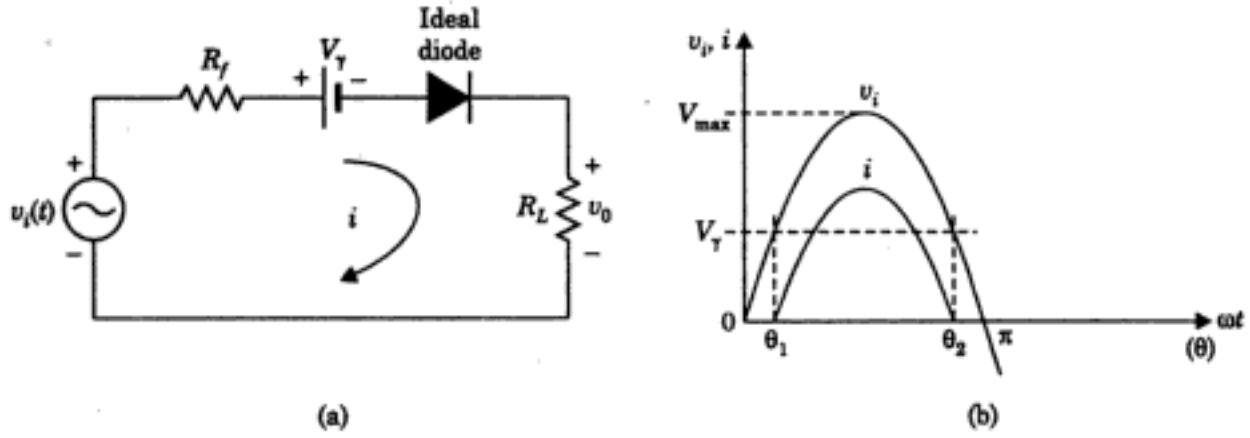


Fig. 3.8 (a) Equivalent circuit of a rectifier. The diode is represented by its large-signal model parameters, R_f, V_γ and an ideal diode. (b) The waveforms for the input voltage v_i and load current i, the ignition angle is θ_1 and extinction angle is θ_2.

EXAMPLE 3.2

Verify Eqs. (3.23) and (3.24).

Solution Clearly,

$$\theta_1 = \sin^{-1} \frac{V_\gamma}{V_m}$$

$$\theta_1 = \pi - \theta_1$$

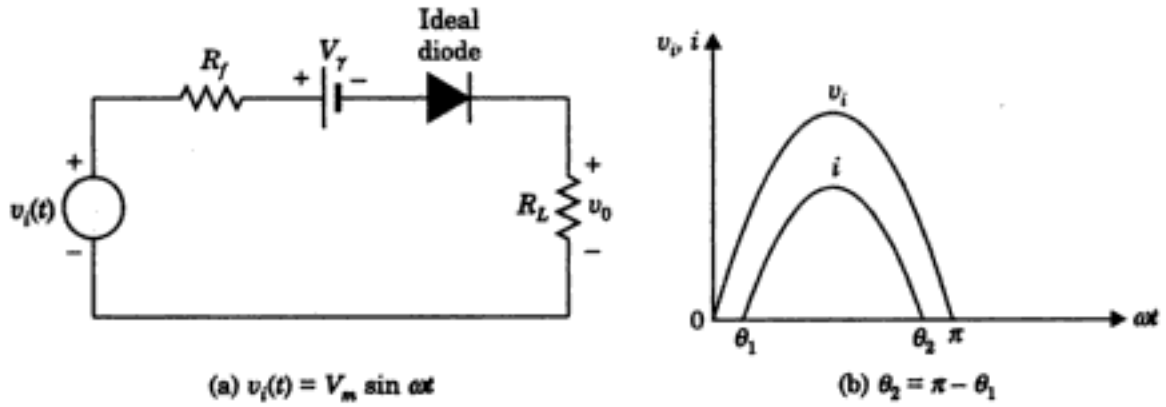


Fig. 3.9 (a) Equivalent circuit of a rectifier (b) Waveforms v_i and i, for Ex. 3.2 (half-wave rectifier).

(a) *Half-wave rectifier*

During conduction

$$i = \frac{(v_i - V_\gamma)}{(R_f + R_L)}$$

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$$\therefore \quad i(t) = \begin{cases} \dfrac{(V_m \sin \omega t - V_\gamma)}{(R_f + R_L)} & \theta_1 \le \omega t \le \pi - \theta_1 \\ 0, \quad \text{otherwise,} & \text{(for half-wave rectifier case)} \end{cases}$$

Then average current is given by

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i(t)\, d(\omega t)$$

$$= \frac{1}{2\pi}\frac{1}{R_f + R_L}\left[\int_{\theta_1}^{\pi-\theta_1} (V_m \sin \omega t - V_\gamma)\, d(\omega t)\right]$$

$$= \frac{1}{2\pi}\frac{1}{R_f + R_L}\left[-V_m \cos \omega t\right]_{\omega t=\theta_1}^{\pi-\theta_1} - \frac{V_\gamma}{2\pi(R_f + R_L)}\left[\omega t\right]_{\omega t=\theta_1}^{\pi-\theta_1}$$

$$= \frac{2V_m \cos \theta_1}{2\pi\,(R_f + R_L)} - \frac{V_\gamma}{2\pi(R_f + R_L)}(\pi - \theta_1 - \theta_1)$$

$$\therefore \quad I_{dc} = \frac{V_m}{\pi(R_f + R_L)}\cos\theta_1 - \frac{(\pi - 2\theta_1)}{2\pi}\frac{V_\gamma}{R_f + R_L}$$

Therefore, Eq. (3.23) is verified. Q.E.D.

[*Note.* Q.E.D. = Quod Erat Demonstrandum which is a Latin abbreviation meaning "which was to be proved".]

(b) *Full-wave Rectifier*

Figure 3.9(c) shows the circuit of a full-wave rectifier. Fig. 3.9(d) shows the waveform of input voltage $v_i = V_{max} \sin \omega t$ and the conduction current $i = i_1 + i_2$.

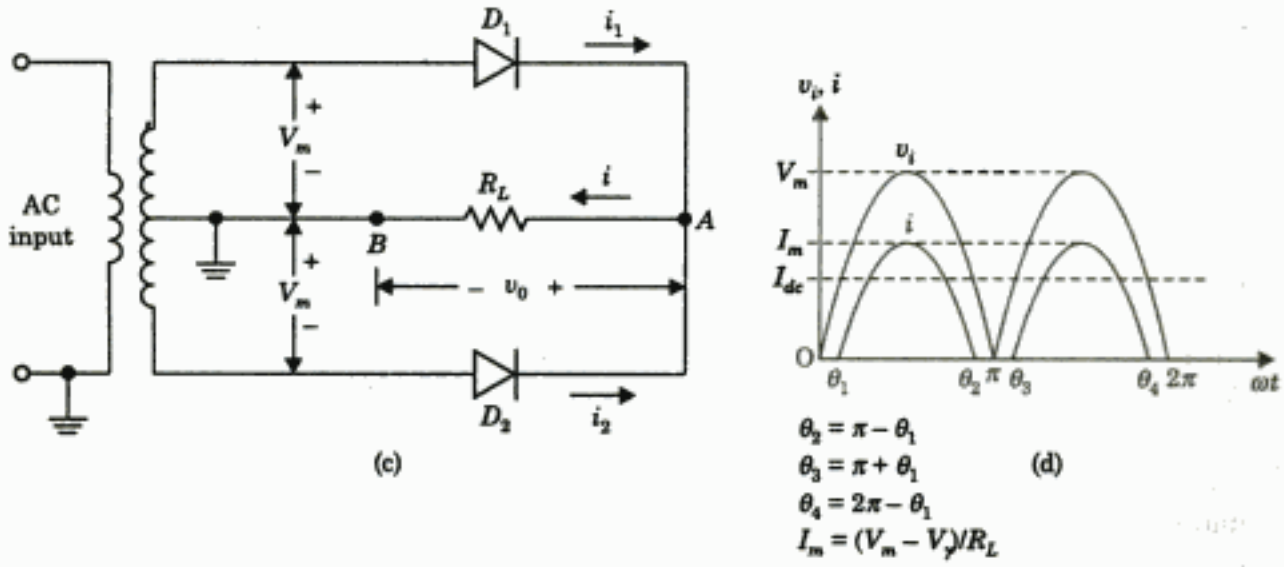


Fig. 3.9 (c) A full-wave rectifier, (d) Diode current, i_1 and i_2, $v_0 = iR_L$, for Ex. 3.2 (full-wave rectifier).

Here
$$i(t) = \begin{cases} \dfrac{(V_m \sin \omega t - V_\gamma)}{(R_L + R_f)}, & \theta_1 \le \omega t \le \theta_2 \\ \dfrac{[V_m \sin(\omega t - \pi) - V_\gamma]}{(R_L + R_f)}, & \theta_3 \le \omega t \le \theta_4 \end{cases}$$

$\therefore$ I_{dc} = Average of $i(t)$ over $\omega t = 0$ to 2π

$$= \frac{1}{2\pi}\int_0^{2\pi} i(t)\, d\omega t$$

$$= \frac{1}{2\pi(R_L + R_f)}\left[\int_{\theta_1}^{\pi-\theta_1} (V_m \sin \omega t - V_\gamma)\, d(\omega t) + \int_{\pi+\theta_1}^{2\pi-\theta_1} [V_m \sin(\omega t - \pi) - V_\gamma]\, d(\omega t)\right]$$

$$= \frac{1}{2\pi(R_L + R_f)}\left[\left\{-V_m \cos \omega t - V_\gamma(\omega t)\right\}_{\omega t=\theta_1}^{\pi-\theta_1} + \left\{-V_m \cos(\omega t - \pi) - V_\gamma(\omega t)\right\}_{\omega t=\pi+\theta_1}^{2\pi-\theta_1}\right]$$

$$= \frac{1}{2\pi(R_L + R_f)}[\{2V_m \cos\theta_1 - V_\gamma(\pi - 2\theta_1)\} + \{2V_m \cos\theta_1 - V_\gamma(\pi - 2\theta_1)\}]$$

$$= \frac{1}{\pi(R_L + R_f)}[2V_m \cos\theta_1 - (\pi - 2\theta_1)V_\gamma]$$

$\therefore$ $$I_{dc} = \frac{2V_{max}}{\pi(R_f + R_L)}\cos\theta_1 - \frac{\pi - 2\theta_1}{\pi}\cdot\frac{V_\gamma}{R_f + R_L}$$ (as expected) Q.E.D.

Hence Eq. (3.24) is proved.

Peak inverse voltage (PIV): For each rectifier circuit, there is a maximum voltage to which the diode can be subjected. This potential is called **peak inverse voltage (PIV)**. It occurs during that part of the cycle *when the diode is non-conducting.*

For a half-wave rectifier (see Fig. 3.3) the PIV is clearly V_{max}. When D is OFF and v_i is $-V_{max}$, diode D has reverse voltage applied across to it is V_{max}.

For a full-wave rectifier (see Fig. 3.10), when D_1 is conducting and D_2 is OFF, assume $R_f \to 0$. Hence we may short D_1.

Potential $V_A = V_P = V_{max}$; and Potential $V_Q = -V_{max}$

$\therefore$ $V_{AQ} = 2V_{max}$

When V_{PB} is V_{max} then diode D_2 has PIV of $2V_{max}$. In a full-wave circuit, the peak inverse voltage across each diode is twice the maximum transformer voltage measured from midpoint to either end, i.e., PIV = $2V_{max}$ in Fig. 3.10. For safe operation of diodes so that these do not puncture at peak inverse voltage, we must choose a diode having PIV higher than the circuit produces in the rectifiers. The value of PIV is usually indicated in the data sheet of the diode.

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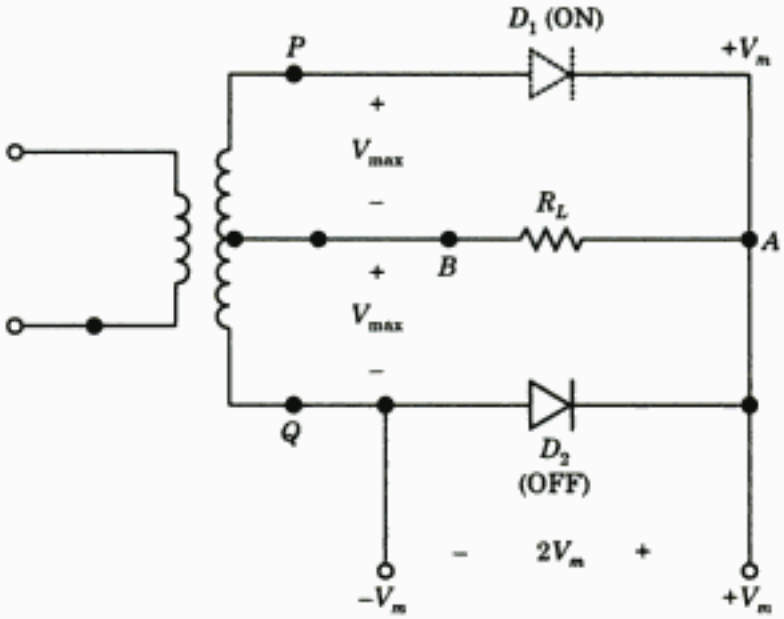


Fig. 3.10 Full-wave rectifier D_1 is ON, D_2 is OFF. Voltage across D_2 is $2V_{max}$. (PIV) We have assumed $V_\gamma = 0$ and $R_f = 0$. When D_1 is short (due to conduction) $V_A = V_P = +V_{max}$. Also, D_2 is OFF (no conduction), hence $V_Q = -V_{max}$.

3.2.3 Other Full-wave Rectifiers

Besides two-diode rectifier discussed earlier, there are a variety of other rectifiers. Also, there are several types of voltage doubling and various types of voltage-multiplying circuits. Bridge circuit (a full-wave rectifier) is very popular and is used in power circuits. It also can be used in AC meters when the AC signal contains a fairly wide range of frequencies.

The bridge rectifier: Here we use 4 diodes D_1, D_2, D_3 and D_4, as shown in Fig. 3.11. Each one has the same cut-in voltage V_γ and the same forward resistance R_f. Here two diodes, say D_1 and D_3 (or D_2 and D_4) conduct simultaneously. Let V_{AB} be +ve and greater than $2V_\gamma$ then the current i_1 is given by (solid lines)

$$i_1 = \frac{V_{AB} - 2V_\gamma}{2R_f + R_L} \quad \text{or} \quad i_1 = \frac{V_{max} \sin \omega t - 2V_\gamma}{2R_f + R_L} \tag{3.25}$$

Similarly, when V_{AB} is negative (i.e., point A is –ve w.r.t. B), and V_{BA} greater than $2V_\gamma$ then the current i_2 is given by (broken lines)

$$i_1 = \frac{V_{BA} - 2V_\gamma}{2R_f + R_L} \quad \text{or} \quad i_2 = \frac{V_{max} \sin \omega t - 2V_\gamma}{2R_f + R_L} \tag{3.26}$$

Figure 3.12 shows the input voltage v_{AB} ($= V_{max} \sin \omega t$) and the currents i_1 and i_2. Note that i_1 and i_2 are AC, half cycle currents, each being equal if we assume all the diodes D_1, D_2, D_3 and D_4 identical. These currents are +ve and –ve implying that they flow in the opposite directions as far as the transformer winding AB is concerned. However, they flow in the same directions in the load Z_L as seen in Fig. 3.11 and redrawn in Fig. 3.13.

It is now clear that the currents flowing in the load Z_L, though half cycles shape, have a DC average as shown in the following calculations.

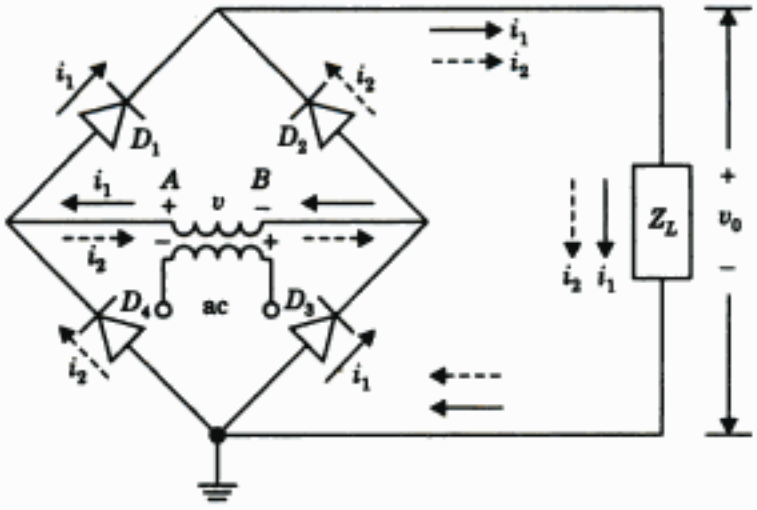


Fig. 3.11 A full-wave bridge rectifier solid line current when V_{AB} is positive, broken line current when V_{AB} is negative.

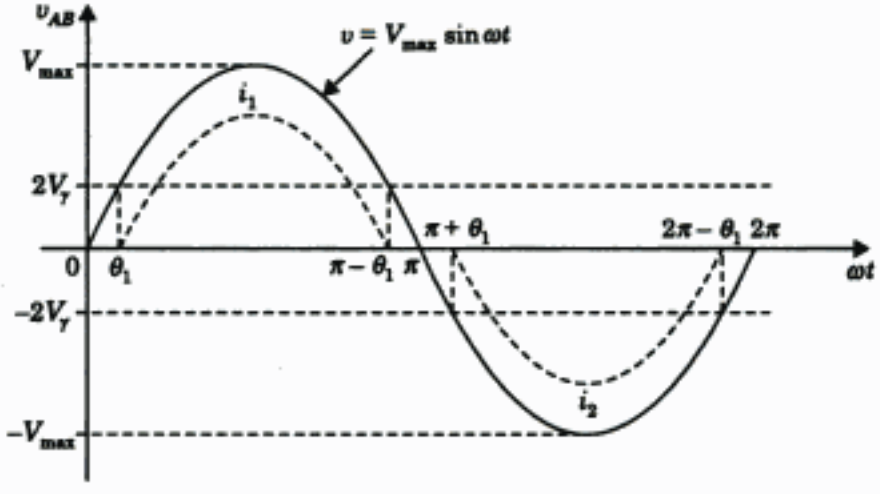


Fig. 3.12 Voltage $v = V_{max} \sin \omega t$ and currents i_1 and i_2 flowing through D_1, D_3, and D_2, D_4.

Calculation of I_{dc} in a bridge rectifier: The derivation of I_{dc} here is similar as was for the case of full-wave rectifier (see **Example 3.2**). This is so because the current i shown in Fig. 3.13 for the bridge rectifier resembles the current i in Fig. 3.5(b) for the full-wave rectifier. [only θ_1 has been taken zero in Fig. 3.5(b)].

I_{dc} = Average of $i(= i_1 + i_2)$ from $\omega t = 0$ to $\omega t = 2\pi$

= Average of i_1 only for $\omega t = 0$ to $\omega t = \pi$ ($\because$ $i_1 = i_2$ in shape)

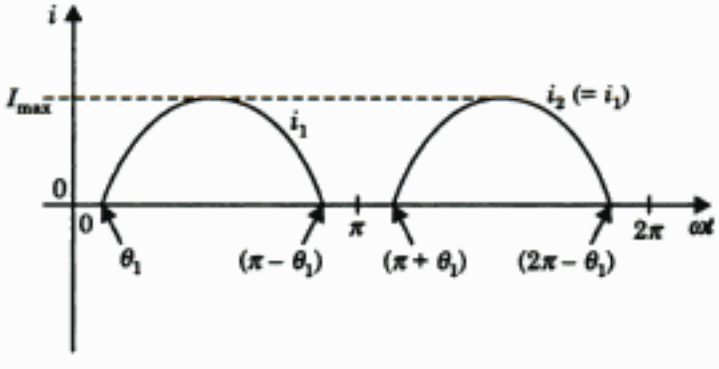


Fig. 3.13 Currents in Fig. 3.12 redrawn as these flow in the load Z_L (i.e., in the same direction) for the case of a bridge rectifier.

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The conduction in diodes D_1 and D_3 requires that the value of input voltage v must be greater than $2V_\gamma$. Also, during conduction of D_1 and D_3. $2R_f$ resistance of these two diodes is in the path of current i_1. Hence we can write

At θ_1 $$v = 2V_\gamma$$

$\therefore$ $$V_{max} \sin\theta_1 = 2V_\gamma$$

or $$\theta_1 = \sin^{-1}\frac{2V_\gamma}{V_{max}} \tag{3.27}$$

$$i_1 = \frac{v - 2V_\gamma}{2R_f + R_L} = \frac{V_{max}\sin\omega t - 2V_\gamma}{2R_f + R_L}$$

During the one cycle period (i.e. $\omega t = 0$ to 2π), each current i_1 and i_2 contributes the same value of average dc current. Hence, we can say average of i = average of $(i_1 + i_2) = 2 \times$ average of i_1. Hence we can write

or $$I_{dc} = \frac{1}{\pi}\int_{\theta_1}^{\pi-\theta_1} i_1\, d(\omega t)$$

$$= \frac{1}{\pi(2R_f + R_L)}\int_{\theta_1}^{\pi-\theta_1}(V_{max}\sin\omega t - 2V_\gamma)\, d(\omega t)$$

i.e. $$I_{dc} = \frac{1}{\pi(2R_f + R_L)}\left[-V_{max}\cos\omega t - 2V_\gamma(\omega t)\right]_{\theta_1}^{\pi-\theta_1}$$

$$= \frac{1}{\pi(2R_f + R_L)}\left[2V_{max}\cos\theta_1 - 2V_\gamma(\pi - 2\theta_1)\right]$$

$\therefore$ $$I_{dc} = \frac{2V_{max}\cos\theta_1}{\pi(2R_f + R_L)} - \frac{2V_\gamma(\pi - 2\theta_1)}{\pi(2R_f + R_L)} \tag{3.28}$$

Note that if we change R_f to $2R_f$ and V_γ to $2V_\gamma$ in Eq. (3.24) of full-wave rectifier case, we readily obtain the above value of I_{dc} given in Eq. (3.28) for the bridge rectifier. This is understandable, because whenever current i_1 or i_2 flows in the bridge rectifier, there are two diodes in series (either D_1, D_3 or D_2, D_4) instead of one diode as is in the case of full-wave rectifier. Also here $\theta_1 = \sin^{-1}(2V_\gamma/V_{max})$ and it was $\sin^{-1}(V_\gamma/V_{max})$ is full-wave rectifier discussed earlier.

Advantages of bridge rectifier over the full-wave rectifier:

1. There is no need of centre tapped transformer as the full secondary winding is in use for each current i_1 and i_2.
2. The transformer needed here is lighter in weight, as its secondary winding is half the size of secondary winding of the full-wave rectifier case.
3. The peak inverse voltage (PIV) of each diode used here is only V_{max} and (not $2V_{max}$ as was for the case of full-wave rectifier). Thus, the diodes D_1, D_2, D_3 and D_4 are less expensive (compared to the diodes D_1 and D_2 of the full-wave rectifier).

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4. Even if two diodes either D_1, D_3 or D_2, D_4 become defective, the bridge rectifier continues to act as a rectifier with the remaining two diodes, though a half-wave type. In case of full-wave rectifier if one diode open circuits, the rectifier functions as a half-wave rectifier, but if both its diodes D_1 and D_2 become defective it totally fails.

Disadvantages of a bridge rectifier

1. It is costlier as compared to the two-diode type full-wave rectifier as it requires 4 diodes.
2. The four diodes must all be identical (same V_γ and R_f). If one diode fails, one may not be able to procure a similar one, it might become necessary to replace all the four diodes.

Ripple Factor (r): It is seen that for rectification, we convert AC voltage to series of unidirectional half cycles, such as shown in Fig. 3.3(c) (where alternate half cycle of current i is zero) or Fig. 3.5(b) (where each –ve half cycle has been converted into +ve half cycle). Thereafter, we calculate the value of DC current as the average of such unidirectional (usually all +ve) half cycles of current. In practice, the unidirectional half cycles contain, besides the DC value, (which we call DC) many harmonics. We determine the amplitudes of such harmonics by Fourier analysis by using formulas similar to indicated by Eq. (3.3) and Eq. (3.4). The rms values of such ripples/harmonics indicate how much impure the output DC value is. If there are no harmonics in the output, the average value of the output is purely DC and is ripple free. However, if there are harmonic contents in the output (as is the usual case), the output is not a pure DC but DC + unwanted ripples.

In many applications, a residual pulsation in the output DC is not desirable. A measure of the purity of the DC output is called the **ripple factor** r, and is defined as:

$$\textbf{Ripple factor, } r = \frac{\text{rms value of AC component}}{\text{Average value of wave}} \tag{3.29}$$

We may write

$$r = \frac{I'_{\text{rms}}}{I_{dc}} = \frac{V'_{\text{rms}}}{V_{dc}}$$

where I'_{rms} and V'_{rms} denote the rms values of the AC components of the current and voltage, respectively. As the instantaneous AC component (i.e., ripple current) of the current is given by

$$i' = i - I_{dc} \qquad \left(I_{dc} = \text{Average of } i = \frac{1}{2\pi}\int_0^{2\pi} i\, d(\omega t)\right) \tag{3.30}$$

$$\therefore \quad (I'_{\text{rms}})^2 = \frac{1}{2\pi}\int_0^{2\pi} (i - I_{dc})^2\, d(\omega t)$$

$$= \frac{1}{2\pi}\int_{\omega t=0}^{2\pi} (i^2 - 2iI_{dc} + I_{dc}^2)\, d(\omega t)$$

$$= I_{\text{rms}}^2 - 2I_{dc}I_{dc} + I_{dc}^2 \qquad \left(\because \frac{1}{2\pi}\int_0^{2\pi} i\, d(\omega t) = I_{dc}\right)$$

$$= (I_{dc})^2\left[\frac{I_{\text{rms}}^2}{I_{dc}^2} - 1\right]$$

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$$\therefore \quad I'_{rms} = I_{dc}\sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$\therefore \quad r = \frac{I'_{rms}}{I_{dc}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \tag{3.31}$$

For half-wave rectifier

$$I_{rms} = \frac{I_{max}}{2} \qquad (\because \text{ current is zero during half-wave})$$

$$I_{dc} = \frac{I_{max}}{\pi}$$

$$\therefore \quad \frac{I_{rms}}{I_{dc}} = \frac{\pi}{2}$$

$$\therefore \quad r = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = \sqrt{(1.57)^2 - 1} = 1.21 \tag{3.32}$$

For half-wave rectifiers, the ripple voltage exceeds the DC output voltage. Hence half-wave rectifier is a poor circuit for conversion of AC to DC.

For full-wave rectifier

$$I_{rms} = \frac{I_{max}}{\sqrt{2}}$$

$$I_{dc} = \frac{2}{\pi} I_{max}$$

$$\therefore \quad \frac{I_{rms}}{I_{dc}} = \frac{\pi}{2\sqrt{2}} = 1.1107$$

$$\therefore \quad r = \sqrt{(1.1107)^2 - 1} = \sqrt{0.2337} = 0.483 \tag{3.33}$$

Thus, for the full-wave rectifier, the ripple factor drops from 1.21 (half-wave rectifier) to 0.483.

Rectifier efficiency (η_r): Rectifier efficiency η_r is a figure used as a measure of merit to compare the rectifiers. η_r is defined as:

$$\eta_r = \frac{\text{DC power delivered to the load}}{\text{AC input power from transformer secondary}} \tag{3.34}$$

$$= \frac{P_{dc}}{P_{ac}}$$

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For full-wave rectifier

$$P_{dc} = I_{dc}^2 R_L = \left(\frac{2}{\pi} I_{\max}\right)^2 R_L$$

But $$P_{ac} = \left(\frac{I_{\max}}{\sqrt{2}}\right)^2 (R_f + R_L), \text{ i.e., } I_{\text{rms}}^2 (R_f + R_L)$$

$$\therefore \quad \eta_r = \frac{\left(\frac{2}{\pi}\right)^2 I_{\max}^2 R_L}{\left(\frac{R_f + R_L}{2} I_{\max}^2\right)}$$

$$= \frac{8}{\pi^2} \cdot \frac{1}{1 + (R_f / R_L)}$$

$$= \frac{8}{\pi^2} = 0.8105 \text{ for } R_f \to 0 \tag{3.35}$$

For half-wave rectifier

$$I_{dc} = \frac{I_{\max}}{\pi}, \; P_{dc} = (I_{dc})^2 R_L = (I_{\max}/\pi)^2 R_L$$

$$P_{ac} = \frac{1}{2} P_{ac \text{ (full-wave case)}} = \frac{1}{2}\left(\frac{I_{\max}}{\sqrt{2}}\right)^2 (R_f + R_L) \tag{3.36}$$

$$\eta_r = \frac{(I_{\max}/\pi)^2 R_L}{\frac{1}{2}\left(\frac{I_{\max}}{\sqrt{2}}\right)^2 (R_f + R_L)}$$

$$= \frac{4}{\pi^2} \frac{1}{(1 + R_f / R_L)} = \frac{4}{\pi^2} \text{ for } R_f \to 0$$

Hence, $$\eta_r \big|_{\text{half-wave rect.}} = \frac{1}{2} \eta_r \Big|_{\text{full-wave rect.}} \tag{3.37}$$

EXAMPLE 3.3

The efficiency of rectification η_r is defined as the rates of the DC output power, $P_{dc} = V_{dc} I_{dc}$ to the input power $P_i = \frac{1}{2\pi} \int_0^{2\pi} v_i \, i \, d\alpha$.

(a) Show that, for the half-wave rectifier circuit,

$$\eta_r = \frac{40.6}{1 + (R_f / R_L)} \%$$

(b) Show that, for the full-wave rectifier, η_r has twice the value given in part (*a*).

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Solution

(a) $$P_{dc} = I_{dc}^2 R_L = \left(\frac{I_{max}}{\pi}\right)^2 R_L \qquad \text{(for half-wave rectifier)}$$

$$P_i = \frac{1}{2}\left(\frac{I_{max}^2}{2}\right)(R_f + R_L) \qquad \text{(AC input power)}$$

$\therefore$ $$\eta_r = \frac{P_{dc}}{P_i} = \frac{(I_{max}^2/\pi^2)R_L}{(I_{max}^2/4)(R_f + R_L)}$$

$$= \frac{4}{\pi^2}\frac{R_L}{R_f + R_L}$$

$$= (0.40528)\frac{1}{1 + (R_f/R_L)}$$

$$= \frac{40.528}{1 + (R_f/R_L)}\% \qquad \text{Q.E.D.}$$

(b) Here, for full-wave rectifier

$$\eta_r = \frac{P_{dc}}{P_{ac}} = \frac{\left(\frac{2}{\pi} I_{max}\right)^2 R_L}{(I_{max}^2/2)(R_f + R_L)} = \frac{8}{\pi^2}\frac{R_L}{(R_f + R_L)}$$

$$= (0.816)\frac{R_L}{R_f + R_L} = \frac{81.6}{1 + (R_f/R_L)} \qquad \textbf{Ans.}$$

Hence η_r is twice the value found is part (a).

EXAMPLE 3.4

A two-diode type full-wave rectifier is inputted from the secondary winding of the transformer giving 40-0-40 V_{rms}. Each diode has forward conducting resistance R_f = 1 Ω and assume V_γ = 0. The load resistance is 29 Ω (see Fig. 3.14). Determine:

(a) DC load current I_{dc}
(b) DC power in load P_{dc}
(c) Rectification efficiency η
(d) percentage regulation
(e) PIV of each diode.

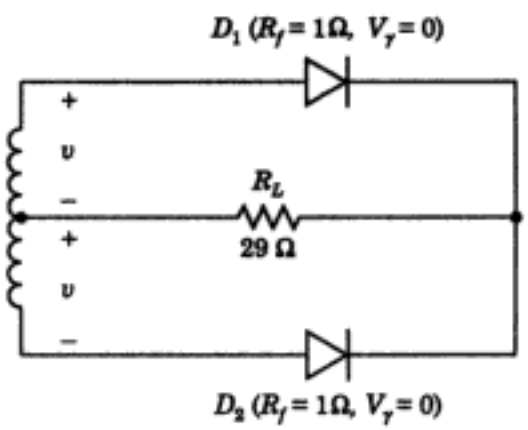


Fig. 3.14 The circuit of the rectifier, in Ex. 3.4.

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Solution Here $v = (\sqrt{2} \cdot 40) \sin \omega t$

$\therefore$ $V_{max} = 40\sqrt{2} = 56.57$ V

and $$I_{max} = \frac{V_{max}}{(R_f + R_L)}$$

$$= \frac{56.75}{1 + 29} = 1.8856 \text{ A}$$

(a) $I_{dc} = \frac{2}{\pi} I_{max} = \frac{2}{\pi}(1.8856) = 1.200$ A **Ans.**

(b) $P_{dc} = I_{dc}^2 R_L = (1.200)^2 \times 29 = 41.789$ W **Ans.**

(c) $\eta = \frac{P_{dc}}{P_{ac}}$

Here $$P_{ac} = \frac{V_{rms}^2}{(R_f + R_L)} = \frac{40^2}{1 + 29} = 53.33 \text{ W}$$

$\therefore$ $$\eta = \frac{41.789}{53.33} = 0.7836 = 78.36\%$$ **Ans.**

(Check, $\eta = 81.6 \Big/ \left(1 + \frac{R_f}{R_L}\right) = 81.6 \Big/ \left(1 + \frac{1}{29}\right) = 78.88\%$, almost same as above value)

(d) The equivalent (Thevenin) circuit of the rectifier is shown in Fig. 3.15

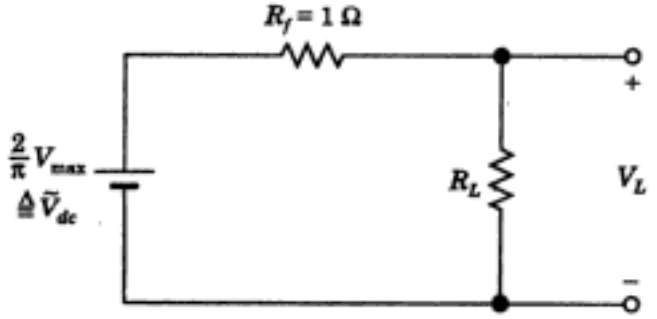


Fig. 3.15 Thevenin equivalent circuit of Ex. 3.4.

$$\bar{V}_{dc} = \frac{2}{\pi} \times \sqrt{2} \times 40 = 36.013 \text{ V} \qquad (\because V_{max} = \sqrt{2} \times 40)$$

$$I_{load} = I_{dc} = 1.200 \text{ A}$$

$\therefore$ $$V_{load} = V_{dc} = 29 \times 1.200 = 34.8 \text{ V}$$

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Now, $$\text{Regulation} = \frac{V_{\text{no load}} - V_{\text{load}}}{V_{\text{load}}}$$ **

$$= \frac{36.013 - 34.8}{34.8} = 3.48\% \quad \textbf{Ans.}$$

(Had we defined regulation by $(V_{\text{no load}} - V_{\text{load}})/V_{\text{no load}}$, we would have obtained regulation = (36.013 – 34.8)/36.013 = 3.36%)

(e) PIV = $2V_{\max}$ in the case for each diode

$= 2 \times 56.57 = 113.14$ V **Ans.**

Note: $$\text{Ripple factor} = \left[\left(\frac{I_{\text{rms}}}{I_{dc}}\right)^2 - 1\right]^{1/2}$$

Here, $$I_{\text{rms}} = \frac{V_{\text{rms}}}{(R_f + R_L)} = \frac{40}{(1+29)} = \frac{4}{3}\text{ A}$$

$I_{dc} = 1.2$ A (from (a))

$\therefore$ $$\text{Ripple factor} = \sqrt{\left(\frac{4/3}{1.2}\right)^2 - 1} = 0.483 = 48.3\%$$ as expected, for a full-wave rectifier.

EXAMPLE 3.5

A full-wave Bridge rectifier with 120 V-rms sinusoidal input has a load resistor of 1 kΩ.

(a) If Silicon diodes are employed, what is the DC voltage available at the load?

(b) Determine the required PIV rating of each diode.

(c) Find the maximum current through each diode during conduction.

(d) What is the required power rating of each diode?

Assume $V_\gamma = 0.7$ V, and $R_f = 0$

Solution For Silicon diodes, $V_\gamma = 0.7$ V.

(a) $$V_{\max} = \sqrt{2}\, V_{\text{rms}} = \sqrt{2} \times 120 = 169.7\text{ V}$$

$$I_{\max} = \frac{(V_{\max} - 2 \times 0.7)}{R_L} = \frac{(169.7 - 2 \times 0.7)}{1} = 168.3\text{ mA}$$

$$I_{dc} = \frac{2}{\pi} I_{\max} = \frac{2}{\pi} \times 168.3 = 107.14\text{ mA}$$

$$V_{dc} = I_{dc} R_L = 107.14 \times 1 = 107.14\text{ V} \quad \textbf{Ans.}$$

**Or directly % regulation $= \frac{R_f}{R_L} \times 100 = \frac{1}{29} \times 100 = 3.448\%$.

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(b) PIV rating = V_{max} = 169.7 V **Ans.**

(c) Maximum current through diode = I_{max} = 168.3 mA **Ans.**

(d) Diode power rating $P_{max} = V_D I_{D\,max}$ (where $V_D = V_\gamma = 0.7$ V here)

$$= 0.7 \times 168.3 = 117.81 \text{ mW} \quad \textbf{Ans.}$$

Note:
$$\eta = \frac{\text{Output power}}{\text{Input power}} = \frac{V_{dc} I_{dc}}{V_{rms} \cdot I_{rms}}$$

$$= \frac{107.14 \times (107.14 \times 10^{-3})}{120 \times (168.3/\sqrt{2}) \times 10^{-3}} = 0.8038 \equiv 80.4\%$$

(This is the ideal value of efficiency when $R_f = 0$)

Input ac power = $V_{rms} \times I_{rms} = 120 \times (168.3/\sqrt{2})$ mW

Output DC power = $\frac{V_{dc}^2}{R_L} = \frac{(107.14)^2}{10^3} = (107.14) \times (107.14)$ mW

$\therefore$ Power dissipated in 4 diodes = $\left(\frac{120 \times 168.3}{\sqrt{2}}\right) - 107.14 \times 107.14$

$$= 14280.73 - 11478.98 = 2801.75 \text{ mW}$$

$\therefore$ Power dissipated (average) in each diode = 700.44 mW

EXAMPLE 3.6

A centre-tapped full-wave rectifier has R_L = 1 kΩ. Each diode has a forward bias dynamic resistance r_d = 10 Ω. The voltage across half the secondary winding is 220 sin 314t. Find (a) Peak value of current, (b) DC value of current, (c) Ripple factor, (d) Rectification efficiency.

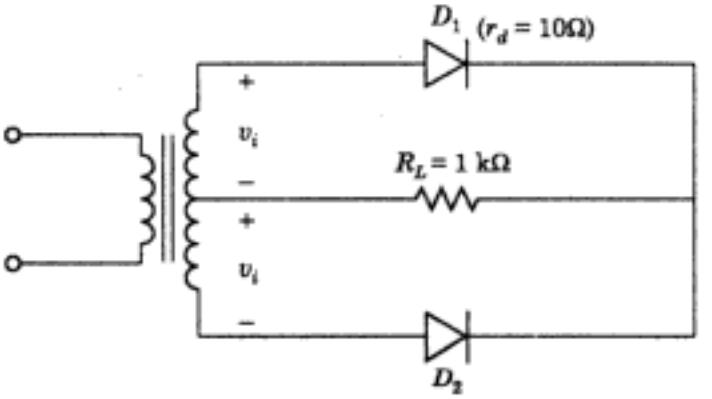


Fig. 3.16 Circuit diagram for Ex. 3.6

Solution Given data is (see Fig. 3.16)

R_L = 1 kΩ,

r_d = 10 Ω,

v_i = 220 sin 314t

(i) Peak value of current $I_{max} = \frac{V_{max}}{r_d + R_L}$.

$$= \frac{220}{10 + 1000} = 0.2178 \text{ A} \quad \textbf{Ans.}$$

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(ii) DC value of current $I_{dc} = \frac{2}{\pi} I_{max}$ (for a full-wave rectifier)

$$= \frac{2}{\pi} \times 0.2178 = 0.13866 \text{ A} \quad \textbf{Ans.}$$

(iii) Ripple factor $= \left[\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1\right]^{1/2}$ (From Eq. 3.31)

$$= \left[\left(\frac{I_{max}/\sqrt{2}}{I_{dc}}\right)^2 - 1\right]^{1/2}$$

$$= \left[\left(\frac{0.2178}{0.13866}\right)^2 \cdot \frac{1}{2} - 1\right]^{1/2} = 0.483 = 48.3\% \quad \textbf{Ans.}$$

(iv) Rectification efficiency $\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_{dc}^2 R_L}{\left(I_{max}/\sqrt{2}\right)^2 (r_d + R_L)}$

$$= \frac{2}{\left(\frac{I_{max}}{I_{dc}}\right)^2 \left(1 + \frac{r_d}{R_L}\right)} = \frac{2}{\frac{\pi^2}{4}\left(1 + \frac{r_d}{R_L}\right)}$$

$$= \frac{8}{\pi^2} \cdot \frac{1}{\left(1 + \frac{r_d}{R_L}\right)} = \frac{8}{\pi^2} \cdot \frac{1}{\left(1 + \frac{10}{1000}\right)} = \frac{0.81}{1 + 0.01} = 80.2\% \quad \textbf{Ans.}$$

3.2.4 The Rectifier Meter

This is a bridge rectifier system where no transformer is required. The voltage to be measured is applied through a limiting resistor R to two corners of the bridge.

A DC millimeter reads current through it. This is an average current. The meter is, however, scaled/calibrated to indicate rms values of a sinusoidal voltage applied to the input points. Thus this instrument will not read correctly when used with waveforms containing appreciable harmonics.

When point A is +ve w.r.t. point B, the diodes D_2 and D_3 conduct producing current shown upward in Fig. 3.17 when point A is –ve w.r.t. point B, then diodes

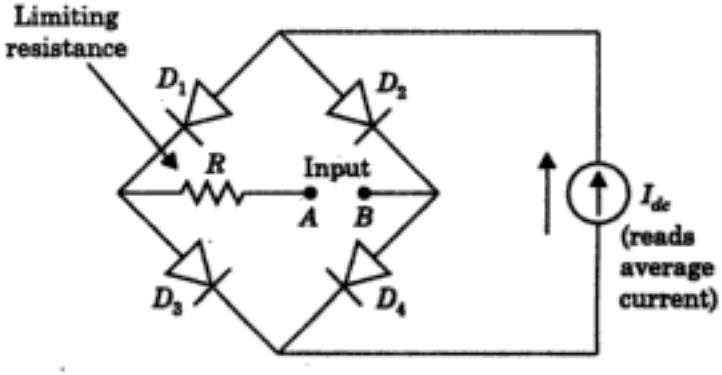


Fig. 3.17 The rectifier voltmeter.

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D_4 and D_1 conduct causing a current again in the same direction in the DC ammeter. In case of an AC input voltage across AB, I_{dc} is calculated as in the case of bridge rectifier. If the input voltage has several harmonics, each frequency content of the input voltage causes its own DC current part. The overall addition of all such DC currents may not represent the actual rms value of the input signal. Anyway, this meter is an inexpensive and robust voltage measuring device. By shunting the ammeter appropriately, the measurement voltage range can be earlier in creased.

EXAMPLE 3.7

A 1 mA DC meter whose resistance is 10 Ω is calibrated to read rms volts when used in a bridge circuit with semiconductor diodes. The effective resistance of each element may be considered to be zero in the forward direction and infinite in the reverse direction. The sinusoidal input voltage is applied in series with a 5-K resistance. What is the full-scale reading of this meter.

Solution Let the input voltage be

$$(\sqrt{2}\,V_{rms})\sin\omega t = V_{max}\sin\omega t$$

Then during conduction $$i_{ac} = \frac{v_{ac}}{R_L + R_f} = \frac{v_{ac}}{R_L} = \frac{V_{max}\sin\omega t}{R_L}$$

$\therefore$ $$I_{max} = \frac{V_{max}}{R_L} = \frac{\sqrt{2}\,V_{rms}}{R_L} = \frac{\sqrt{2}\,V_{max}}{5000 + 10}$$

(Here "R_L" = 5000 + 10 i.e. the total resistance in the current conduction path)

Now,

$$\text{DC current, } I_{dc} = \frac{2}{\pi} I_{max}$$

$$= \frac{2}{\pi}\frac{\sqrt{2}\,V_{rms}}{5010}\text{ A}$$

For full-scale reading, V_{rms} is such that I_{dc} = 1 mA.

(i.e. the given maximum current allowed in the ammeter)

$\therefore$ $$\frac{2}{\pi}\frac{\sqrt{2}V_{rms}}{5010} = 10^{-3}$$ (i.e., 1 mA current in the DC ammeter)

or $$V_{rms} = \frac{\pi \times 5010}{2\sqrt{2}} \times 10^{-3}$$

$$= 5.5647\text{ V}$$

The full-scale deflection (when meter passes 1 mA) corresponds to 5.5647 rms voltage values. **Aps.**

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EXAMPLE 3.8

A 5 mA DC ammeter whose resistance is 40 Ω is calibrated to read rms volts when used in bridge circuit with semiconductor diodes. Assuming ideal diodes, what is full-scale reading of this meter for the sinusoidal input voltage applied in series with a 20 kΩ resistance.

Solution The maximum (safe) current through the DC ammeter is 5 mA. Let the maximum voltage causing I_{DC} = 5 mA be V_{max}.

$$\therefore \quad V_{max} = \sqrt{2}\, V_{rms}$$

But
$$I_{DC} = \frac{V_{max}/(\pi/2)}{(20{,}000 + 40)}$$

$$\therefore \quad 5 \times 10^{-3} = \frac{(\sqrt{2}\, V_{rms}) \times \frac{2}{\pi}}{20040}$$

or
$$V_{rms} = (5 \times 10^{-3} \times 20040) \times \frac{\pi}{2} \frac{1}{\sqrt{2}}$$

$$= 111.294 \text{ V}$$

Thus, the full-scale deflection of the 5 mA DC ammeter is 111.294 rms value of the input AC voltage. **Ans.**

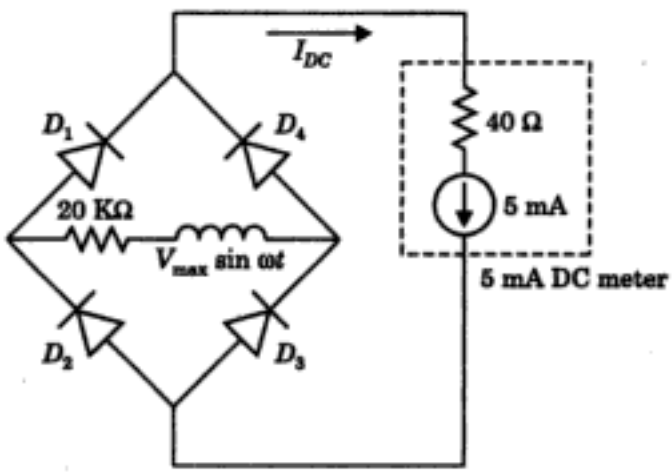


Fig. 3.18 The circuit showing metering arrangement of Ex. 3.8.

3.2.5 A Note on Charging and Discharging of a Capacitor

Charging of Capacitor: If the capacitor C is initially uncharged, i.e., $V_C = 0$ at $t = 0$ and we close the switch K at $t = 0$ (see Fig. 3.19), then we can prove that:

Voltage across C at any time t, $V_C = V(1 - e^{-t/RC})$ (3.38a)

Voltage across R at any time t, $V_R = V - V_C = Ve^{-t/RC}$ (3.38b)

As $t \to \infty$, $V_C \to V$ and $V_R \to 0$, i.e., current $I_{ch} \to 0$.

RC is called the **time constant**, and usually denoted by τ. If RC is very very small, V_C assumes voltage V in a very small time.

If the capacitor C holds an initial charge V_{CO} at $t = 0$ then after switch K is closed, the values of V_C and V_R are:

$$V_C = V_{CO} + (V - V_{CO})(1 - e^{-t/RC}) \tag{3.39a}$$

$$V_R = V - V_C = (V - V_{CO})e^{-t/RC} \tag{3.39b}$$

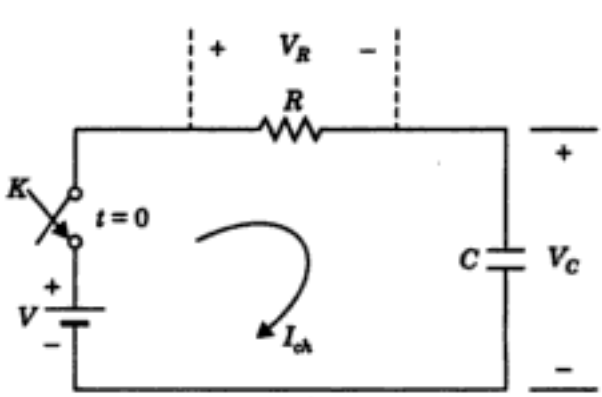


Fig. 3.19 Charging of capacitor C.

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Discharging of capacitor: Let the capacitor C be initially charged to voltage V_{CO}, and at time $t = 0$, the switch K is closed (see Fig. 3.20). Then the value of V_C and V_R at any time t is given by

$$V_C = V_{CO}\, e^{-t/RC} \qquad (3.40a)$$

$$V_R = -V_C = -V_{CO}\, e^{-t/RC} \qquad (3.40b)$$

If the time constant RC is very small, $V_C \to 0$ in a very small time (because $e^{-t/RC}\big|_{RC \text{ small}}$ decays very fast).

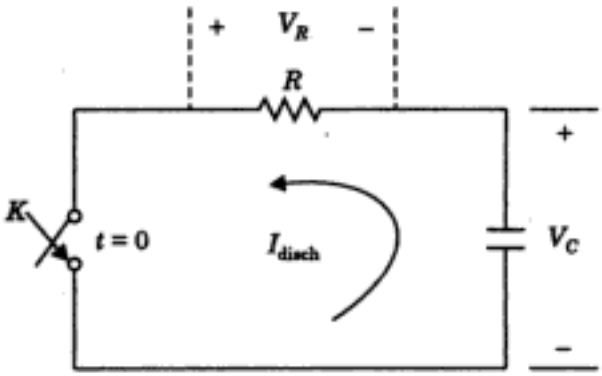


Fig. 3.20 Discharging of capacitor C. At $t = 0$, $V_C = V_{CO}$ (initial charge voltage)

If the time constant RC is very large, $V_C \approx V_{CO}$ for quite some time and only after large time t, V_C comes below V_{CO} substantially. The time constant RC can be made very very small if R is very small (as in case of forward conducting diode, where we shall see that $R = R_f$). So to charge C at a very fast rate we should have small value of R. Similarly, to discharge C slowly we should have large value of R.

3.3 CAPACITOR FILTERS

We have seen that the output from the rectifiers is not pure DC but half cycles, alternate half cycles for single phase half-wave rectifier and all half cycles (made +ve, i.e., rectified) in the case of full-wave rectifiers. The average of such half cycles is of course DC, but there are large number of ripples too. The DC supply voltages with ripples is not useful for driving many types of electronic devices. The circuit for battery chargers may have ripples with not so serious effects. But for some sophisticated electronic gadgets such as radio, tape recorder, TV or computer, pulsating (full of ripples) DC supplies are not acceptable. We need circuits to smoothen the rectified (full of ripples) output to a ripple free DC waveform, as shown in Fig. 3.21.

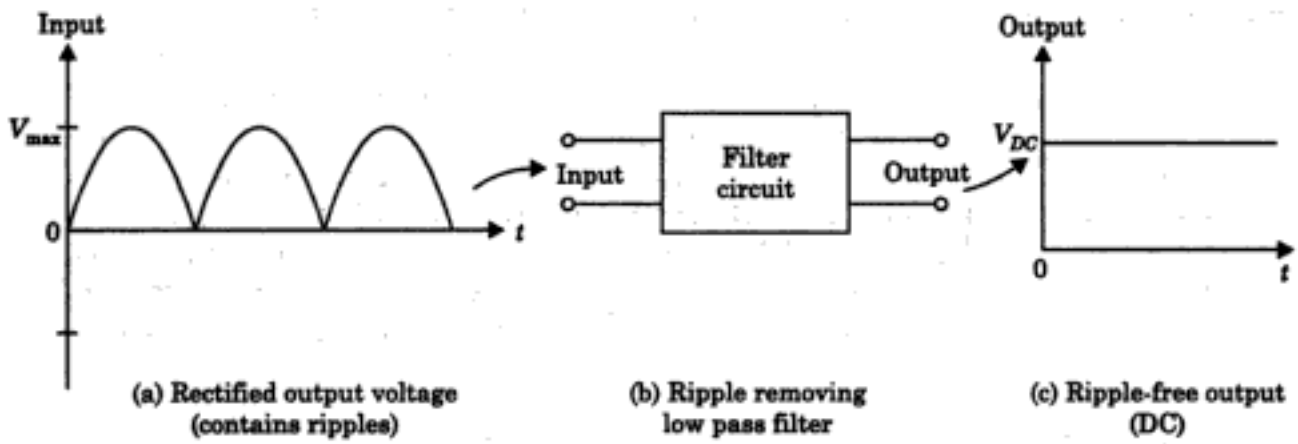


Fig. 3.21 Scheme of obtaining ripple-free output DC.

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The circuit of a typical filter is shown in Fig. 3.22, where a capacitor C has been added in parallel with the load resistance R_L.

The output voltage is smoothened by shunting the load R_L by the capacitor. The capacitor stores energy during the conduction period and delivers this energy to the load during the non-conducting period. This way the time during which the current passes through the load is prolonged and the ripple contents are reduced. The ripple voltage is defined as the deviation of the load voltage from its average DC value. Suppose $R_L = \infty$. The capacitor C charges to voltage V_m during conduction of the diode. Once diode is OFF, it assumes $R_r \approx \infty$ (the reverse resistance). Thus, V_C remains V_m even when the diode D is OFF. Thus, $v_0 = V_m$ is maintained. When the diode is OFF and $v_0 \approx +V_m$ and during this cycle with $v_i = -V_m$, the diode has peak inverse voltage of $2V_m$. Hence we must choose the diode with proper peak inverse voltage (PIV) rating to avoid damage of the diode.

In case the load R_L is not infinity but a specific value, it continues passing current due to the voltage v_0 across it. When diode is OFF, the capacitor C (holding voltage v_0 across it) continues supplying current to R_L. In other words, C discharges through R_L with time constant CR_L during diode D OFF period. During diode again conducting, the capacitor C regains its voltage to V_m. The diode acts as a switch which permits charge to flow into the capacitor when v_i exceeds v_0 (i.e., V_C), and then disconnects the power source when v_i is less than V_C.

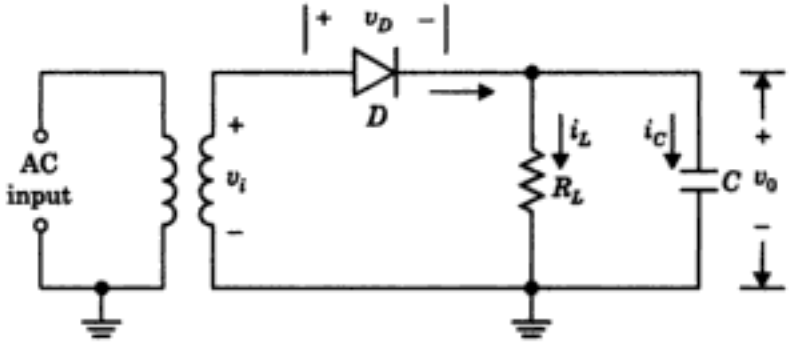


Fig. 3.22 Half-wave rectifier with a capacitor filter ($v_i = V_m \sin \omega t$).

Action of Capacitor C: To improve the output voltage $v_L = iR_L$, we put a smoothening capacitor across R_L as shown in Fig. 3.23.

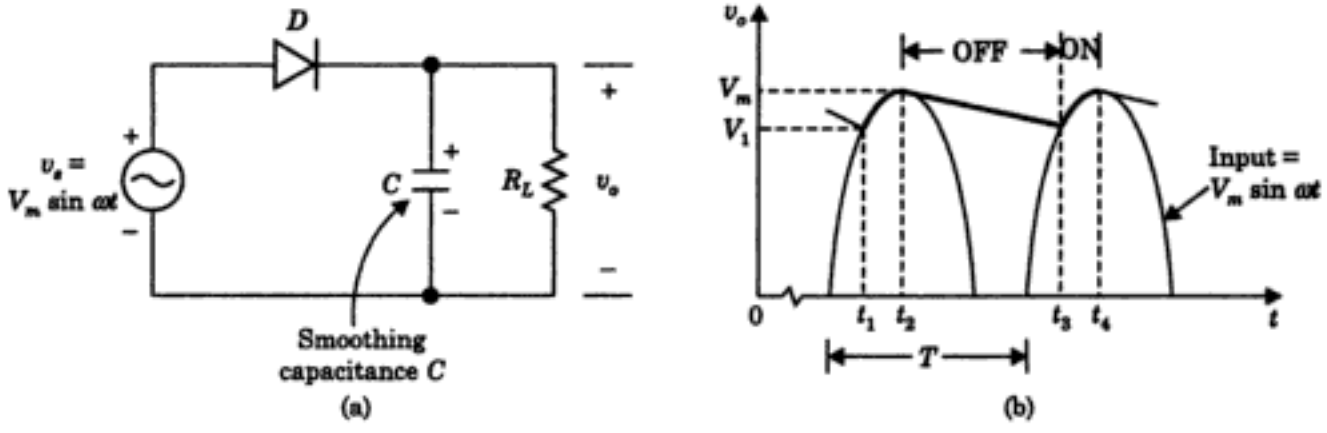


Fig. 3.23 (a) Rectifier with capacitor filter, (b) Output voltage of circuit in (a). From t_1 to t_2 or t_3 to t_4, diode D is ON and the capacitor C charges. From t_2 to t_3, diode D is OFF and the capacitor C discharges to load R_L.

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In the steady state, the voltage across the capacitor is V_1 such that V_1 is almost equal to the input voltage maxima (V_m).

At t_{1+} v_s is greater than V_1, the diode conducts and voltage across capacitor follows v_s till V_m is reached. Note that during the charging time (t_1 to t_2), C charges with time constant CR_f. As R_f (diode forward resistance) is very small, CR_f being very small, the charged voltage v_o almost follows the input voltage v_s during t_1 to t_2; v_o equals V_m at t_2.

At t_2 $V_m = v_0$ i.e., output equals the input peak voltage. The charging current becomes zero.

At t_{2+0} v_s is less than v_0, diode cuts OFF.

v_o decays through R_L such that

$v_0 = V_m e^{-(t-t_2)/R_L C}$ from t_2 to t_3. (see discharge path from t_2 to t_3 in Fig. 3.23(b)).

At t_3 $v_0 = v_s$, i.e., v_s has just equalled capacitor voltage.

At t_{3+0} v_s is greater than v_0. Diode conducts as was the case at t_{1+0}. This cycle continues.

The time constant $R_L C$ is chosen sufficiently large so that the discharge of C during diode OFF period is slow and it maintains a nearly constant voltage v_0 across C.

The above case assumes cut-in voltage $V_\gamma = 0$. If $V_\gamma \neq 0$, we have the circuit illustrated in Fig. 3.24.

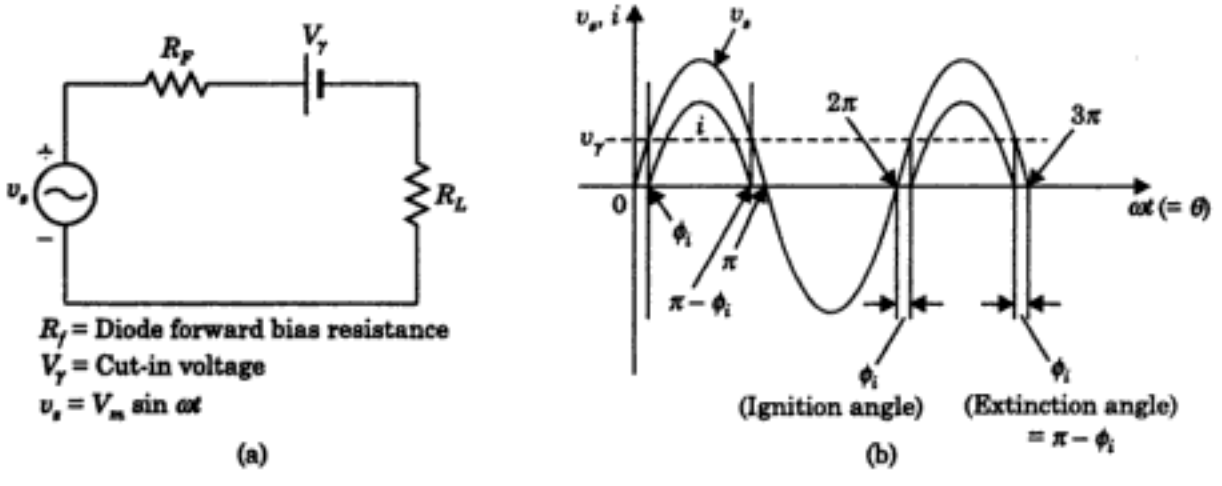


Fig. 3.24 (a) Rectifier equivalent circuit for $V_\gamma \neq 0$ and $R_f \neq 0$, (b) Current waveform showing ignition and extinction angles.

For forward bias,

$$i = \frac{v_s - V_\gamma}{(R_L + R_f)} = \frac{V_m \sin \omega t - V_\gamma}{R_L}, \; (R_f << R_L) \tag{3.41}$$

The current starts only when $V_m \sin \phi_i \geq V_\gamma$, i.e.,

$$\text{Ignition angle } \phi_i = \sin^{-1} \frac{V_\gamma}{V_m}$$

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Similarly, an extinction angle exists such that the diode stops conduction before v_s reaches zero value. Extinction starts when

$$v_s = V_m \sin \theta \leq V_\gamma$$

i.e., $$\sin \theta \leq \frac{V_r}{V_m}$$

$\theta = \phi_i$, gives ignition angle, and

$\theta = \pi - \phi_i$ gives extinction angle.

Thus, Ignition angle $$\phi_i = \sin^{-1} \frac{V_\gamma}{V_m} \quad (3.42a)$$

and Extinction angle $$= \pi - \phi_i = \pi - \sin^{-1} \frac{V_\gamma}{V_m} \quad (3.42b)$$

where V_γ is the cut-in voltage for the diode.

Output voltage under load: The diode D is ON (if we neglect the diode drop V_γ) when

$$v_i > V_C = v_0$$

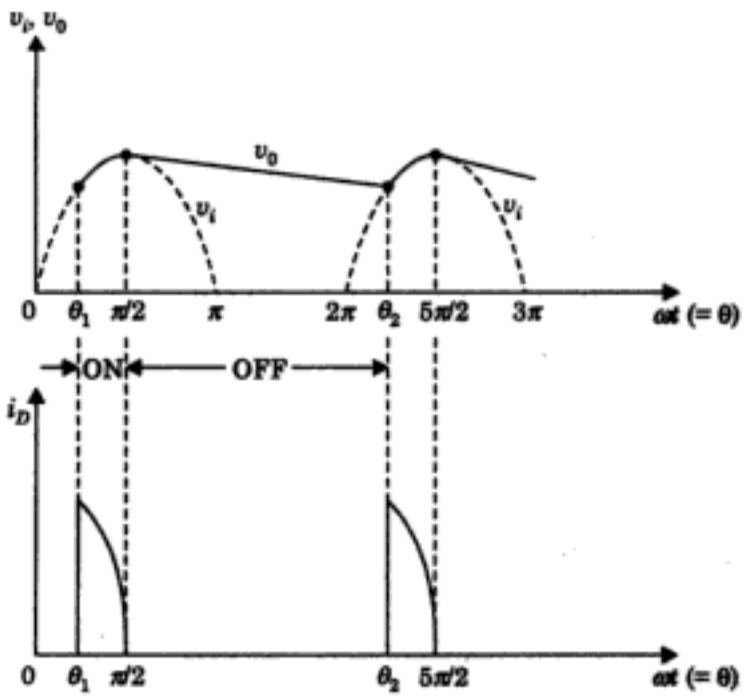


Fig. 3.25 (a) Sketches of input voltage v_i and output voltage v_0. (v_i is shown when D can conduct), (b) Diode current i_D.

In Fig. 3.22, when D conducts, the transformer voltage v_i is applied across the load R_L i.e. then

$$v_0 = V_m \sin \omega t$$

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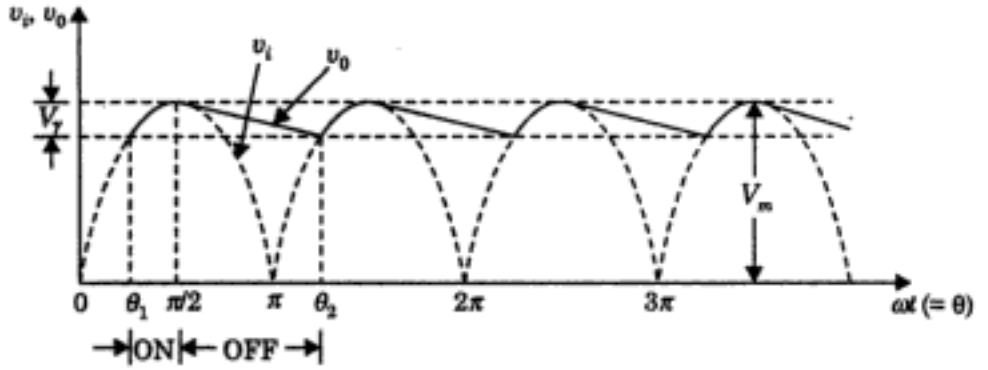


Fig. 3.26 Effect on output voltage by capacitor in a full-wave rectifier.

When diode is ON, the capacitor C regains its voltage V_C upto V_m. As soon as V_C exceeds v_i, the diode cuts OFF. Capacitor discharges through R_L with a time constant CR_L. The diode passes current from 'θ_1' to $\pi/2$ when D is ON. During D 'OFF' from $\pi/2$ to θ_2, C discharges

If we denote $\theta_1 = \omega t_1$ and $\theta_2 = \omega t_2$ then t_1 is cut-in time and t_2 is cut-out time.

The performance for a full-wave rectifier is shown in Fig. 3.26. If the capacitance C is made much larger, the current passage time ON decreases and currents assume sharp peaks. Diode must be chosen to meet such sharp peaks. In such a case, the average current, i.e., A_v $[i_d]$, may be well within the current rating of the diode, and yet the peak current may be excessive.

Approximate analysis: The output voltage v_0, for the given values of ω, R_L, C, V_m can be obtained graphically. But it is a tedious method. An approximate analysis is as follows (see Fig. 3.26). If $\omega CR_L >> 1$ then $\theta_1 \to \pi/2$ and $v_0 \to V_m$ at $t = t_1$. Also, with large C, the exponential decay can be replaced by a linear fall. Let

V_r = ripple voltage (i.e., $\pm\ V_r/2$ deviation from V_{dc})

$$\therefore \qquad V_{dc} = V_m - \frac{V_r}{2} \tag{3.43}$$

Let T_2 be the total non-conducting time, then V_r represents the voltage fall from V_m due to discharge current ($\approx I_{dc}$) in time T_2, i.e.,

$$V_r = \frac{I_{dc} T_2}{C} \qquad (\because \text{ Charge lost } Q \approx I_{dc} T_2 \text{ and } V = Q/C) \tag{3.44}$$

For better filtering, the conduction time T_1 is small and T_2 is half cycle time, i.e.,

$$T_2 = \frac{1}{2f}$$

Hence

$$V_r = \frac{I_{dc}}{C} \cdot \frac{1}{2f} \tag{3.45}$$

$$\therefore \qquad V_{dc} = V_m - \frac{I_{dc}}{4fC} \tag{3.46}$$

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Thus, the power supply may be approximated by a Thevenin's equivalent circuit shown in Fig. 3.27. Here

$$V = V_m$$

$$\text{Output resistance } R_0 = \frac{1}{4fC}$$

where input AC is $V_m \sin 2\pi ft$.

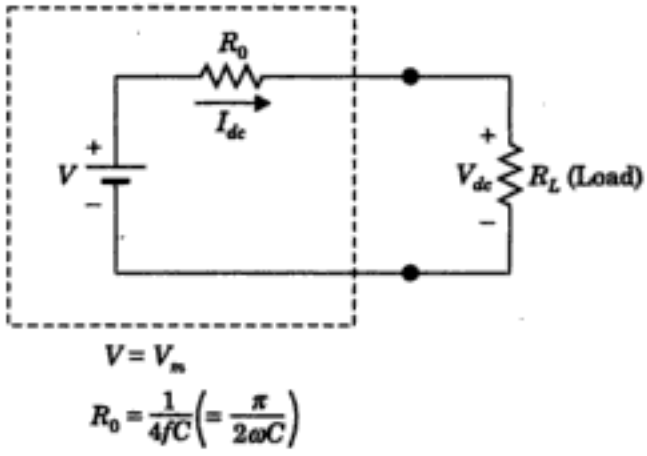


Fig. 3.27 Thevenin equivalent of the power supply.

The ripple, therefore, vary directly with the load current I_{dc} and also inversely with the capacitance C. To keep ripple low and also for good regulation, very large capacitances (of 10 μF to 100 μF) must be used. A common type of capacitor is an electrolytic (which are polarized and must be used with +ve terminal to positive voltage side). The desirable features of rectifiers using capacitor input filters are:

(a) small ripple contents,
(b) high voltage at light load.

Disadvantages of this system are:

(a) Poor regulation,
(b) High ripple for large load currents,
(c) Unsafe peak current that diode must pass during the charging of the capacitor.

Approximate analysis applied to half-wave rectifiers yields: ripple and drop of voltage from no load to full load double the values w.r.t. full-wave rectifiers.

Capacitor-input and choke-input filters: To have more efficient filtering of the rectifier output waveform, we use more than one energy storage elements. The circuits commonly used are capacitor-input and the choke-input filters as shown in Fig. 3.28.

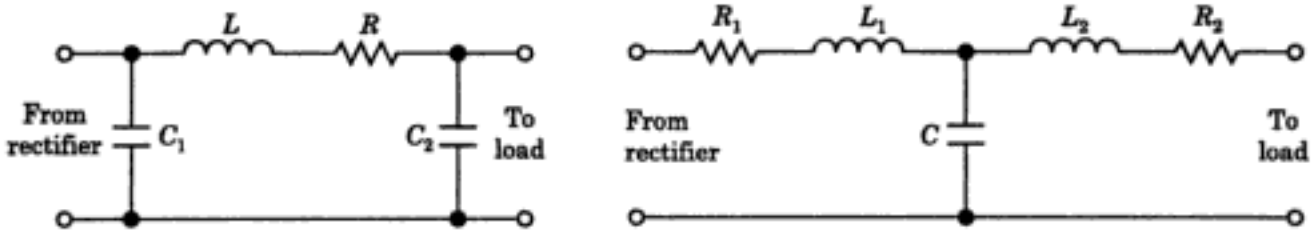


Fig. 3.28 (a) Capacitor-input filter, (b) Choke (Inductor)-input filter.

The resistances R, R_1, R_2 are inseparable parts of the inductors L, L_1 and L_2, respectively. The values of the reactances of all the chokes (inductors) are high at the AC frequency. So, they alternate the ripple voltage. Because of their zero reactances at DC ($\omega = 0$), they do not affect the DC output. The reactances of the various capacitances are low at AC frequency. These provide an easy path for ripple currents, thus eliminating them from the output side.

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EXAMPLE 3.9

(a) Consider the capacitor filter shown in Fig. 3.29. Show that, during the interval when the diode conducts, the diode current is given by

$$i = I_m \sin(\omega t + \psi)$$

where

$$I_m = V_m\sqrt{\frac{1}{R_L^2} + \omega^2 C^2} \quad \text{and} \quad \psi = \arctan \omega C R_L$$

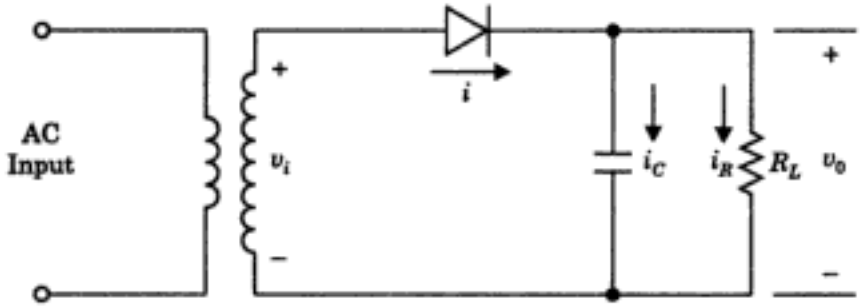


Fig. 3.29 Given circuit for Ex. 3.9.

(b) Find the cut out angle ωt_1 also.

Solution When the diode conducts then

$$v_0 = v_i = V_m \sin \omega t$$

$$i = i_C + i_R$$

$$= C\frac{dv_0}{dt} + \frac{V_m \sin \omega t}{R_L}$$

$$= C(V_m\omega)(\cos \omega t) + \frac{V_m}{R_L}\sin \omega t \qquad (\because\ v_0 = V_m \sin \omega t)$$

$$= \left[\omega C \cos \omega t + \frac{1}{R_L}\sin \omega t\right] V_m$$

Let $\omega C = r \sin \psi$

$$\frac{1}{R_L} = r \cos \psi \quad \therefore \quad r = \sqrt{(\omega C)^2 + \left(\frac{1}{R_L}\right)^2}$$

$$\tan \psi = \omega C R_L$$

$\therefore$ $i = V_m r \sin(\omega t + \psi)$

or $i = I_m \sin(\omega t + \psi)$

where $I_m = V_m\sqrt{\frac{1}{R_L^2} + \omega^2 C^2}$, $\psi = \tan^{-1} \omega C R_L$

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3.4 VOLTAGE-MULTIPLIER CIRCUITS

In order to maintain a relatively low transformer peak voltage we use voltage-multiplier circuits. Such circuits are capable of giving DC voltages two times, three times, four times or even more times the peak voltage of the input transformer.

3.4.1 Voltage Doubler

Consider Fig. 3.30(b). When V_{AB} is +ve, the capacitor C_1, initially being at zero potential difference across it, starts charging. The current flowing through it is I_1. In this situation diode D_2 remains OFF and diode D_1 conducts in forward direction with resistance R_f. Thus, the loop containing the voltage v_{AB} (from the secondary of the transformer), the capacitor C_1 and the resistance R_{f1} (forward conducting resistance of D_1) acts as a charging circuit similar to one shown in Fig. 3.19. C_1R_{f1} being very small, the voltage V_{C1} almost follows V_{AB} as long as D_1 conducts. Reference Fig. 3.30(d), we have the following action.

From $t = 0$ to $T/4$: Diode D_1 continues conducting and V_{C1} almost follows voltage $V_m \sin \omega t$ as shown in Fig. 3.30(d).

From $t = T/4$ to $3T/4$: Since voltage v_{AB} falls from V_m to zero voltage and $V_{C1} = V_m$, the net emf in the loop containing v_{AB}, C_1 and D_1 cannot keep D_1 ON since $(v_{AB} - V_m)$ is –ve. However, the negative voltage $(v_{AB} - V_m)$ at anode of D_1 is also available at the cathode of D_2. Thus, loop current I_2 (see Fig. 3.30(c)) flows and C_2 gets charged with time constant C_2R_{f2}. The direction of charging current I_2 shows that the voltage V_{PQ} is –ve. As long as $v_{AB} - V_m$ remains –ve, I_2 flows and $V_{PQ} = v_{AB} - V_m$. At $t = T/2$, $v_{AB} = 0$, therefore, $V_{PQ} = -V_m$ at $t = T/2$ [see Fig. 3.30(d) (ii)]. At $t = 3/4T$, $v_{AB} = -V_m$, $v_{AB} - V_m = -2V_m$, hence $V_{PQ} = -2V_m$.

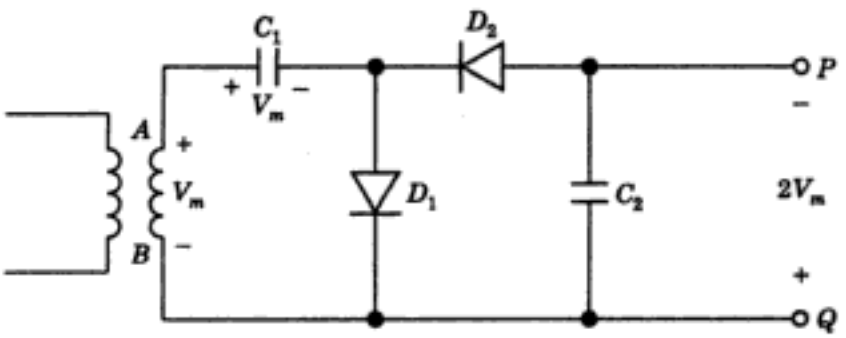


Fig. 3.30(a) A half-wave voltage doubler.

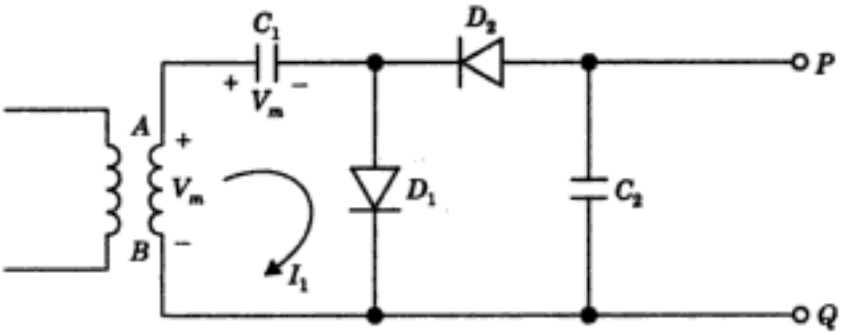


Fig. 3.30(b) D_1 ON, D_2 OFF. C_1 charges to V_m.

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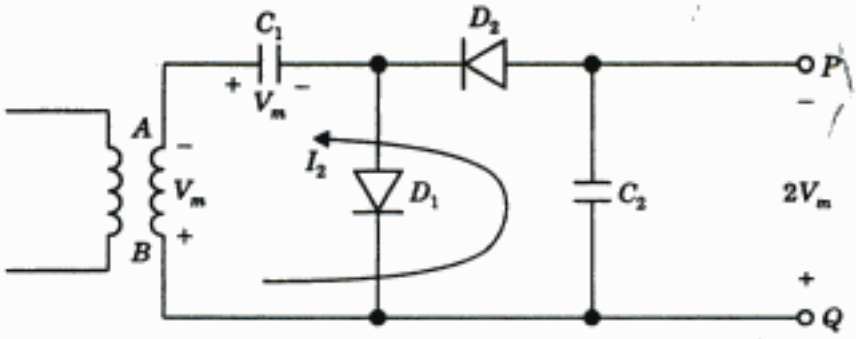


Fig. 3.30(c) D_1 OFF, D_2 ON, C_2 charges to $2V_m$ as shown.

From $t = 3/4T$ to $t = T$: Here neither D_1 conducts nor D_2 conducts. The voltages across C_1 and C_2 continue to be $+V_m$ and $-2V_m$, respectively assuming no discharge.

As we would expect, however, there is a load connected across terminals PQ (across $-2V_m$ DC voltage). The C_2 gets discharged by time constant C_2R_L. If the load resistance R_L is large, the discharge rate is low. In any case $|V_{PQ}|$ becomes lower than $2V_m$. In the next AC cycle of voltage v_{AB}, C_1 regains its lost voltage to again regain voltage V_m during time $t = 0$ to $T/4$. Also, V_{PQ} assumes a value $-2V_m$ during the cycle time $t = T/4$ to $3/4T$.

The output waveform across the capacitor C_2 is that of a half-wave signal filtered by a capacitor. The peak inverse voltage (PIV) of each diode D_1 and D_2 is $2V_m$.

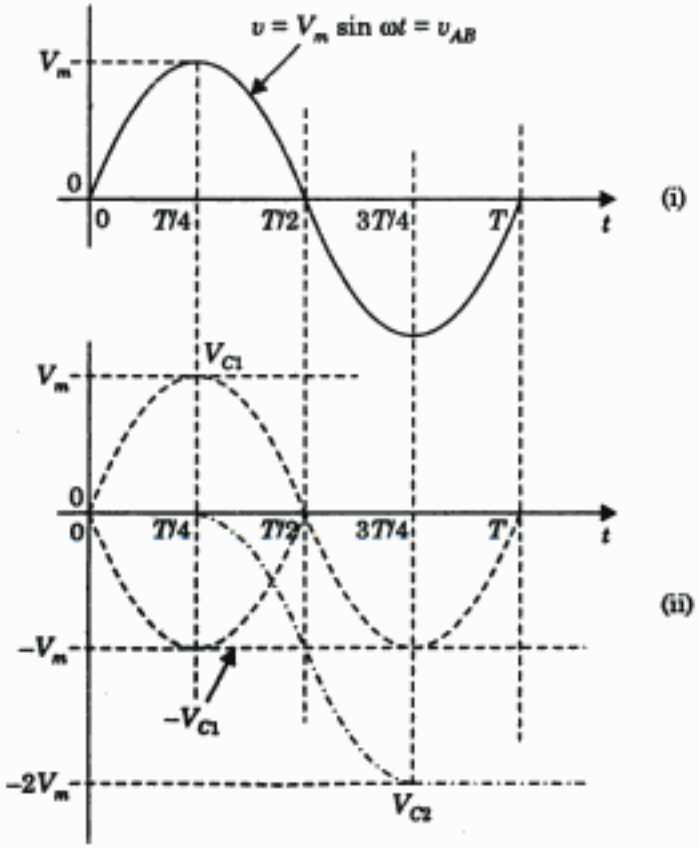


Fig. 3.30(d) The charging voltages V_{C1} and V_{C2}.

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3.4.2 Another Voltage Doubler Circuit

An alternative voltage doubler is shown in Fig. 3.31(a). During +ve half cycle of $V_{AB} = v_{AB} = V_m \sin \omega t$, the diode D_1 conducts and C_1 charges as shown in Fig. 3.31(b). V_{C1} maximum value is V_m. During the negative half cycle of v_{AB}, diode D_2 conducts and C_2 charges as depicted in Fig. 3.31(c). V_{C2} maximum value is V_m.

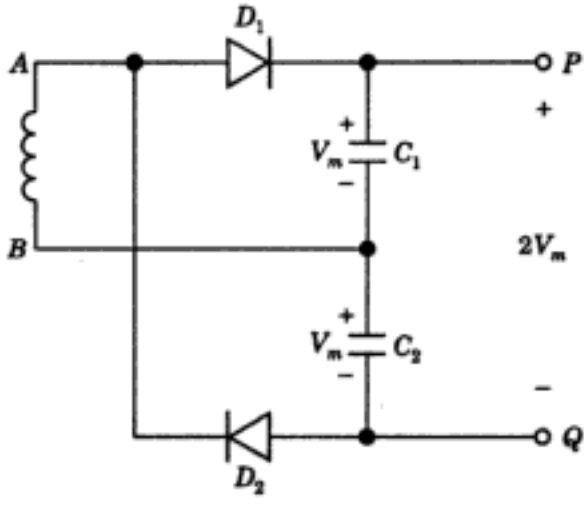


Fig. 3.31(a) Another half-cycle voltage doubler.

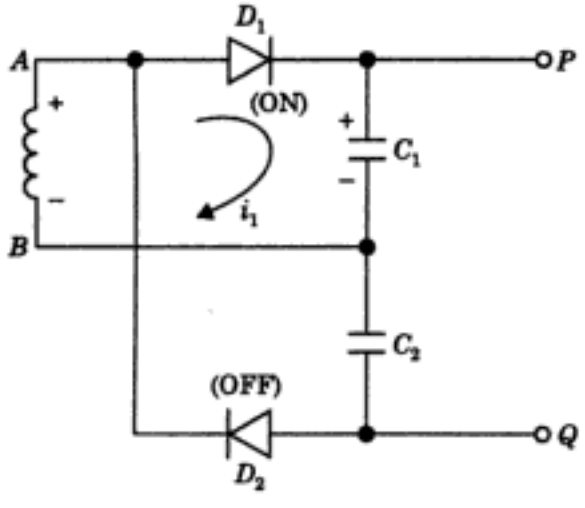


Fig. 3.31(b) C_1 charging by current i_1. V_{AB} is +ve.

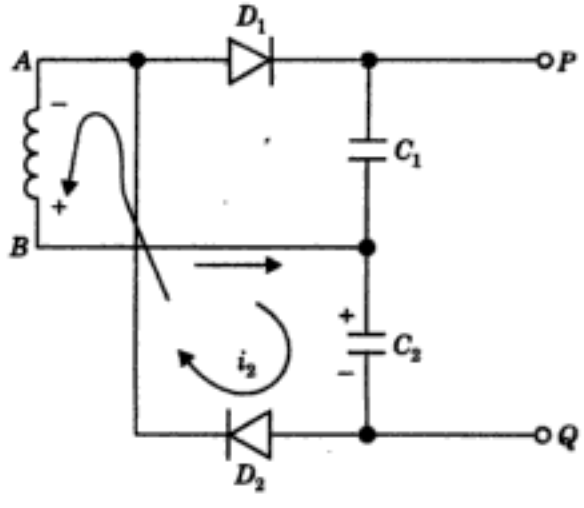


Fig. 3.31(c) C_2 charging by current i_2. V_{AB} is –ve.

The net voltage $V_{PQ} = 2V_m$. With load connected across PQ, the capacitors C_1 and C_2 discharge passing the same current. It implies that C_1 and C_2 are in series (with equivalent value $C_1C_2/(C_1 + C_2)$ which is less than C_1 or C_2. This provides poor filtering action as compared to the earlier circuit.

3.4.3 Voltage Tripler and Voltage Quadrupler

We can extend the idea of voltage doubler to higher multiples, as shown in Fig. 3.32. We have shown in Fig. 3.32 circuit capable of behaving as a voltage doubler, tripler and a

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quadrupler. By adding more capacitor and diode in the fashion as shown in Fig. 3.32, we can obviously realize voltage output which is five times, six times the V_m.

During the +ve half cycle of $V_m \sin \omega t$, the diode D_1 conducts and charges C_1 to a peak voltage of V_m. Then during the negative half of $V_m \sin \omega t$, D_2 conducts and charges C_2 to $2V_m$ volts. Then during the next positive half cycle of $V_m \sin \omega t$, D_1 and D_2 cannot conduct. It is so because voltage at E is –ve or at the most zero due to charged voltage $+V_m$ across C_1, hence D_1 cannot conduct. Also, net loop voltage in the loop $v_{AB} \rightarrow C_1 \rightarrow D_2 \rightarrow C_2$ is $v_{AB} - V_m + 2V_m$ is $+V_m$ to $2V_m$ during +ve half cycle of v_{AB}, and D_2 cannot conduct with V_{GH} +ve. However, if C_3 is initially uncharged, during v_{AB} +ve half cycle, charging current can pass in the conduction loop $A \rightarrow E \rightarrow G \rightarrow I \rightarrow J \rightarrow H \rightarrow F \rightarrow B$. This charges C_3 to $2V_m$ as shown in Fig. 3.32. Proceeding similarly, we find that all the capacitors except C_1 get charged to a peak voltage of $2V_m$ (as shown in Fig. 3.32), and C_1 gets charged to a peak voltage of V_m. This results in availability of $2V_m$, $3V_m$, $4V_m$, ... across BH, AI and BQ ... .

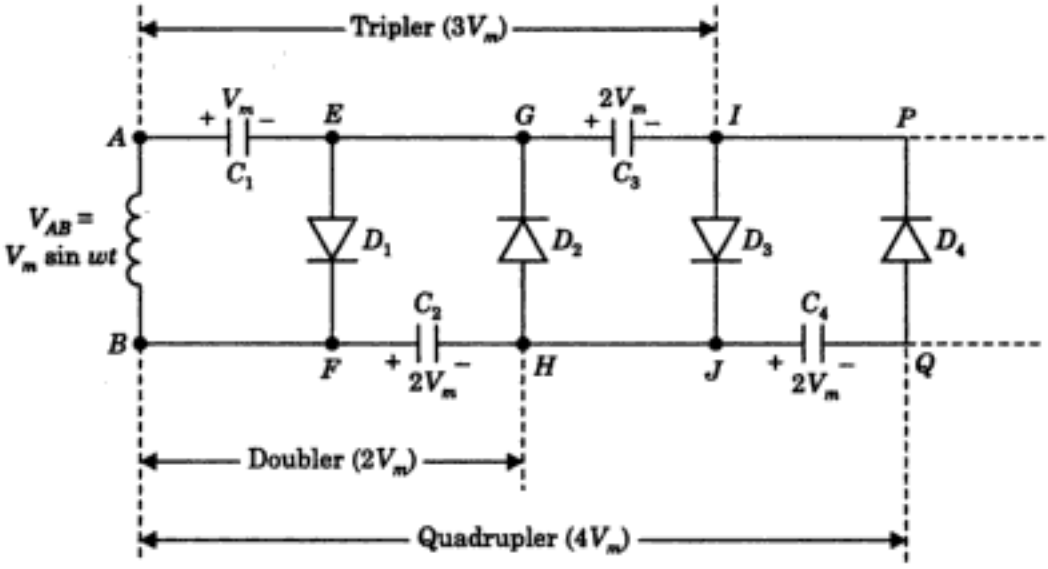


Fig. 3.32 Circuit of a generic voltage multiplier.

The transformer rating is only V_m, and each diode in the circuit must be rated at $2V_m$ PIV. We require large capacitors C_1, C_2, ..., having very low leakages, and this multiplier circuit can meet small load current.

3.5 ZENER VOLTAGE REGULATOR

The zener diodes are extensively used for voltage regulation, i.e., to keep the output voltage constant ($V_0 = V_Z$) independent of variations in load resistance R_L, and even if the supply DC voltage V_s being unregulated. The analysis of voltage regulator and design of voltage regulators using zener diodes make use of rules/formulas given in Chapter 2.

EXAMPLE 3.10

Explain the zener and Avalanche breakdown in a junction diode. Give their main comparison.

For the circuit shown in Fig. 3.33, find the minimum and maximum values of zener diode currents to ensure regulation by the zener.

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Solution For explanation of Zener and Avalanche breakdowns, see Chapter 2. We solve the numerical as follows:

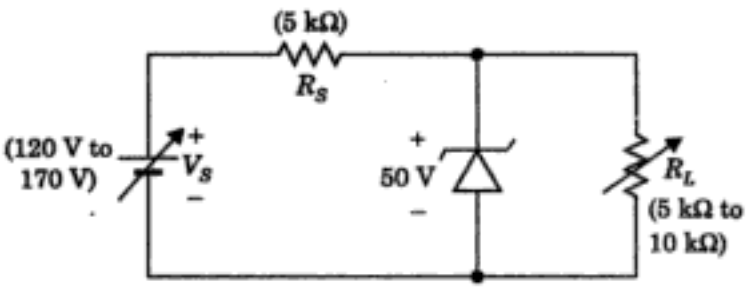


Fig. 3.33 The given figure, Ex. 3.10.

$$I_{Z_{min}} = \frac{V_{S_{min}} - V_Z}{R_S} - I_{L_{max}}$$

$$= \frac{120 - 50}{5} - \frac{50}{5}$$

$$\left(\because I_{L\,max} = \frac{50}{5}\,\text{mA}\right)$$

$$= 14 - 10 = 4 \text{ mA}$$

$$I_{Z_{max}} = \frac{V_{S_{max}} - V_Z}{R_S} - I_{L_{min}}$$

$$= \frac{170 - 50}{5} - \frac{50}{10} \qquad \left(\because I_{L\,min} = \frac{50}{10}\,\text{mA}\right)$$

$$= 24 - 5 = 19 \text{ mA}$$

$\therefore$ $I_{Z_{min}} = 4$ mA, $I_{Z_{max}} = 19$ mA **Ans.**

EXAMPLE 3.11

(a) For the circuit shown in Fig. 3.34, what values of V can regulate the voltage correctly. Assume I_L = 0 to 4 mA and I_Z has safe values from 1 to 5 mA.

(b) If I_L is fixed at 50/15 mA (i.e. R_L = 15 kΩ fixed), then find the safe voltage range of V.

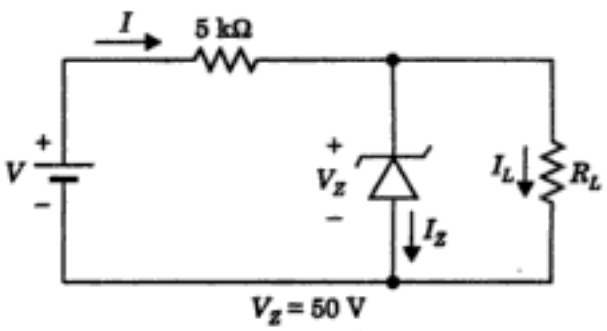


Fig. 3.34 Given circuit, Ex. 3.11.

Solution (a) Given $I_{Z_{min}} = 1$ mA

$I_{Z_{max}} = 5$ mA

I_L = 0 to 4 mA

$$\frac{(V_{max} - 50)}{5} = I_{Z\,max} + I_{L\,min} = 5 + 0$$

$\therefore$ $V_{max} = 75$ V

$$\frac{(V_{min} - 50)}{5} = I_{Z_{min}} + I_{L_{max}}$$

$$= 1 + 4$$

$\therefore$ $V_{min} = 75$ V

Thus, for V_L = 50 V regulated and I_L = 0 to 4 mA, V = 75 V No variation permissible. **Ans.**

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(b) Now, $$I_L = \frac{50}{15} = \frac{10}{3} \text{ mA (fixed)}$$

$$\therefore \quad \frac{(V_{max} - 50)}{5} = I_{Z_{max}} + I_L$$

$$= 5 + \frac{10}{3} = \frac{25}{3}$$

or $$V_{max} = 50 + 5 \times \frac{25}{3} = 91\frac{2}{3} \text{ V}$$

Then $$\frac{(V_{min} - 50)}{5} = I_{Z_{min}} + I_L$$

$$= 1 + \frac{10}{3} = \frac{13}{3}$$

or $$V_{min} = 50 + 5 \times \frac{13}{3} = 71\frac{2}{3} \text{ V}$$

$$\therefore \quad (V_{max}, V_{min}) = (91.66 \text{ V}, 71.66 \text{ V}) \quad \textbf{Ans.}$$

EXAMPLE 3.12

A voltage regulator consisting of a 6.8 V zener diode and a 100 Ω resistor and intended for operation with a 9 V supply is accidently connected to 15 V supply instead. Assuming that r_Z is very small, calculate the expected values of zener diode current and the power dissipation in both the zener diode and the resistor, for both normal and aberrant situations, and compare the ratios.

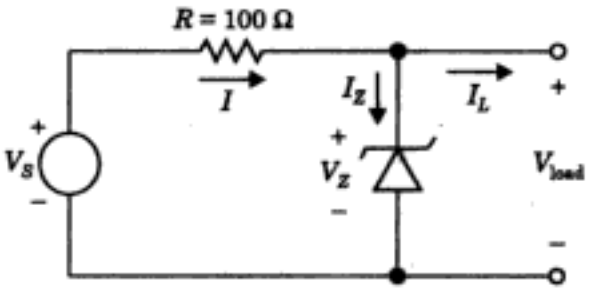


Fig. 3.35 Circuit for Ex. 3.12.

Solution *Normal situation*

$$V_S = +9\text{V}$$

$$\therefore \quad I = \frac{V_S - V_Z}{R} = \frac{9 - 6.8}{100} = 22 \text{ mA}$$

When load current I_L is zero, $I_Z = I = 22$ mA.

$$\therefore \quad P_{zener} = I_{Z_{max}} V_Z$$

$$= (22)\ (6.8) = 149.6 \text{ mW} \quad \textbf{Ans.}$$

Power dissipation in Resistor $P_{resistor} = I^2R$

$$= (22)^2 \times (100) = 48.4 \text{ mW} \quad \textbf{Ans.}$$

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Solution: (see Fig. 3.37)

For R = 1 kΩ,

$$I = \frac{10 - 6.8}{1 \times 10^3} = 3.2 \text{ mA}$$

$$\therefore \quad I_{L_{max}} = I - I_{ZK}$$

$$= 3.2 - 0.1 = 3.1 \text{ mA}$$

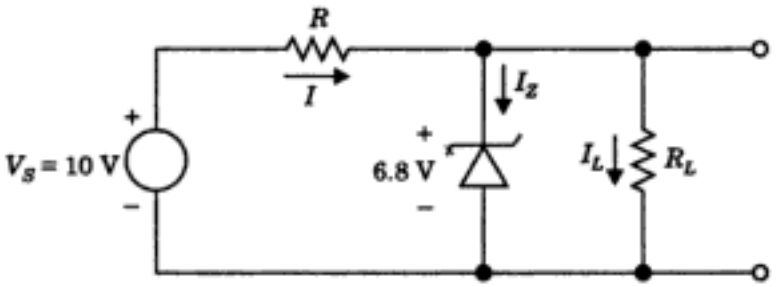


Fig. 3.37 Circuit for Ex. 3.14.

and $$R_L = \frac{6.8}{3.1} = 2.194 \text{ kΩ}$$

The load current range is $0 \le I_L \le 3.1$ mA for regulated output. **Ans.**

Redesign Part

Here R_L = 1 kΩ

and $I'_{ZK} = 10 \times I_{ZK} = 10 \times 0.1 = 1$ mA

$$\therefore \quad I_L = \frac{6.8}{1} = 6.8 \text{ mA}$$

$$I \ge I_L + I'_{ZK}$$

$$= 6.8 + 1 = 7.8 \text{ mA}$$

As $$I = \frac{V_S - V_Z}{R} \quad \therefore \quad R = \frac{10 - 6.8}{I}$$

For $I \ge 7.8$ mA, $$R \le \frac{10 - 6.8}{7.8} = 410 \text{ Ω}$$

A standard value of R = 310 may, therefore, be used in redesign. **Ans.**

EXAMPLE 3.15

The regulator illustrated in Fig. 3.38 is to provide 6 V load voltage for all load currents $I_L \le 0.5$ A. The unregulated supply varies between 8 and 10 V, and the zener diode provides regulation for $I_Z > 0$. Determine:

(a) The series resistance R_S needed.

(b) The power dissipation rating of the zener diode.

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Solution The given data is:

$$V_{S_{min}} = 8 \text{ V},\ V_{S_{max}} = 10.0 \text{ V},\ I_{L_{min}} = 0 \text{ A},\ I_{L_{max}} = 0.5 \text{ A},\ V_Z = 6 \text{ V and } I_{Z_{min}} = 0 \text{ A}$$

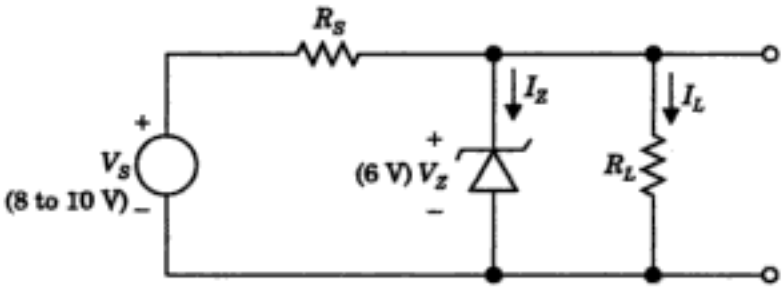


Fig. 3.38 The given circuit with values for Ex. 3.15.

We know that $$\frac{V_{S_{min}} - V_Z}{R_S} = I_{L_{max}} + I_{Z_{min}}$$

$\therefore$ $$\frac{8-6}{R_S} = \frac{2}{R_S} = 0.5 + 0.0 = 0.5$$

or $$R_S = 4\ \Omega$$

Again $$\frac{V_{S_{max}} - V_Z}{R_S} = I_{L_{min}} + I_{Z_{max}}$$

$\therefore$ $$\frac{10-6}{R_S} = \frac{4}{4} = I_{Z_{max}} + I_{L_{min}} = I_{Z_{max}} \qquad (\because\ I_{Z_{min}} = 0)$$

or $$I_{Z_{max}} = 1 \text{ A}$$

Then $$P_{Z_{max}} = V_Z I_{Z_{max}}$$

$$= 6 \times 1 = 6 \text{ W} \quad \textbf{Ans.}$$

EXAMPLE 3.16

A 7.2 V zener is used in the circuit shown in Fig. 3.39, and the load current is to vary from 12 to 100 mA. Find the value of series resistance R to maintain a voltage of 7.2 V across the load. The input voltage is constant at 20 V and the minimum zener current is 10 mA. Find also $I_{Z_{max}}$

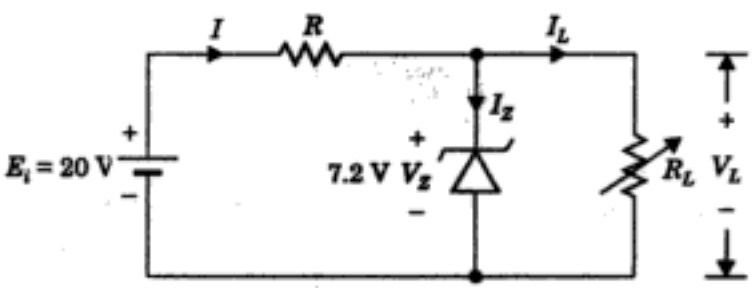


Fig. 3.39 Given circuit for Ex. 3.16.

Solution Given data is:

$$I_{Zmin} = 10 \text{ mA},\ I_{Lmin} = 12 \text{ mA},\ I_{Lmax} = 100 \text{ mA},\ E_i = 20 \text{ V and } V_Z = 7.2 \text{ V}.$$

$\therefore$ $$R = \frac{E_i - V_Z}{I} = \frac{E_i - V_Z}{I_Z + I_L}$$

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The voltage across the load would remain constant at 7.2 V due to the zener diode for all load currents I_L.

I_Z is minimum when I_L is maximum. Under this condition,

$$I = I_{Z_{min}} + I_{L_{max}} \qquad \text{(Note this step)}$$

$$= 10 + 100 = 110 \text{ mA}$$

$$\therefore \quad R = \frac{20 \text{ V} - 7.2 \text{ V}}{110} = \frac{12.8 \text{ V}}{110} = 0.116 \text{ k}\Omega = 116 \ \Omega$$

When the load current is 12 mA, the current through R remains

$$\frac{E_i - V_Z}{R} = \frac{20 - 7.2}{116} = 110 \text{ mA}$$

However, $I_{Z_{max}} = 110 - I_{L_{min}} = 110 - 12 = 98$ mA

When $I_L = 0$, then $I_Z = 110$ mA the maximum zener current for safe operation

$$I_{Z_{max}} = 110 \text{ mA} \quad \textbf{Ans.}$$

EXAMPLE 3.17

(a) The avalanche diode in the circuit regulates at 50 V over a range of diode currents from 5 to 40 mA. The supply voltage V = 200 V. Calculate R to allow voltage regulation from a load current I_L = 0 upto I_{max}, the maximum possible value of I_L (b) If R is set as in part (a) and the load current is set at I_L = 25 mA, what are the limits between which V may vary without loss of regulation.

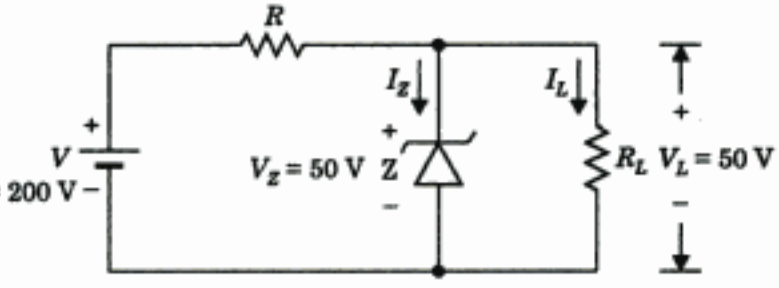


Fig. 3.40(a) The given circuit for (a), Ex. 3.17.

Solution *To find R* (see Fig. 3.40(a))

(a) When $I_L = 0$, $I_{Z\max}$ =40 mA

As $V_L = +50$ V

$$\therefore \quad \frac{200 - 50}{R} \le 40$$

or $$\frac{150}{40} \le R$$

or $$R \ge \frac{15}{4} = 3.75 \text{ k}\Omega \quad \textbf{Ans.}$$

Then I_L is maximum when I_Z is minimum. As $I_{Z_{min}}$ is 5 mA,

$\therefore$ $I_{L\max}$, for R = 3.75 kΩ, 40 – 5 = 35 mA. **Ans.**

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(b) *To find limits of V for I_L = 25 mA*

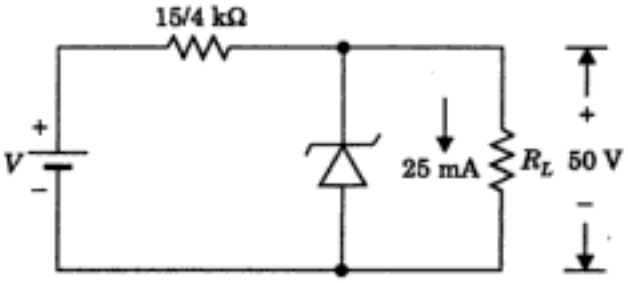


Fig. 3.40(b) Circuit for part (b), Ex. 3.17.

$$I_{Z_{min}} = \frac{V_{min} - 50}{15/4} - I_L$$

$$\therefore \quad 5 = \frac{V_{min} - 50}{15/4} - 25$$

$$\text{or} \quad V_{min} = 30 \times \frac{15}{4} + 50 = \frac{225}{2} + 50$$

$$= 162.5 \text{ V}$$

$$I_{Z_{max}} = \frac{V_{max} - 50 \text{ V}}{15/4} - 25$$

$$\therefore \quad V_{min} = 162.5 \text{ V}, V_{max} = 293.75 \text{ V} \quad \textbf{Ans.}$$

$$\text{and} \quad V_{max} = (40 + 25) \times \frac{15}{4} + 50 = \frac{65 \times 15}{4} + 50 = 293.75 \text{ V}$$

EXAMPLE 3.18

For the circuit shown in Fig. 3.41, find the value of R if the circuit regulates at 6 V for the input supply voltage of 22 V. The zener diode currents are minimum 10 mA and maximum 40 mA. The load current I_L varies from 0 to I_{max}. What is the value of I_{max}? Also, find the power rating of the zener diode.

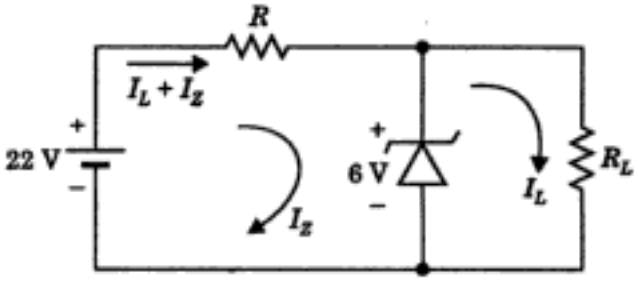


Fig. 3.41 Given circuit, Ex. 3.18.

Solution

When $I_L = 0$, $I_Z = I_{Z_{max}} = 40$ mA then

$$R = \frac{22 - 6}{40} = \frac{16}{40 \times 10^{-3}} = 400 \ \Omega \quad \textbf{Ans.}$$

Given, I_{max} for zener = 40 mA

I_{min} for zener = 10 mA

Thus, when I_L is maximum I_Z is minimum.

$$\therefore \quad I_{L_{max}} = 40 - 10 = 30 \text{ mA} \quad \textbf{Ans.}$$

Then Zener rating $= I_{Z_{max}} \times V_{zener}$

$$= (40)(6)$$

$$\therefore \quad P_{zener} = 240 \text{ mW} \quad \textbf{Ans.}$$

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EXAMPLE 3.19

For the network shown in Fig. 3.42, determine:

(a) V_L, I_L, I_Z and I_R for R_L = 180 ohms.

(b) the value of R_L that will establish maximum power dissipation condition for the zener diode.

(c) the maximum value of R_L to ensure that the zener diode remains in ON state.

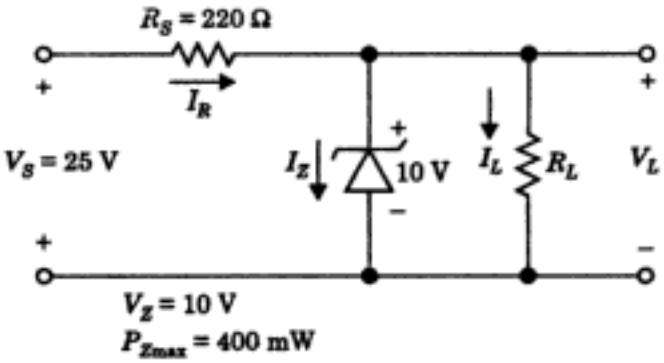


Fig. 3.42 Given circuit, Ex. 3.19.

Solution: Given data is:

$$V_Z = 10 \text{ V}$$

$$\therefore \quad I_{Z_{max}} = \frac{P_{Z_{max}}}{V_Z}$$

$$= \frac{400}{10} = 40 \text{ mA}$$

Let $I_{Z_{min}}$ = 10% of $I_{Z_{max}}$ = 4 mA (Note this step)

(a) $V_L = 10$ V, $I_L = \dfrac{V_Z}{R_L} = \dfrac{10}{180} = 5.55$ mA, $I_R = \dfrac{25-10}{220} = 68.18$ mA

$\therefore \quad I_Z = 68.18 - 5.55 = 62.63$ mA

(b) If $I_Z = I_{Z_{max}} = 40$ mA, then $I_L = I_R - I_{Z_{max}} = 68.18 - 40 = 28.18$ mA

$$\therefore \quad R_L|_{max} = \frac{V_Z}{I_L} = \frac{10}{28.18 \times 10^{-3}} = 354.8 \approx 355\ \Omega \quad \textbf{Ans.}$$

(c) If R_L is decreased, I_L increases and I_Z decreases. To keep the zener diode ON, I_Z must not be less than $I_{Z_{min}}$ (= 4 mA).

$\therefore \quad$ Maximum $I_{L_{max}} = I_R - I_{Z_{min}} = 68.18 - 4 = 64.18$ mA

and $$R_L = \frac{V_Z}{I_L} = \frac{10}{64.18 \times 10^{-3}} = 155.8 \approx 156\ \Omega \quad \textbf{Ans.}$$

If $I_{Z_{min}} = 0$ then

$$R_L = \frac{10}{68.18 \times 10^{-3}} = 146.6 \approx 147\ \Omega \quad \textbf{Ans.}$$

EXAMPLE 3.20

For the zener voltage regulator shown in the circuit, (Fig. 3.43) find the range and average wattage of the resistor R_S to keep the zener in its regulation range under the following operating conditions:

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$20\ \text{V} \le V_S \le 30\ \text{V}$, $1\ \Omega \le R_L \le 10\ \Omega$, $I_{Z_{min}} = 10\ \text{mA}$,

$P_{Z_{max}} = 50\ \text{W}$ and $V_Z = 10\ \text{V}$

Solution The given data is: (see Fig. 3.43)

$V_{S_{max}} = 30\ \text{V}$, $V_{S_{min}} = 20\ \text{V}$, $R_{L_{max}} = 10\ \Omega$

$R_{L_{min}} = 1\ \Omega$, $V_0 = V_Z = 10\ \text{V}$, $I_{Z_{min}} = 10\ \text{mA}$

Thus, $I_{L_{min}} = \dfrac{10}{10} = 1\ \text{A}$ and $I_{L_{max}} = \dfrac{10}{1} = 10\ \text{A}$

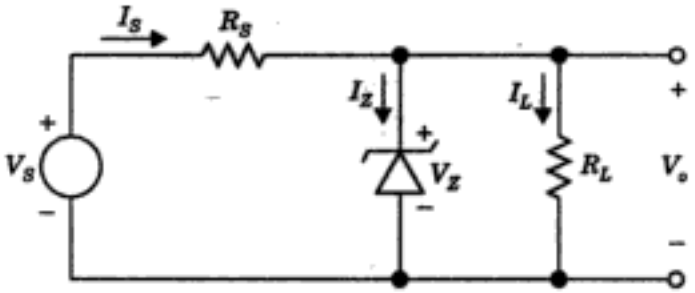


Fig. 3.43 The given circuit, Ex. 3.20.

Now, $I_{Z_{max}} = \dfrac{P_{Z_{max}}}{V_Z} = \dfrac{50}{10} = 5\ \text{A}$

Let $V_{S_1} = V_{S_{min}} = 20\ \text{V}$

$\therefore \quad \dfrac{V_{S_{min}} - V_Z}{R_{S_1}} \ge (I_{L_{max}} + I_{Z_{min}})$

$\therefore \quad R_{S_1} \le \dfrac{20 - 10}{10.01}$ or $R_{S_1} \le 0.999\ \Omega$

Now, let $V_{S_2} = V_{S_{max}} = 30\ \text{V}$

$\therefore \quad \dfrac{V_{S_{max}} - V_Z}{R_{S_2}} \le (I_{L_{min}} + I_{Z_{max}})$

or $R_{S_2} \ge \dfrac{30 - 10}{6}$ or $R_{S_2} \ge 3.333\ \Omega$

Thus, to meet the load current variation from 1 A to 10 A a zener of specification $I_{Z_{min}} = 0.01\ \text{A}$ to $I_{Z_{max}} = 5\ \text{A}$ cannot meet the requirement for any value of R_S

Because the conflicting requirement

$R_S \le 0.999\ \Omega$

$R_S \ge 3.333\ \Omega$ cannot be met. **Ans.**

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Note:

When $(I_{Z_{max}} - I_{Z_{min}}) < (I_{L_{max}} - I_{L_{min}})$, the zener regulator cannot be designed in general. Suppose, in the given numerical, the value of R_L were $1\ k\Omega \le R_L \le 10\ k\Omega$ then

$$I_{L_{min}} = \frac{10}{10} = 1\ mA$$

$$I_{L_{max}} = \frac{10}{1} = 10\ mA$$

$$\therefore \quad \frac{V_{S_{min}} - V_Z}{R_S} \ge (I_{L_{max}} + I_{Z_{min}})$$

$$\text{i.e.} \quad \frac{20 - 10}{R_S} \ge (10 + 10)\ mA$$

$$\therefore \quad R_S \le 0.5\ k\Omega$$

$$\text{and} \quad \frac{V_{S_{max}} - V_Z}{R_S} \le (I_{L_{min}} + I_{Z_{max}})$$

$$\text{i.e.} \quad \frac{30 - 10}{R_S} \le (0.001 + 5)\ A$$

$$\therefore \quad R_S \ge \frac{20}{5.001} = 3.999\ \Omega \quad \textbf{Ans.}$$

Thus, $3.999 \le R_S \le 500\ \Omega$

Choose $R_S = 4\ \Omega$, say

$$\text{Wattage of } R_S = I_{max}^2 R_S = (I_{L_{max}} + I_{Z_{max}})^2 R_S$$

$$= (0.01 + 5)^2 \times 4 = 100.4\ W \quad \textbf{Ans.}$$

3.6 CLIPPING AND CLAMPING

Clipping and Clamping operations refer to waveshaping and by these we modify the given waveform for specific requirements, in special electronic units.

3.6.1 Clipping

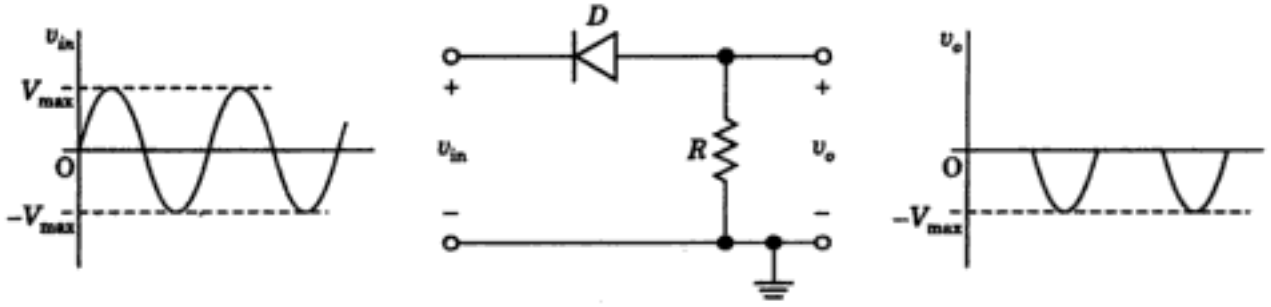
In many situations we are required to transmit a part of waveform which lies, say, above or below some reference voltage. The half-wave rectifier clips one half of the input AC voltage waveform and the other half waveform is outputted as it is without any change. Such circuits which allow a part of the waveform (usually AC waveforms) at the output without any distortion, are called **Clippers**. Thus, the function of a clipping circuit is to clip

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off (to cut off) or to remove an unwanted portion of the input signal without distorting the remaining part of the input AC waveform.

In order to perform clipping operation, we, in general, require a diode, a resistor, a battery or a combination of these components. In such circuits the diode acts as a switch which is ON (closes) on forward bias and is OFF (opens) on reverse bias. The battery used in the clipper circuit enables us to realize clipping at different voltage levels. The clipped circuits find extensive use in radars, digital computers and other electronic gadgets.

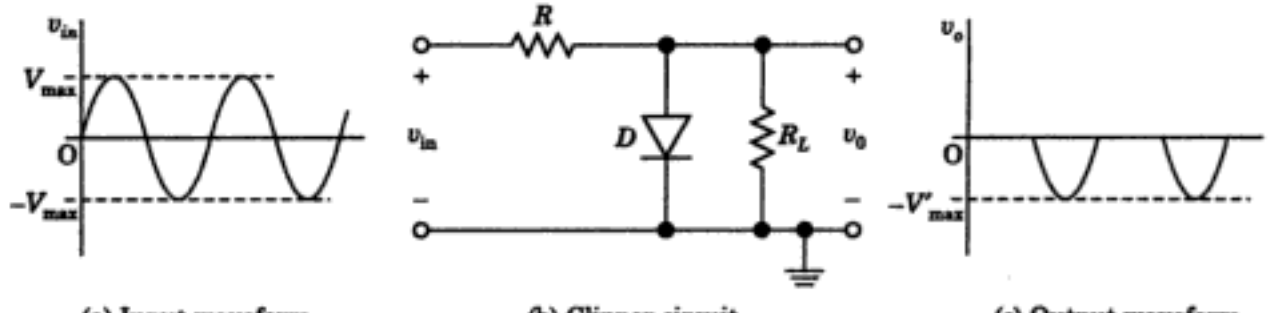
Series clippers. Consider the circuits exhibited in Fig. 3.44. Assume that the diode D is ideal (i.e., $V_\gamma = 0$, $R_f = 0$). Whenever the cathode of the diode D is –ve w.r.t. its anode, D conducts, acts as an ON switch, and allows the input waveform V_{in} to appear, without any distortion, at the output as v_0, as shown in Fig. 3.44(c). If we reverse the direction of the diode D in above circuit, the output v_0 will consist of +ve half cycles of the input wave v_{in}. This is precisely the function of a half-wave rectifier. Thus we obtain +ve or –ve waveform clipping by inserting a diode in series with the input signal v_{in}.



(a) Input waveform (b) Clipper circuit (c) Output waveform

Fig. 3.44 A positive series clipper (positive part of v_{in} gets cut).

Shunt Clippers. The clipping operation achieved by the circuit illustrated in Fig. 3.44 can also be achieved by an alternative circuit shown in Fig. 3.45.



(a) Input waveform (b) Clipper circuit (c) Output waveform

Fig. 3.45 A positive clipper—shunt clipper.

When v_{in} is +ve, diode D conducts, it shorts the load resistance R_L and $v_0 = 0$. When v_{in} is –ve, D is OFF, v_{in} gets divided as

$$v_o = v_{in} \times \frac{R_L}{R + R_L}$$

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$$\therefore \quad V'_{max} = V_{max} \cdot \frac{R_L}{R + R_L}$$

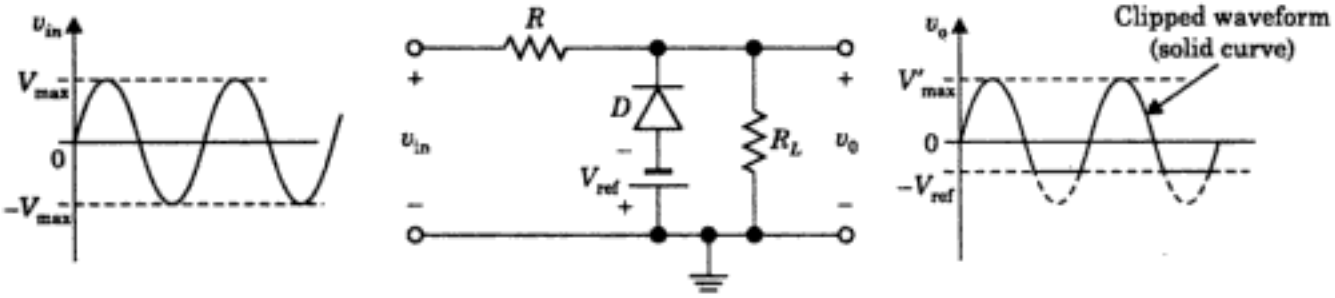
If we choose $R_L >> R$ then V'_{max} is nearly equal to V_{max}, i.e., v_0 is of the same shape (in –ve cycles) but slightly reduced in amplitude.

Biased clippers. We can also have clippers which clip a part of input wave above or below a voltage level. Consider the clipper circuit given in Fig. 3.46. This is a modification of the shunt clipper of Fig. 3.45 where we have added a –ve voltage $-V_{ref}$ (Reference voltage for clipping) as shown in Fig. 3.46. The output voltage, when Diode D is ON is not zero here (as was in the case of unbiased shunt clipper of Fig. 3.45). Diode D is OFF (i.e. open circuit) as long as its cathode is above $-V_{ref}$ voltage and here the output is given as

$$v_0 = v_{in} \times \frac{R_L}{R + R_L} \qquad \text{(for } D \text{ OFF)}$$

$$\therefore \quad V'_{max} = V_{max} \frac{R_L}{R + R_L}$$

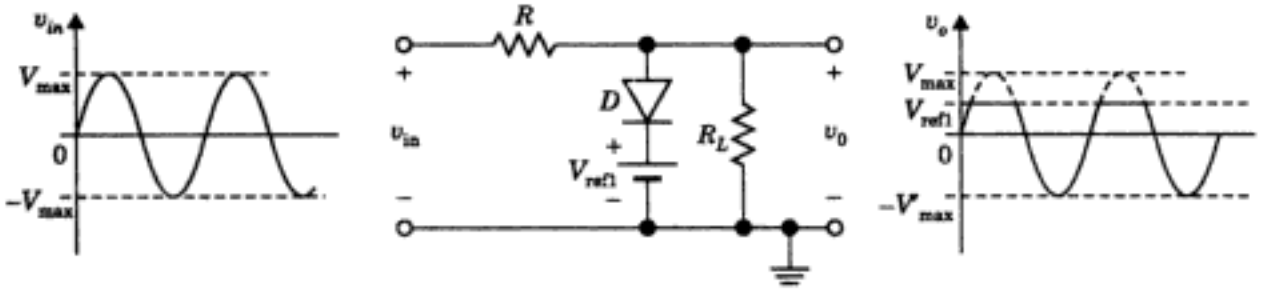
When v_{in} is less than $-V_{ref}$, D is ON, and v_0 equals the battery voltage $-V_{ref}$.



(a) Input waveform (b) The biased clipper circuit (c) Output waveform

Fig. 3.46 The biased clipper (Negative bias).

It is also possible to clip an input voltage above some other reference voltage, say, V_{ref1}, as shown in Fig. 3.47.



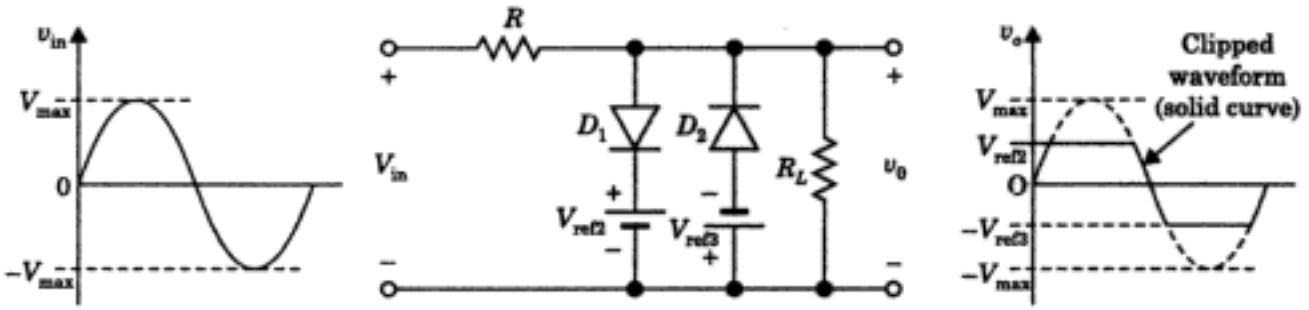
(a) Input waveform (b) Positive biased clipper (c) Output waveform

Fig. 3.47 Positive biased clipper.

Here the diode D is ON when v_{in} exceeds V_{ref1} and in this condition $v_0 = V_{ref1}$. As long as D is OFF (when $v_{in} < V_{ref1}$), $v_o = v_{in}$. We have assumed $R_L >> R$ for simplicity.

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Bidirectional (combined) clippers. It is also feasible to design clippers which clip (cut off) the input waveform above a certain level (V_{ref2}) and below a certain level ($-V_{ref3}$) as shown in Fig. 3.48.



(a) Input waveform (b) The bidirectional clipper circuit (c) Output waveform

Fig. 3.48 Combined clipper.

Note that when v_{in} exceeds V_{ref2}, D_1, being forward biased, conducts and $v_0 = + V_{ref2}$. When v_{in} has the amplitude below $-V_{ref3}$. D_2 conducts (D_1 is OFF in this case), and $v_0 = - V_{ref3}$. Between the values $-V_{ref3} < v_{in} < V_{ref2}$, both the diodes D_1 and D_2 are OFF, and $v_0 = v_{in} \dfrac{R_L}{R + R_L}$. If $R_L >> R$, then $v_0 \approx v_{in}$ when v_{in} varies between $-V_{ref3}$ and $+V_{ref2}$, as is shown in Fig. 3.48(c).

The following examples illustrate the operation of clippers.

EXAMPLE 3.21

Sketch the transfer characteristics and the outputs of the circuits shown in Fig. 3.49(a) and (b), assuming $V_\gamma = 0.6$ V, and $R_f = 100\ \Omega$, $R_\gamma = \infty$.

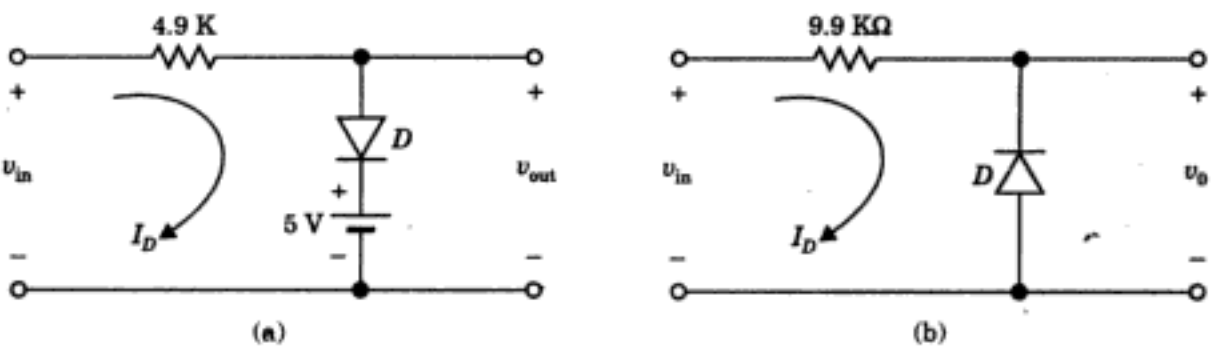


Fig. 3.49 Given circuits for Ex. 3.21.

Solution

(a) Given $v_{in} = 40 \sin \omega t$, $V_\gamma = 0.6$ V and $R_f = 0.1$ kΩ

Diode D is OFF for $v_{in} < 5.6$ V then $v_0 = v_{in}$

Diode D is ON for $v_{in} \geq 5.6$ V then

$$I_D = \frac{v_{in} - 5.6}{4.9 + 0.1} = \frac{1}{5}(v_{in} - 5.6)$$

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$$v_0 = v_{in} - I_D(4.9) = v_{in} - 4.9\left(\frac{v_{in}}{5} - \frac{5.6}{5}\right)$$

$$= 0.02v_{in} + 5.488$$

Check, when $v_{in} = 5.6$ V

$$v_o = 0.02(5.6) + 5.488$$

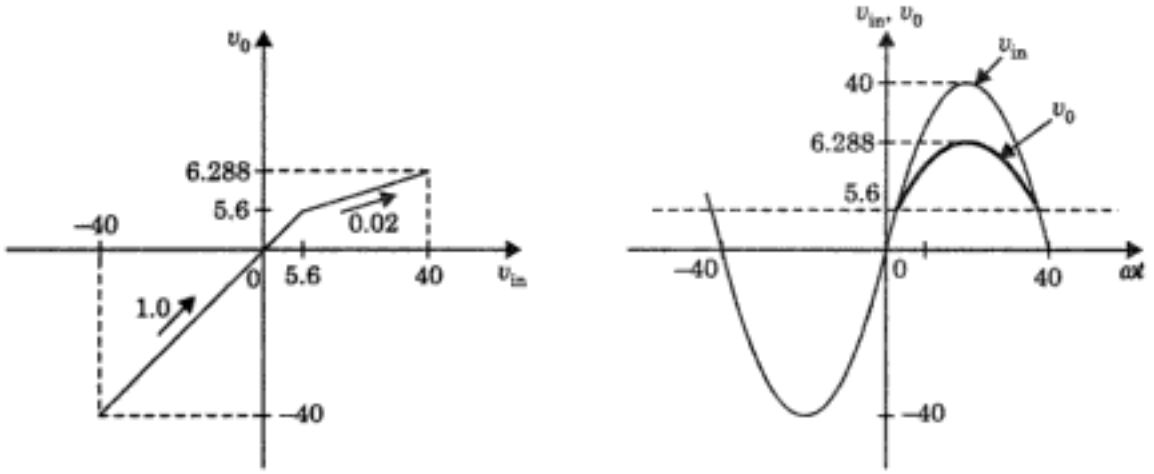
$$= 0.112 + 5.488$$

$$= 5.6 \text{ V (as expected)}$$

When $v_{in} = 40$ V

$$v_o = 0.02\ (40) + 5.488$$

$$= 6.288 \text{ V}$$



(a) The transfer characteristic

(b) Output voltage v_0 and the input voltage v_{in}

Fig. 3.50 Ex. 3.21(a) Transfer characteristic and the output waveforms.

(b) Given $v_{in} = 40 \sin \omega t$, $V_\gamma = 0.6$ V and $R_f = 0.1$ kΩ

Diode D is OFF when $v_{in} > -0.6$ V

then $v_0 = v_{in}$

Diode D is ON when $v_{in} < -0.6$ V, then

$$I_D = \frac{v_{in} + 0.6}{9.9 + 0.1}$$

(and for D to conduct, I_D, as shown in Fig. 3.49(b) must be –ve, i.e., $v_{in} < -0.6$ V)

$$= \frac{1}{10}(v_{in} + 0.6)$$

$\therefore$ $v_0 = v_{in} - I_D \times 9.9$

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i.e. $$v_0 = v_{in} - \frac{1}{10}(v_{in} + 0.6) \times 9.9$$

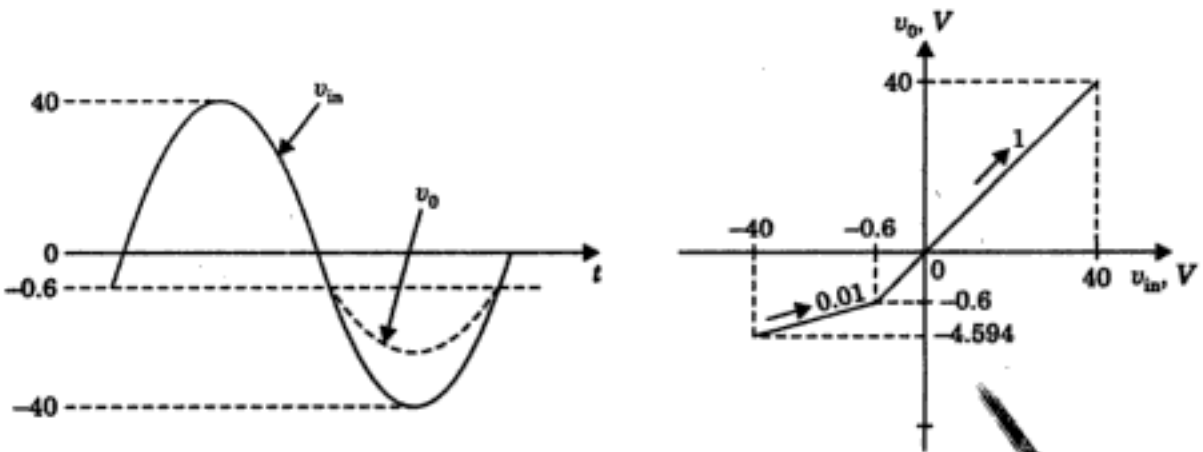
$$= 0.01v_{in} - 0.594$$

Check, when $v_{in} = -0.6$ V

$$v_0 = 0.01(-0.6) - 0.594 = -0.6 \text{ V} \quad \text{(as expected)}$$

When $v_{in} = -40$ V

$$v_0 = 0.01(-40) - 0.594 = -4.594 \text{ V}$$



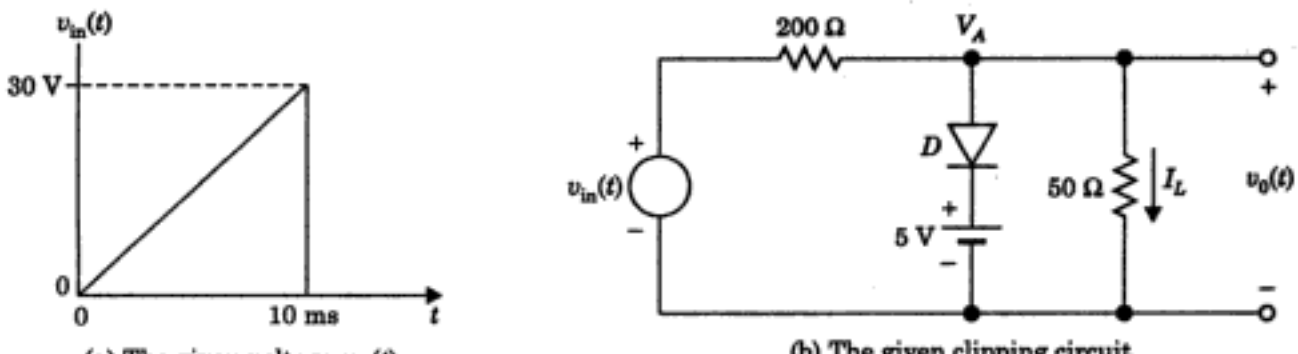
(a) Output voltage v_0 and the input voltage v_{in}

(b) The transfer characteristic

Fig. 3.51 Ex. 3.21(b) The output waveform and the transfer characteristic.

EXAMPLE 3.22

Sketch the voltage transfer characteristic (v_0 versus v_{in}) for the circuit shown in Fig. 3.52, assuming that the diode is (a) ideal, (b) represented by $V_\gamma = 0.5$ V and $R_f = 40\ \Omega$.



(a) The given voltage $v_{in}(t)$

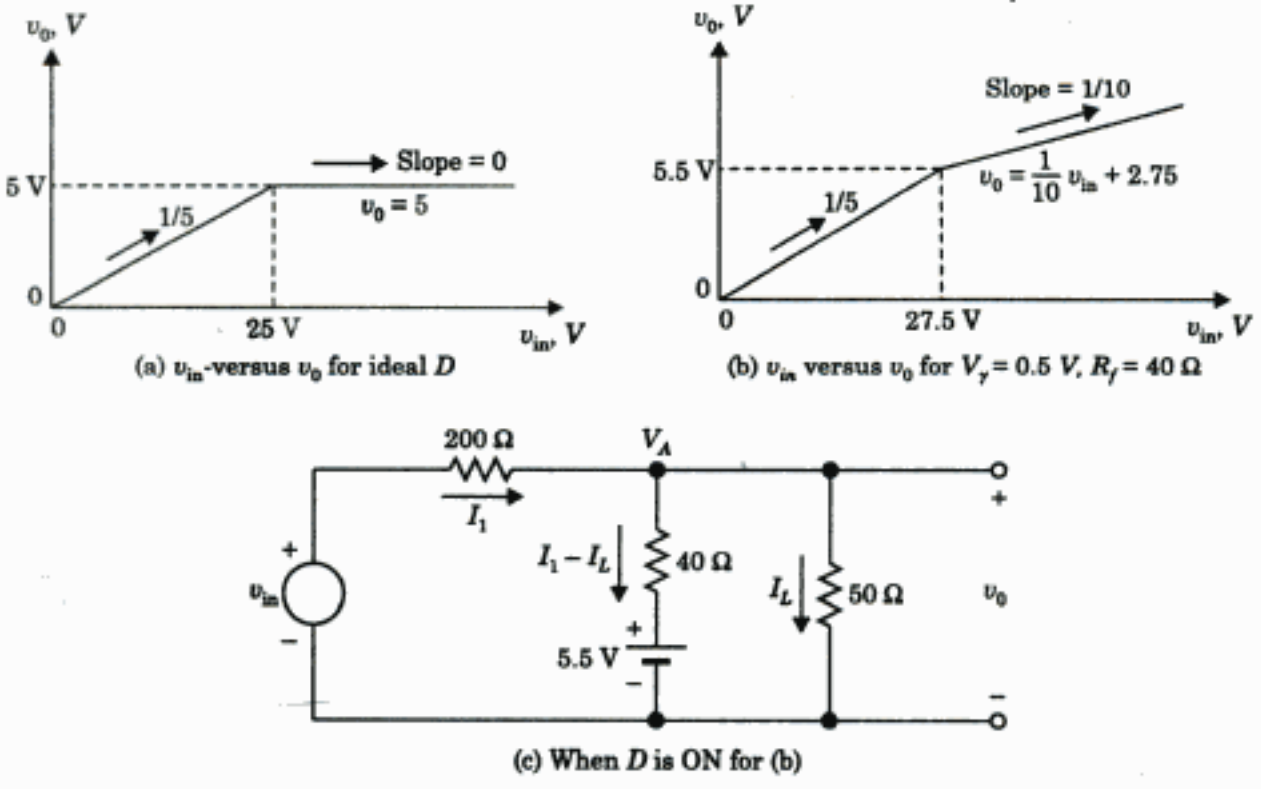
(b) The given clipping circuit

Fig. 3.52 Circuit for Ex. 3.22

Solution (a) When $V_\gamma = 0$, $R_f = 0$. Clearly D conducts when $v_0(t) \geq 5$. Then

$$v_o(t) = \begin{cases} \dfrac{50}{250} v_{in}, v_{in}(t) < 5, & \text{D-OFF} \\ 5 \text{ V}, v_{in}(t) \geq 5, & \text{D-ON} \end{cases}$$

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(a) v_{in}-versus v_0 for ideal D

(b) v_{in} versus v_0 for $V_\gamma = 0.5$ V, $R_f = 40\ \Omega$

(c) When D is ON for (b)

Fig. 3.53 Ex. 3.22(a) and (b) are the transfer characteristics and (c) is the equivalent circuit when D is ON.

When D is OFF

Here $$I_L = \frac{v_{in}}{200 + 50}$$

and $$v_0 = I_L \times 50 = \frac{1}{5} v_{in}$$

Then $v_0 < 5$ V upto $v_{in} = 0$ to 25 V

When D is ON

$v_0 = 5$ V (the battery voltage)

The transfer characteristic for D ideal is shown in Fig. 3.53(a).

(b) If $V_\gamma = 0.5$ V, $R_f = 40$.

When V_0 exceeds 5.5, then D conducts.

When D is OFF

$$v_0 = \frac{v_{in}}{250} \times 50 = \frac{1}{5} v_{in}$$

$v_0 \geq 5.5$ when $v_{in} \geq 5 \times 5.5 = 27.5$ upwards

When D is ON

$$I_1 = \frac{v_{in} - V_A}{200}$$

$$I_L = \frac{V_A}{50}$$

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and $$I_1 - I_L = \frac{(V_A - 5.5)}{40}$$

Eliminate I_1 and V_A, we get

$$I_L = \frac{(v_i + 27.5)}{500}$$

$$v_0 = 50 \times I_L = \frac{1}{10} v_{in} + 2.75$$

The transfer characteristic when V_γ = 0.6 V and R_f = 40 Ω is shown in Fig. 3.53(b).

EXAMPLE 3.23

Find the output voltage v_0 for the clipper shown in Fig. 3.54. Also, plot the transfer characteristic curve, i.e., v_{in} versus v_0.

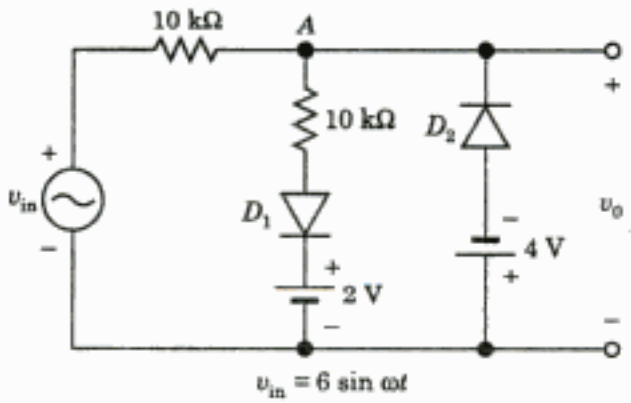


Fig. 3.54(a) The given circuit (clipper) for Ex. 3.23.

Solution *D_1, D_2 both ON* (if possible)

It is not feasible, since when D_2 is ON then $V_A \leq -4$ V, and then D_1 cannot conduct when V_A is –ve.

Only D_1 ON and D_2 OFF (see Fig. 3.54(b))

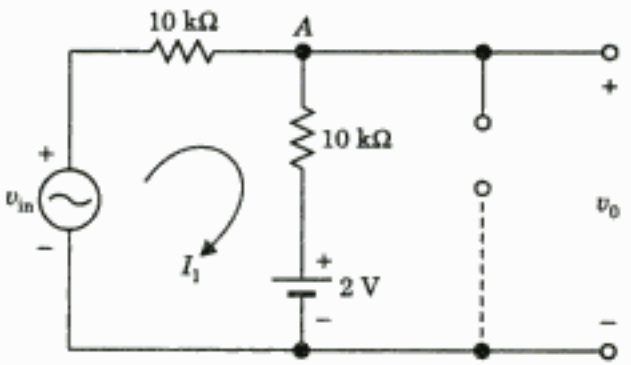


Fig. 3.54(b) D_1 ON, D_2 OFF.

The resulting circuit is illustrated in Fig. 3.54(b)

$$I_1 = \frac{(v_{in} - 2)}{(10 + 10)}$$

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I_1 is +ve only for $v_{in} \geq 2$.

Then $$v_0 = v_{in} - 10 \cdot I_1 = v_{in} - 10 \frac{v_{in} - 2}{20}$$

$$= \frac{1}{2} v_{in} + 1 \qquad \text{(for } v_{in} \geq 2\text{)}$$

D_1 OFF and D_2 ON

The resulting circuit is shown in Fig. 3.54(c)

$$I_2 = -\frac{v_i + 4}{10}$$

I_2 is +ve, only for $v_{in} < -4$ V.

Then $v_0 = -4$ V (for $v_{in} \leq -4$)

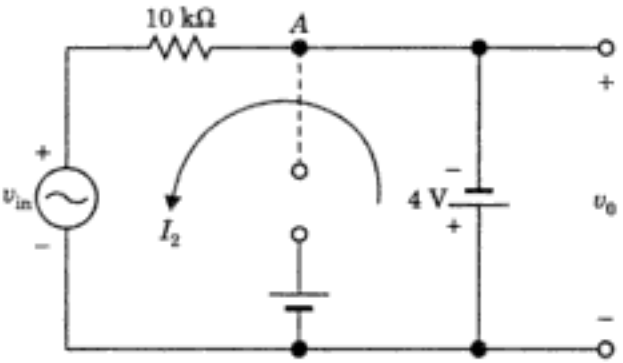


Fig. 3.54(c) D_1 OFF, D_2 ON.

Both D_1 and D_2 OFF

Clearly, when D_1 is OFF ($v_{in} \leq 2$ V) and D_2 is OFF ($v_{in} \geq -4$ V). Both D_1 and D_2 are, therefore, OFF for

$$-4 \leq v_{in} \leq 2$$

Here, $v_0 = v_{in}$ (for $-4 \leq v_i \leq 2$)

The resulting transfer characteristic is shown in Fig. 3.54(d).

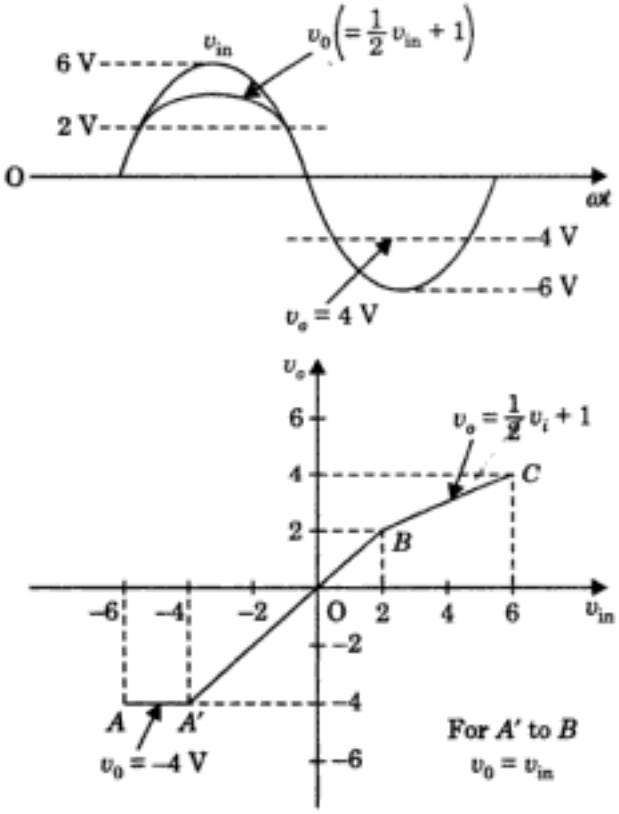


Fig. 3.54(d) Transfer characteristics.

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EXAMPLE 3.24

Obtain the voltage transfer characteristics for the circuit shown in Fig. 3.55(a) assuming that the diodes are identical and have $V_\gamma = 0.6$ V, $R_f = 0$.

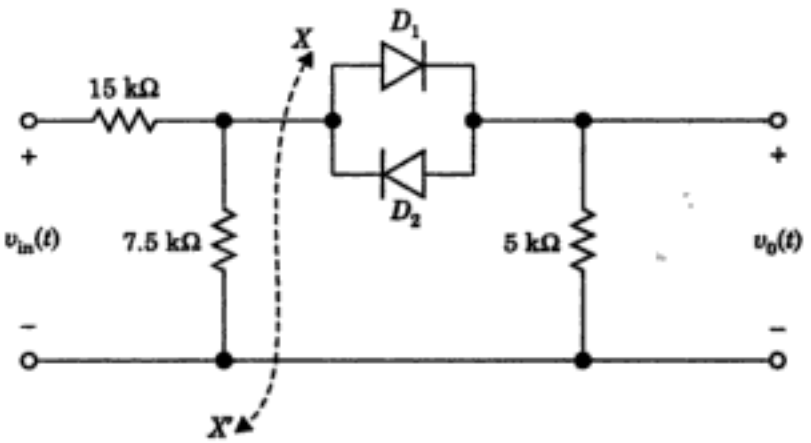


Fig. 3.55(a) The given circuit, Ex. 3.24.

Solution

We first obtain Thevenin's equivalent on LHS of XX' [see Fig. 3.55(b)]

$$V_{TH} = V_{in}(t) \times \frac{7.5}{15 + 7.5} = V_{in}(t) . \frac{1}{3}$$

and

$$R_{TH} = (15\ \text{K}) \parallel (7.5\ \text{K}) = \frac{15 \times 7.5}{15 + 7.5} = 5.0\ \text{k}\Omega$$

Let $\tilde{V}_s(t)$ be such that D_1 conduct and, therefore, $\tilde{V}_s > 0$, making D_2 OFF. Then I_1 flows.

$$I_1 = \frac{\tilde{V}_s - 0.6}{5 + 5} = \frac{\frac{1}{3} v_{in} - 0.6}{10}$$

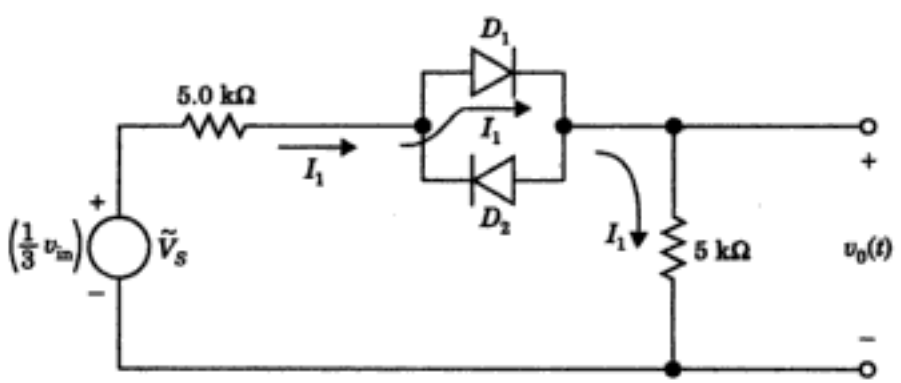


Fig. 3.55(b) Thevenin's equivalence of circuit in Fig. 3.55(a).

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I_1 is +ve only for $V_{in} > 1.8$ V. Then

$$v_0 = 5.0 \times I_1 = \frac{5}{10}\left(\frac{v_{in}}{3} - 0.6\right)$$

$$= \frac{v_{in}}{6} - 0.3$$

$v_0(t)$ versus $v_{in}(t)$ is shown in Fig. 3.55(c).

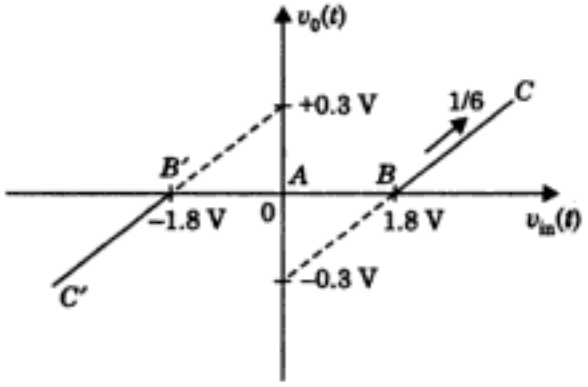


Fig. 3.55(c) The transfer characteristics.

AB : $v_{in}(t)$ is 0 to 1.8 V, $v_o = 0$

BC : $v_{in}(t) > 1.8$, BC has slope 1/6

Part $AB'C'$ can be drawn by symmetry. **Ans.**

EXAMPLE 3.25

The input voltage v_{in} to the circuit shown in Fig. 3.56(a) is a sinusoidal wave with ± 15 V. Assume ideal diodes; sketch

(i) Output voltage waveform v_0

(ii) Transfer curve v_0 versus v_{in}.

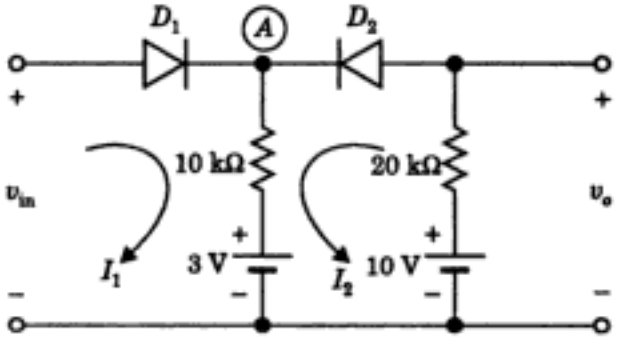


Fig. 3.56(a) The given circuit, Ex. 3.25.

Solution

When $v_{in} < 3$ V, *D_1 is OFF and D_2 is ON.*

$\therefore \quad I_1 = 0 \quad (D_1 \text{ OFF})$

and $$I_2 = \frac{(10-3)}{(20+10)} = \frac{7}{30} \times 20 \text{ mA} \quad (D_2 \text{ ON})$$

$$v_0 = +10 - I_2 \,.\, 20 = 10 - \frac{7}{30} \times 20 = 10 - \frac{14}{3} = \frac{16}{3} \text{ V.} \quad \textbf{Ans.}$$

We shall see that v_{in} must be less than 16/3 V for D_1 to remain OFF and D_2 to be ON.

Suppose D_1 conducts and D_2 is also ON. We first find the minimum value of v_{in} when D_1 can just start conduction.

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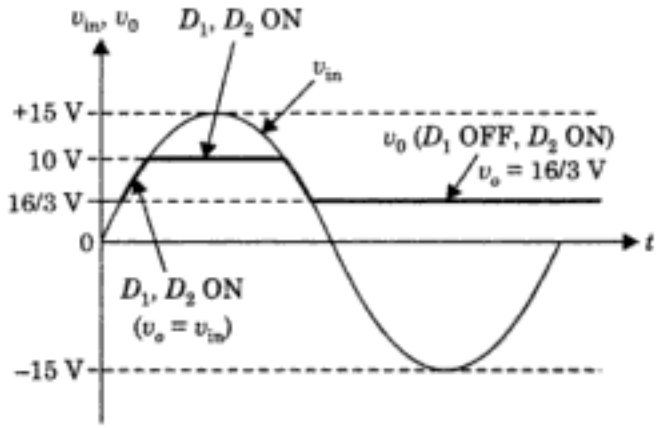


Fig. 3.56(b) Input-output waveforms.

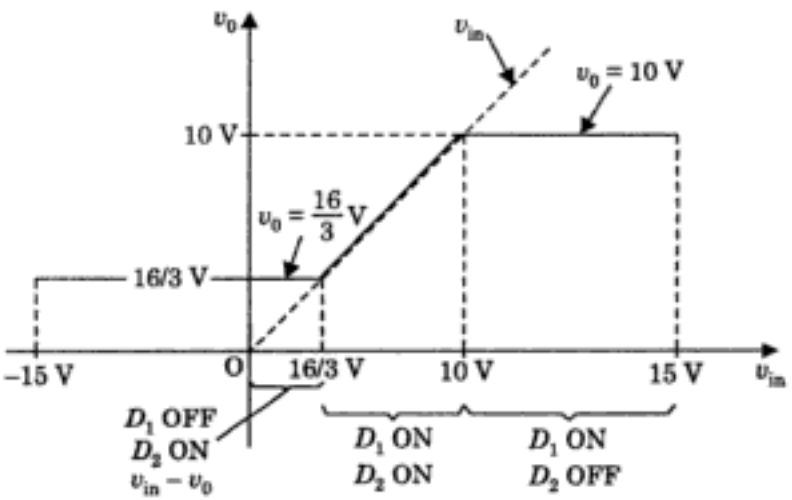


Fig. 3.56(c) Transfer curve.

If D_1 and D_2 both conduct, the currents I_1 and I_2 as shown in Fig. 3.56(a) must be +ve. We have

$$v_{in} - 3 = 10(I_1 + I_2) \quad \text{(loop of } D_1 \text{ conduction)} \tag{i}$$

$$10 - 3 = 20I_2 + 10(I_1 + I_2) \quad \text{(loop of } D_2 \text{ conduction)} \tag{ii}$$

From Eq. (ii), $30I_2 = 7 - 10I_1 \quad \therefore \quad I_2 = \dfrac{1}{30}(7 - 10I_1)$

Putting $I_2 = \dfrac{1}{30}(7 - 10I_1)$ in Eq. (i), we get

$$v_{in} - 3 = 10\left(I_1 + \frac{7}{30} - \frac{10I_1}{30}\right) = \frac{7}{3} + \frac{20}{3}I_1$$

$$\therefore \quad I_1 = \frac{3}{20}\left(v_{in} - \frac{16}{3}\right)$$

Thus, I_1 is +ve only if $v_{in} > 16/3$. Hence, for $v_{in} > 16/3$, $v_0 > 16/3$ V as in case (a) since *D_1 is OFF and D_2 is ON.*

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As v_{in} rises (for D_1 ON, D_2 ON and $v_{in} > 16/3$) a stage comes when $V_A = v_0$ (now) exceeds 10 V. Once V_A exceeds 10 V, D_2 goes OFF and the output

$$v_0 = 10 \text{ V} \quad \text{as} \quad I_2 = 0. \quad (D_1 \text{ ON and } D_2 \text{ OFF})$$

The input v_{in} and output v_0 waveforms and also the transfer curve ($v_{in} - v_0$) are as shown in Fig. 3.56(b) and 3.56(c), respectively.

EXAMPLE 3.26

For the circuit shown in Fig. 3.57(a) obtain voltage transfer characteristic (i.e., v_{in} versus v_0). Also, draw $v_{in}(t)$ and $v_0(t)$ versus time t on the same graph. Assume ideal diodes D_1 and D_2. Assume the input voltage varying from 0 to 120 V in time 0 to T as shown in Fig. 3.57(b).

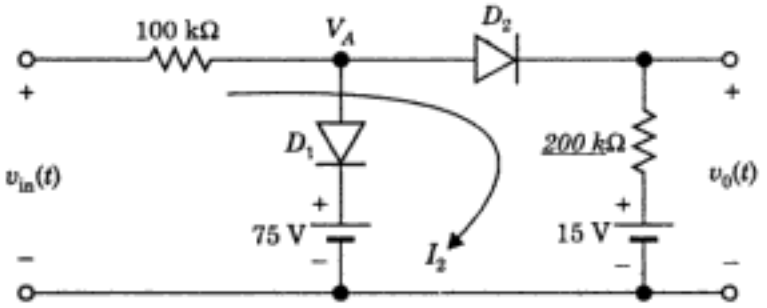


Fig. 3.57(a) The given circuit, Ex. 3.26.

Solution As $v_{in}(t)$ increases from 0 to 120 V, clearly D_2 will conduct first (at v_{in} = 15 V). To find this, let D_2 be ON and D_1 OFF and current I_2 flow as shown. For D_2 to conduct, I_2 must be positive. We have

$$v_{in} - 15 = (100 + 200)I_2$$

$$\therefore \quad I_2 = \frac{v_{in} - 15}{300}$$

I_2 is +ve for $v_{in} > 15$ V.

When $v_{in} < 15$ V, then D_1 and D_2 are both OFF,

and $v_0 = 15$ volts. (due to battery voltage)

When $v_{in} > 15$ V, and assuming D_1 is OFF,

then $v_0 = v_{in} - 100I_2$

$$= v_{in} - 100\left(\frac{v_{in} - 15}{300}\right)$$

$$\therefore \quad v_0 = \frac{2}{3}v_{in} + 5$$

(shown as straight line AB in Fig. 3.57(d)) (*i*)

When $v_0 = V_A = 75$, then D_1 as well as D_2 are ON, and $v_0 = 75$ V. From Eq. (*i*) for $v_0 = 75$,

$$v_i = (75 - 5) \times \frac{3}{2} = 105 \text{ V}$$

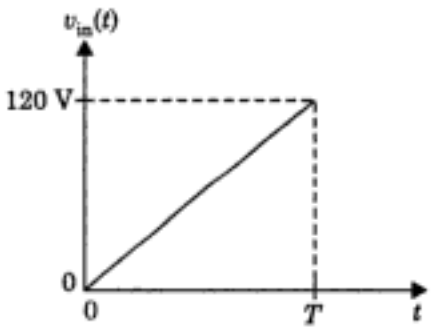
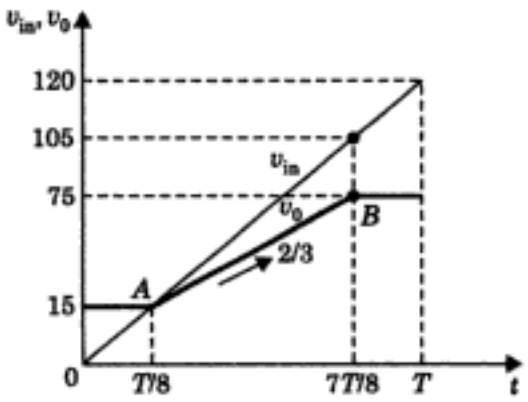


Fig. 3.57(b) Input voltage $v_{in}(t)$ applied to the given circuit.

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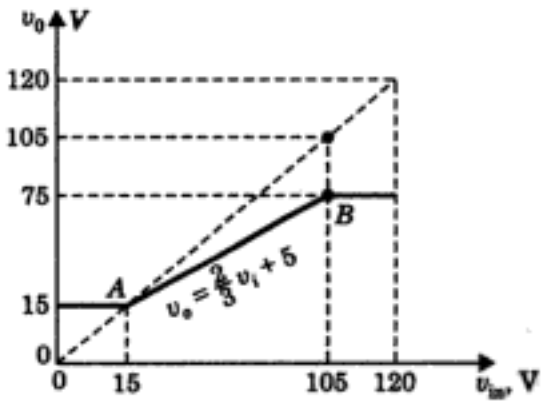


(c)

$v_{in} < 15$ V, $v_0 = 15$ V

$15 < v_{in} < 105$, $v_0 = \frac{2}{3} v_{in} + 5$

$v_{in} > 105$, $v_0 = 75$ V



(d) Transfer characteristic (v_{in} versus v_o)

Fig. 3.57 (c) Curves showing v_{in} and v_o from time $t = 0$ to T, (d) The resulting transfer characteristics.

EXAMPLE 3.27

Assume that the diodes are ideal. Make a plot of v_0 versus v_{in} for the range of v_{in} from 0 to 50 V. Indicate for each region which diodes are conducting.

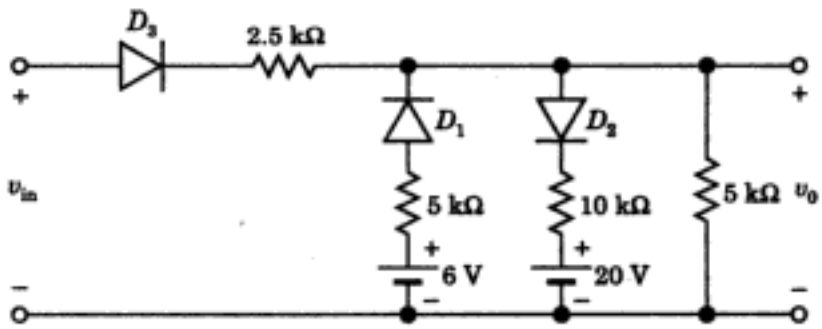


Fig. 3.58(a) The given circuit, Ex. 3.27.

Solution *When* $v_{in} < 3$ *V*, D_1 ON, D_2, D_3 OFF (see Fig. 3.58(b))

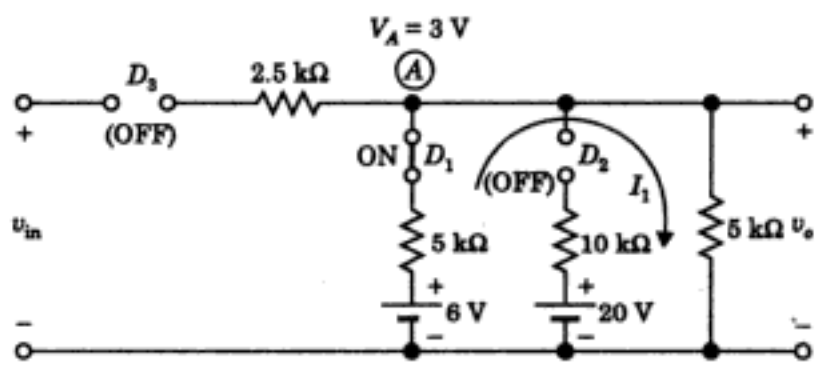


Fig. 3.58(b) $v_0 = 3$ V for $v_{in} < 3$ V, D_1 ON, D_2, D_3 OFF.

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$$I_1 = \frac{6}{5+5} = \frac{6}{15}\text{ mA}$$

$$V_A = \frac{6}{10} \times 5 = 3\text{ V}$$

For $v_{in} < 3$ V, D_3 remains OFF. Also D_2 is OFF due to reverse bias. Here $v_0 = 3$ V is constant. (see part of curve *AB* in Fig. 3.58(f).

When $v_i \geq 3$ *V*

Let D_1, D_3 be ON, D_2 OFF. (see Fig. 3.58(c)) To find range of v_{in} where I_3 and I_1 remain +ve,

$$I_3 = \frac{(v_{in} - V_A)}{2.5} \tag{1}$$

$$I_1 = \frac{(6 - V_A)}{5} \tag{2}$$

$$V_A = (I_1 + I_3) \,.\, 5 \tag{3}$$

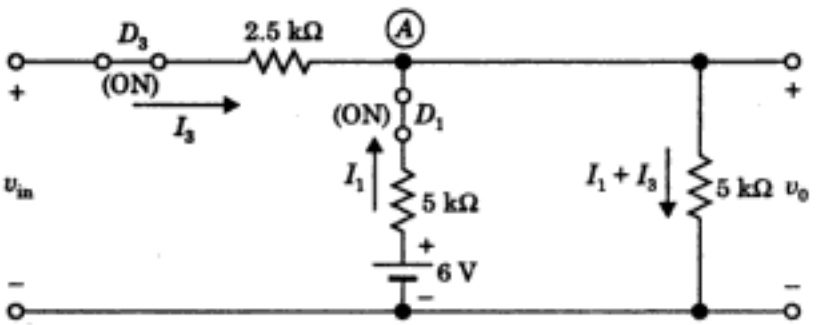


Fig. 3.58(c) D_3, D_1 ON, D_2 OFF, $3 < v_{in} < 9$, $v_0 = \frac{1}{2}v_{in} + \frac{3}{2}$.

From Eqs. (1) and (3),

$$I_3 = \frac{1}{2.5}[V_{in} - (I_1 + I_3).5]$$

i.e., $$2I_1 + 3I_3 = \frac{v_{in}}{2.5} \tag{4}$$

From Eqs. (2) and (3),

$$I_1 = [6 - (I_1 + I_3) \,.\, 5]/5$$

i.e., $$2I_1 + I_3 = \frac{6}{5} \tag{5}$$

Solving Eqs. (4) and (5) for I_1 and I_3, we have

$$I_1 = \frac{9 - v_{in}}{10}, \quad I_3 = \frac{v_{in} - 3}{5} \tag{5A}$$

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For I_1 and I_3 to be +ve, $3 < v_{in} < 9$ must hold.

Here $$v_0 = 5(I_1 + I_3) = 5\left[\frac{9 - v_{in}}{10} + \frac{v_{in} - 3}{5}\right] = \frac{1}{2}v_{in} + \frac{3}{2}$$

(see part of curve *BC* in Fig. 3.58(f))

From (5A), it is seen that when v_{in} exceeds 9 V, I_3 remains +ve, i.e., D_3 remains conducting; but I_1 becomes –ve, i.e., D_3 ON, D_1, OFF for $v_{in} > 9$ V.

When $V_{in} > 9$ V, D_3 ON, D_1, D_2 OFF (see Fig. 3.58(d))

Here $$v_0 = \frac{5}{5 + 2.5}v_{in} = \frac{2}{3}v_{in}$$

$$v_0 = 20 \text{ V when } v_{in} = \frac{20 \times 3}{2} = 30 \text{ V}$$

This part is shown as curve *CD* in Fig. 3.58(f).

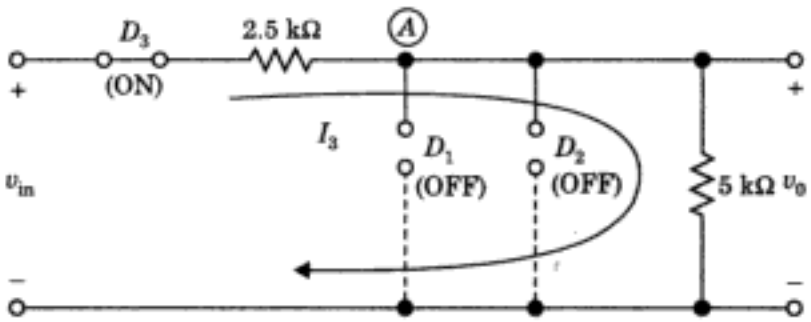


Fig. 3.58(d) D_1, D_2 OFF, D_3 ON, $v_0 = \frac{2}{3}v_{in}$ for $9 < v_{in} < 30$.

Till v_0 (i.e., V_A) reaches 20 V, D_2 remains OFF, D_1 will remain OFF for $v_{in} > 9$.

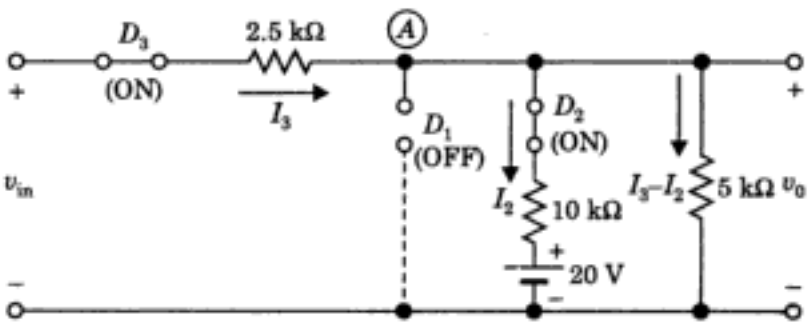


Fig. 3.58(e) D_2, D_3 ON, D_1 OFF $v_{in} > 30$ V, $30 \le v_{in} \le 50$, $v_0 = \frac{4}{7}v_{in} + \frac{20}{7}$.

When $v_{in} > 30$ V, D_3, D_2 ON, D_1 OFF (see Fig. 3.58(e))

$$I_2 = \frac{V_A - 20}{10} \quad \text{(must be +ve)} \qquad (6)$$

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$$I_3 = \frac{v_{in} - V_A}{2.5} \qquad \text{(must be +ve)} \tag{7}$$

$$V_A = (I_3 - I_2)5 \tag{8}$$

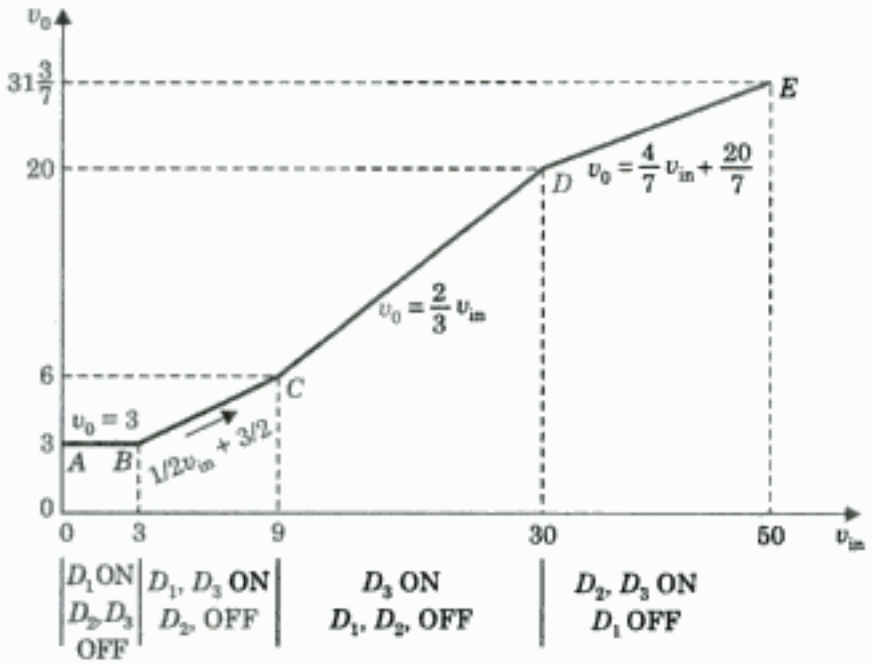


Fig. 3.58(f) Transfer curve (v_{in} versus v_o)

From Eqs. (6) and (8), $$I_2 = \frac{1}{10}[(I_3 - I_2)5 - 20]$$

$\therefore$ $$3I_2 - I_3 = -4 \tag{9}$$

From Eqs. (7) and (8),

$$I_3 = \frac{2}{5}[v_{in} - 5(I_3 - I_2)]$$

$\therefore$ $$2I_2 - 3I_3 = -\frac{2}{5} v_{in} \tag{10}$$

Solving Eqs. (9) and (10), **we obtain**

$$\left.\begin{aligned} I_2 &= \frac{2v_{in} - 60}{35} \quad v_{in} \geq 30 \\ I_3 &= \frac{6v_{in} - 40}{35} \quad v_{in} \geq \frac{20}{3} \end{aligned}\right\} \quad \therefore \quad v_{in} \geq 30 \text{ V}$$

$$v_0 = 5(I_3 - I_2) = \frac{1}{7}(4v_{in} + 20)$$

i.e., $$v_0 = \frac{4}{7} v_{in} + \frac{20}{7} \quad \textbf{Ans.}$$

See curve ***DE*** in Fig. 3.58(f), **for this result.**

3.6.2 Clamping (DC Restorer)

Clamping implies addition or subtraction of a DC voltage in the input waveform. By subtracting (or adding) this DC voltage from the clamped waveform, we can easily recover the original (unclamped) waveform. Thus, a clamper (or clamping network) is one that can clamp (clamp means to fix) a signal to a different DC level. The clamper circuit must have a capacitor, a diode, and a resistive element. However, a clamper circuit can also use an independent DC supply to introduce additional voltage shift. The magnitude of resistance R and capacitance C must be so chosen that the time constant $\tau = RC$ should be large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval when the diode is non-conducting. It is practically sufficient to have RC time constant such that the capacitor will fully charge or discharge in five or six time constants. To understand the principle of clamping, we shall first assume that the diode is ideal.

How do we obtain clamping: Figure 3.59 explains the philosophy of DC level shifting. Here we have used fixed DC batteries of voltages V_1 or V_2. However, we require a circuit capable of producing a DC voltage like a battery and also capable of producing variable dc voltage as per our requirement. We exploit the switching property (ON or OFF) of a diode and charge a capacitor to a voltage and ensure that the voltage across this capacitor remains constant. Thus, this charged capacitor will behave like a battery of Fig. 3.59.

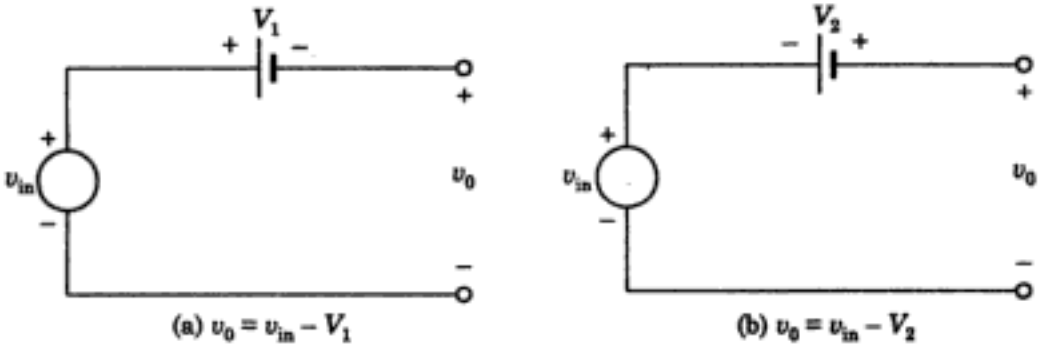


Fig. 3.59 Clamping, how do we add or subtract a DC voltage in input signal.

Consider the circuit given in Fig. 3.60. Note that initially the capacitor C has voltage $V_C = 0$, being uncharged. As soon as v_{in} exceeds V_1 (at $t = t_1$), the diode D starts conducting since

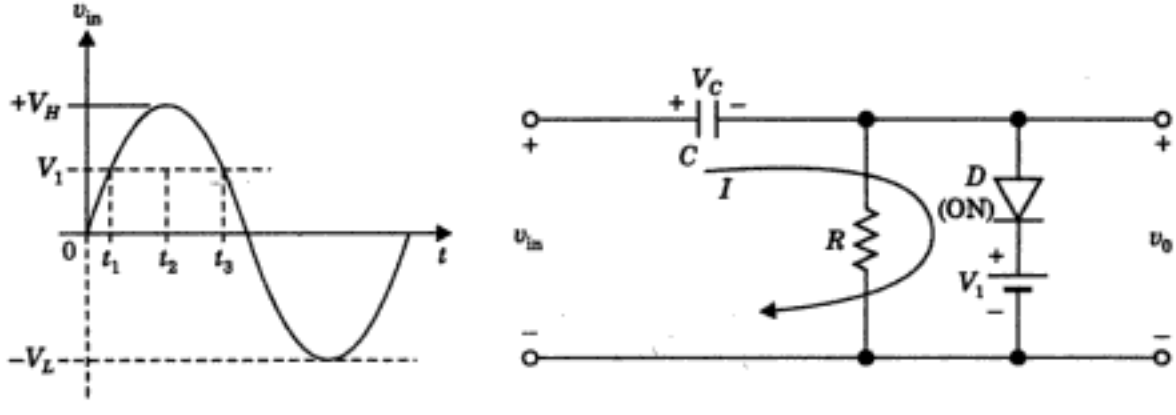


Fig. 3.60 Charging of capacitor C when diode D is ON.

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its anode has potential more than V_1 after t_1 and the diode's cathode is at potential V_1. During diode's conduction, it can be replaced by its forward resistance R_f (which is very small). Thus, the charging current I charges the capacitor C with a time constant CR_f which is extremely small. It enables C to acquire the voltage V_C across it which is almost equal to

$$V_C = v_{in} - V_1, \quad t_1 < t < t_2$$

Hence, at time t_2, when $v_{in} = v_H$, V_C equals $V_H - V_1$ volts. As soon as v_{in} starts decreasing from its hightest value v_H, i.e., for $t > t_2$, the diode cannot continue conducting. For example, assume $V_1 = 2$ V, $V_H = 10$ V and $V_C = 10 - 2 = 8$ V. After t_2. Let v_{in} be 9.5 V. The situation looks as shown in Fig. 3.61. Note that the potential of anode of the diode is 1.5 V and that of the cathode is 2 V. Hence D is OFF, i.e., D is like open circuit. In this situation capacitor C can discharge only through resistor R. But R has a large value, therefore, discharge rate of C is very very low. In other words, we can assume that V_C continues to maintain a constant voltage of $V_H - V_1$ (barring a small decrease due to leakage or discharge). So we have simulated a battery of voltage V_C (= $V_H - V_1$). The output is given by

$$v_0 = v_{in} - V_C$$

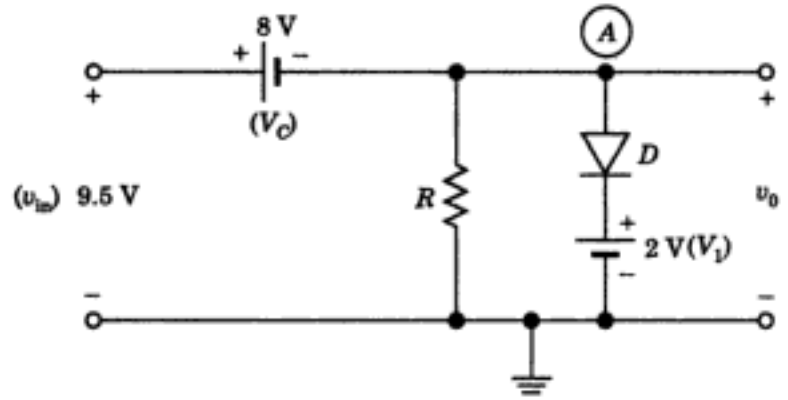


Fig. 3.61 The situation after v_{in} has crossed V_H (Here $V_A = 9.5 - 8 = 1.5$ V).

The output waveform is shown in Fig. 3.62.

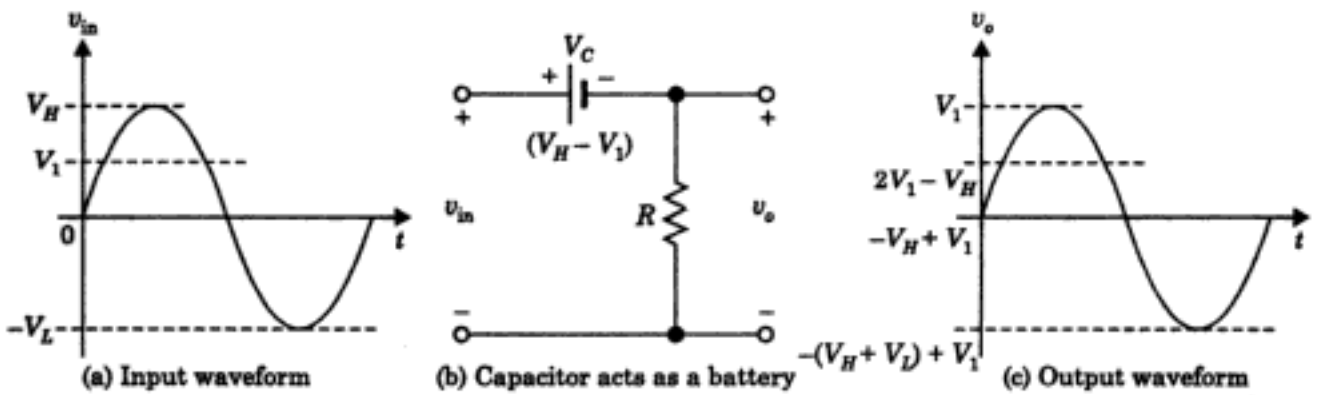


Fig. 3.62 The clamping operation: $v_0 = v_{in} - V_C = v_{in} - (V_H - V_1)$.

To obtain v_o, we use the relation $v_0 = v_{in} - V_c$. In fact we first draw a waveform as v_{in} and just indicate appropriate voltages of vital points. For example, for the circuit shown in Fig. 3.62:

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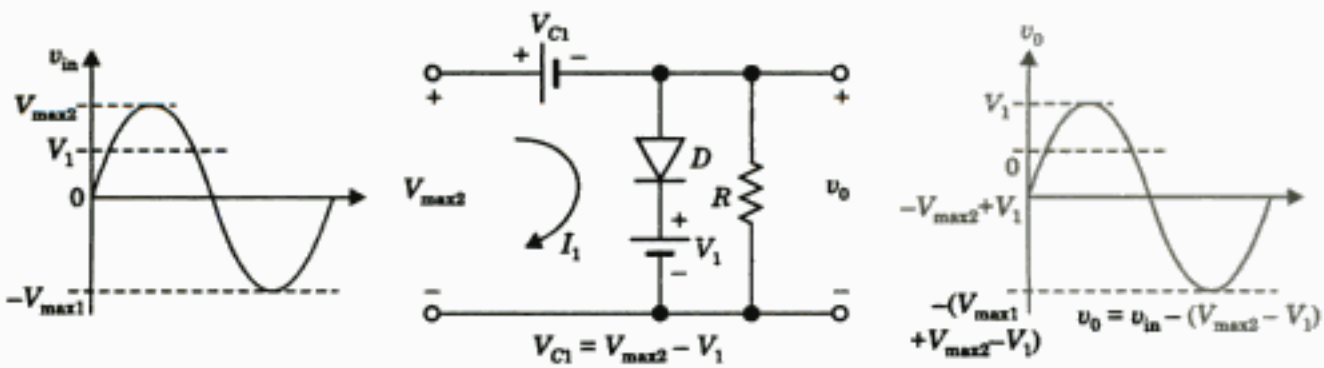
V_H of v_{in} becomes $V_H - (V_H - V_1) = V_1$ volt in v_0
V_1 of v_{in} becomes $V_1 - (V_H - V_1) = 2V_1 - V_H$ in v_0
0 of v_{in} becomes $0 - (V_H - V_1) = -V_H + V_1$ in v_0
$-V_L$ of v_{in} becomes $-V_L - (V_H - V_1) = -(V_H + V_L) + V_1$ in v_0

The above computed values of v_o are shown in Fig. 3.62(c). The above operation also proves that the basic waveforms of v_{in} and v_0 are just the same, only DC voltage is added/subtracted in v_{in} to get v_o. In the above example we have subtracted voltage $(V_H - V_1)$ from v_{in} to obtain v_o.

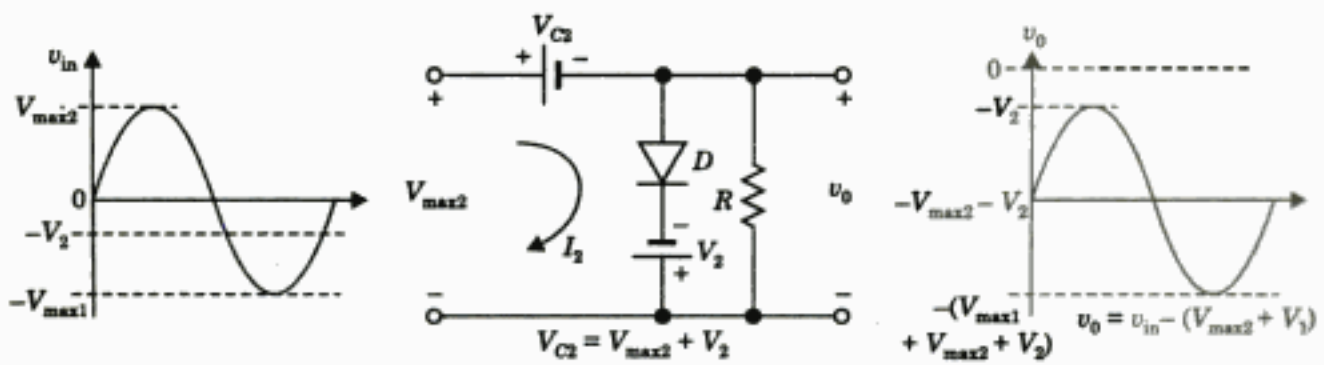
We can extend the aforementioned technique of clamping to any complex waveform. Only we need to find out the voltage V_C first. We also remember that the voltage V_C is the maximum amplitude of the voltage attained by the capacitor C, and V_C is caused by the conduction of the diode (to be ON). We first find the condition when diode D just starts getting ON and determine the maximum or minimum voltage extremum of the input waveform v_{in}. By applying loop condition (KVL) we find the highest (+ve or –ve) value which V_C can attain.

Summary of commonly used clampers:

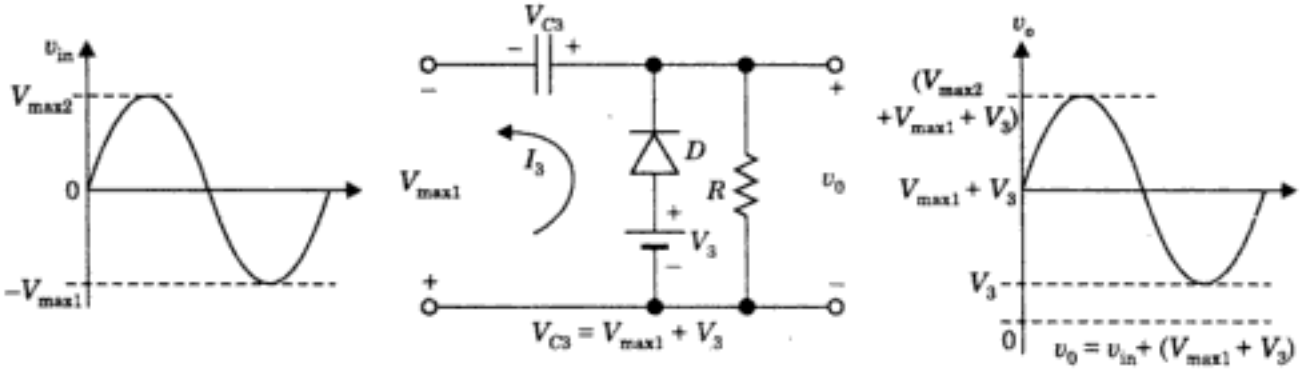
We have shown the currents I_1, I_2, I_3 and I_4 for causing maximum possible voltage V_c across the capacitor. Diodes are assumed ideal with $V_\gamma = 0$ and R_f very very small.



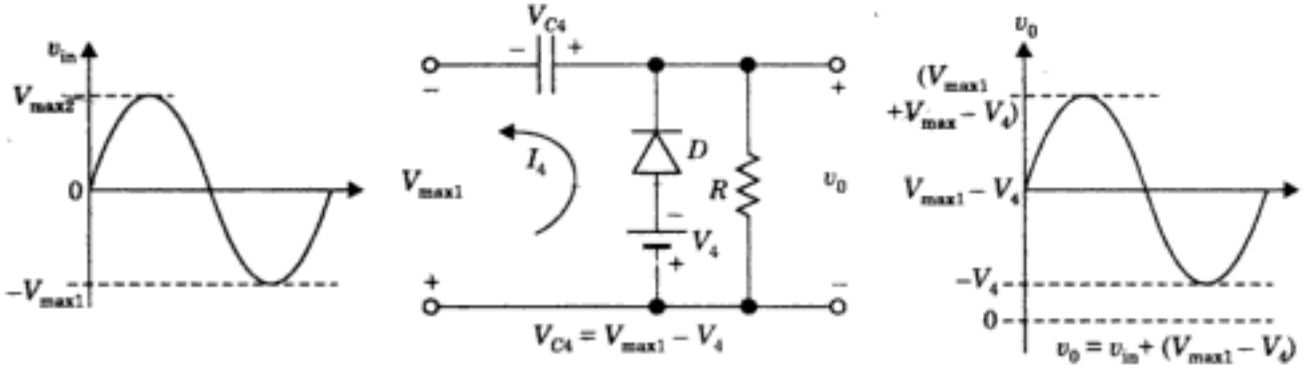
(a)



(b)



(c)



(d)

Fig. 3.63 Clamping for different reference voltages V_1, V_2, V_3, V_4 and diode orientations.

In the four possible clamping circuits shown in Fig. 3.63, we have assumed v_{in} as a generic waveform with positive peaks as V_{max2} and negative peaks on V_{max1}. Note that the v_{in} shown for the clamper circuit are the peak values (V_{max1} or V_{max2}) which causes the diode to conduct and causes maximum voltage to develop across the capacitor.

The necessity of high resistance R in clamper circuits: In practical situations neither are the capacitors non-leaky nor it is feasible to hold constant voltage V_c after once it has appeared across the capacitor. We consider three possible cases.

Case A *Constant peak waveform continues*

Once V_C has been attained, say to a value 8 V for the case when $V_{max1} = V_{max2} = 10$ V and $V_1 = 2$ V (see top clamper circuit in Summary, Fig. 3.63a). After the peak $V_{max2} = 10$ V has passed its peak instant and $V_{C1} = 8$ V achieved, the diode D opens (OFF state) and V_{C1} acts as a "battery" causing clamping action. As time passes, V_{C1} does decrease from 8 V to, say, 7 V due to leakage current. However, V_{C1} again increases from 7 V to 8 V as soon as +ve cycle of the input waveform v_{in} crosses 9 V towards 10 V (i.e., V_{max2}). This way V_{C1} keeps on maintaining values between 8 to 7 V. In general, the actual variation may be even less than taken in this example.

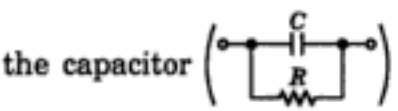
Case B *Input waveform with higher V_{max} arrives later*

If after the present v_{in} (with, say, ±10V maximum values), a changed v_{in} with $V_{max} = \pm 15$V arrives, V_C will immediately increase to the desired value of 13 V (if $V_1 = 2$, top case in summary, Fig. 3.63(a)) with the arrival of first +ve maxima of the new waveform having

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V_{max} = 15 V. This is so because the charging time CR_f is very very small and V_C almost follows the emf in the charging circuit. See Fig. 3.64, V_C immediately attains a new values V_C+ at peak C for the new v_{in} waveform.

Case C *Input waveform with lower V_{max} arrives later*

V_C is decaying, between the last charging cycle till the new charging period, due to CR time constant (though slow). It should *not increase* for the incoming waveform with lower V_{max} which follows. It will go on decreasing due to discharging via resistor R, till it has come down sufficiently to attain the lower values of V_c^- to match the new input waveform with lower V_{max}. (see Fig. 3.64c, V_C^+ misses E and F peaks and stabilities at G). In some circuits we may also put a resistance across the capacitor 

to allow fast discharge if we expect variable shape of incoming waveforms. This is the case in radars, sonars and TV circuits. Figure 3.64 explains the variation of V_C for the cases A, B and C described earlier.

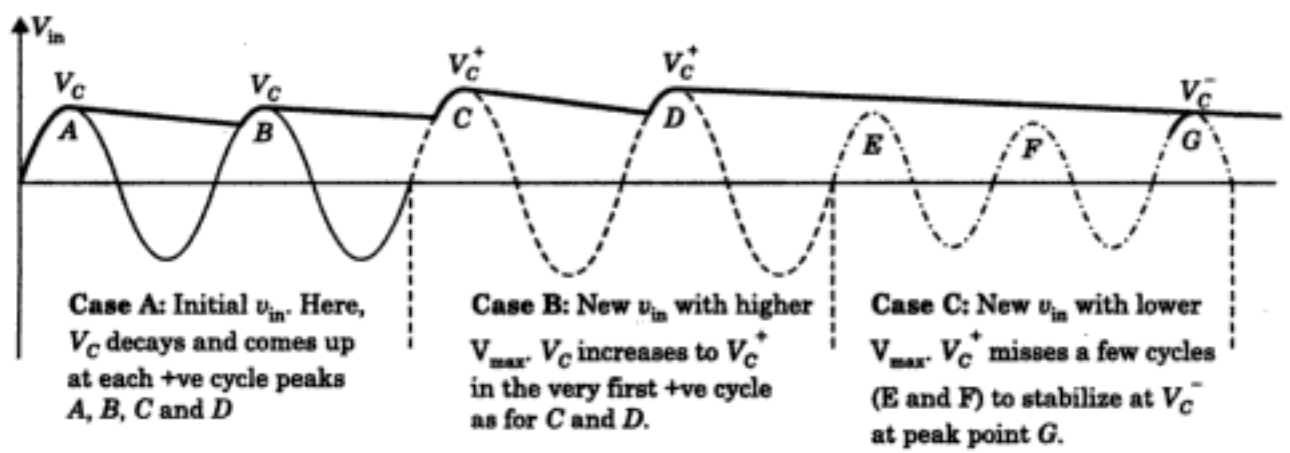

V_{in}
V_C
A
V_C
B
V_C^+
C
V_C^+
D
E
F
V_C^-
G
Case A: Initial v_{in}. Here, V_C decays and comes up at each +ve cycle peaks A, B, C and D
Case B: New v_{in} with higher V_{max}. V_C increases to V_C^+ in the very first +ve cycle as for C and D.
Case C: New v_{in} with lower V_{max}. V_C^+ misses a few cycles (E and F) to stabilize at V_C^- at peak point G.

Fig. 3.64 Variation of V_C for three cases of V_{in} variations. The slant straight lines from $A \rightarrow B \rightarrow C \rightarrow \ldots G$ indicate the decay path of capacitor voltage V_C.

EXAMPLE 3.28

Sketch the output voltage $v_0(t)$ in the circuit shown in Fig. 3.65(a) for $0 \le t \le 5$ ms, assuming that the diode is ideal.

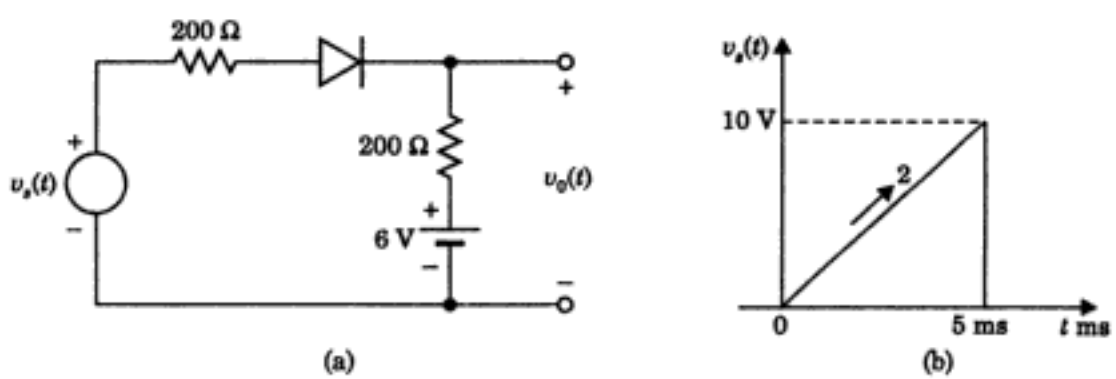


Fig. 3.65 (a) Given circuit, (b) Given $v_s(t)$, Ex. 3.28.

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Solution When the diode is OFF,

$$v_0(t) = 6 \text{ V} \quad \text{(due to the battery voltage)}$$

When $v_s > 6$ V

The diode can conduct, as shown in Fig. 3.65 (c)

$$i = \frac{v_s - 6}{400}$$

$$\therefore \quad v_0(t) = 6 + i \times 200$$

$$= 6 + \frac{v_s - 6}{400} \times 200 = 6 - 3 + \frac{1}{2} v_s$$

$$= 3 + \frac{1}{2} v_s$$

At $t = 5$ ms, $v_s = 10$

$$\therefore \quad v_0(t)\big|_{t=5 \text{ m sec}} = 3 + \frac{1}{2} v_s(t)\big|_{t=1}$$

$$= 3 + \frac{1}{2} \times 10 = 8 \text{ V}$$

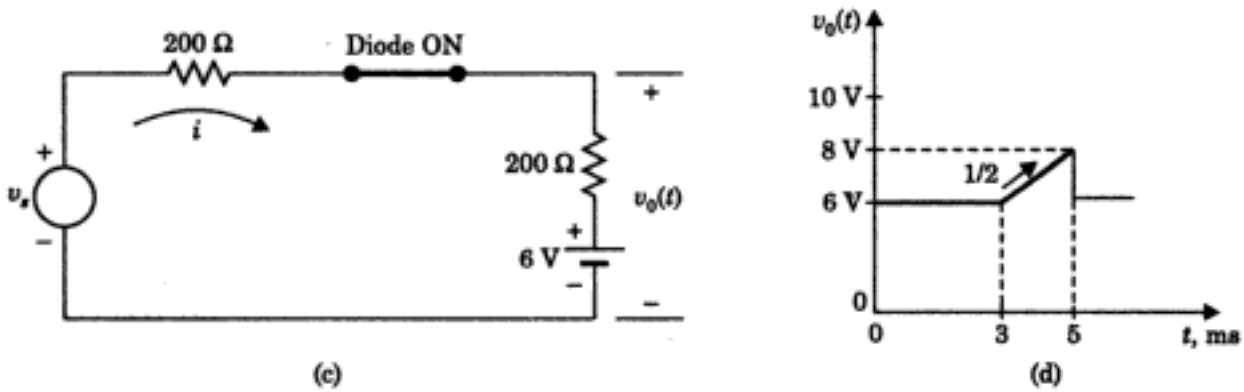


Fig. 3.65 (c) When diode conducts $i = (v_s - 6)/400$, (d) $v_0(t)$ for this circuit.

Thus, $v_0(t)$ is as shown in Fig. 3.65(d), i.e.

$$v_o(t) = \begin{cases} 6V, & v_s < 6V \\ 3 + \frac{1}{2} v_s, & v_s \geq 6V \end{cases}$$

EXAMPLE 3.29

Repeat Problem 3.28, given that the diode is represented by $V_\gamma = 0.5$ V and $R_f = 50\ \Omega$.

Solution The circuit for the non-ideal diode is shown in Fig. 3.66(a).

When $v_s(t) < 6.5$ V, i cannot pass as diode is reverse biased.

$$\therefore \quad v_0 = 6 \text{ V} \quad \text{(due to the battery voltage)}$$

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When $v_s(t) \geq 6.5$ V, diode conducts

$$i = \frac{v_s - 6.5}{260 + 50 + 200} = \frac{v_s}{450} - \frac{6.5}{450}$$

$$v_0(t) = 6 + i \times 200$$

$$= 6 + 200\left(\frac{v_s}{450} - \frac{6.5}{450}\right) = 3.11 + \frac{4}{9}v_s$$

At $v_s(t) = 6.5$ V, $t = \frac{6.5}{2} = 3.25$ ms

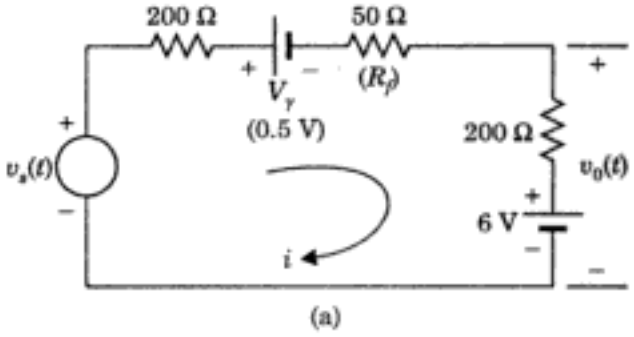


Fig. 3.66(a) Circuit for non-ideal diode, Ex. 3.20.

Thus, v_s/v_0 characteristic curve is shown in Fig. 3.66(b)

At $v_s = 10$ V

$$v_0 = 3.11 + \frac{4}{9} \times 10 = 7.55 \text{ V}$$

The time-wise response is illustrated in Fig. 3.66(c).

Hence we here have

$$v_o(t) = \begin{cases} 6\,V, & v_s < 6.5\,V \\ 3.11 + \frac{4}{9}v_s, & v_s \geq 6.5\,V \end{cases}$$

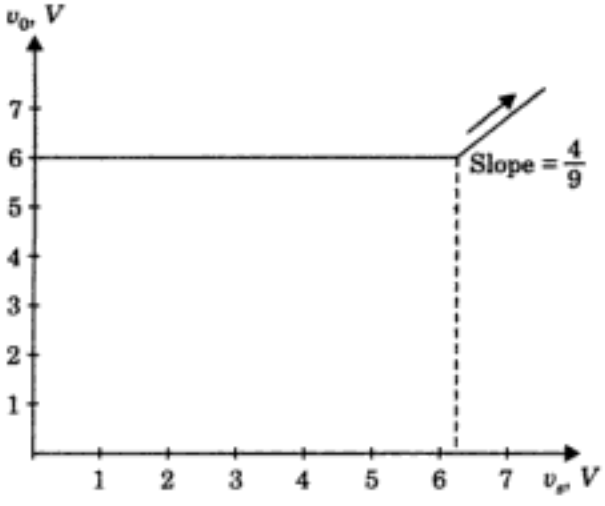


Fig. 3.66 (b) v_0 versus v_s.

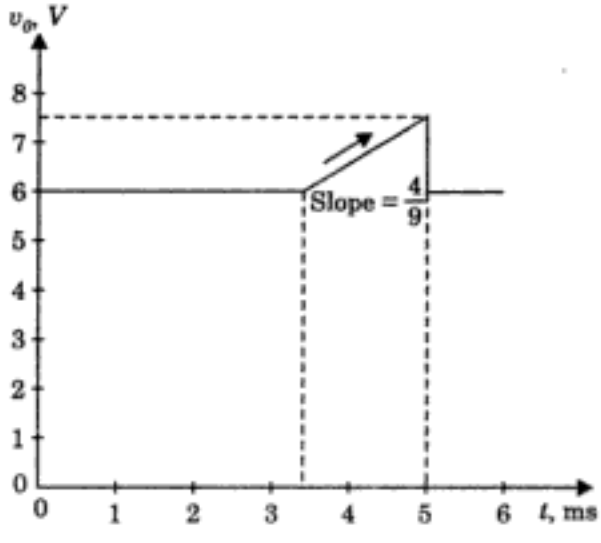
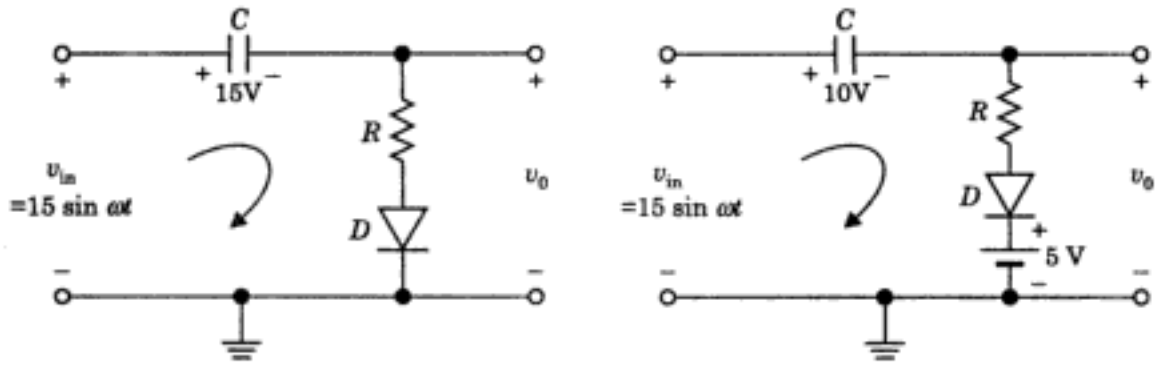


Fig. 3.66 (c) $v_0(t)$ versus t.

EXAMPLE 3.30

Explain the working of the following circuits given in Fig. 3.67 and sketch the output waveform. Assume that the diode is ideal and the input voltage v_{in} is a sinusoidal wave with $V_{max} = 15$ V.

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(a) Top peak clamper (b)

Fig. 3.67 Given circuit Ex. 3.30.

Solution (a) Let input be $v_{in} = 15 \sin \omega t$. This is a top peak clamping circuit. The peak voltage v_0 cannot exceed zero voltage. We assume CR much smaller than $(2\pi/\omega)$. Whenever D conducts, though for an extremely small time, C charges through R to +15 V. Thus, C acts as an opposing battery for v_{in} to give $v_{in} - 15 = v_o$.

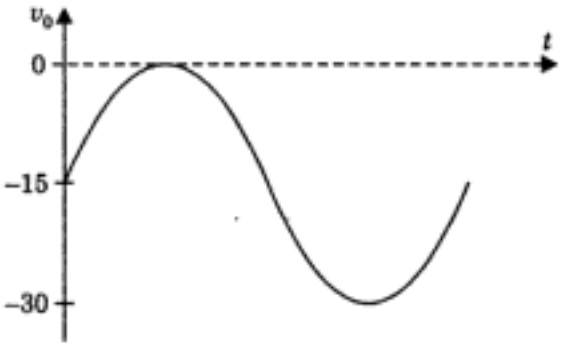


Fig. 3.68(a) Output v_o, top clamped to 0 V. ($v_o = v_{in} - 15$)

(b) Here C charges to a voltage of

$$15 - 5 = +10 \text{ V}$$

$$\therefore \quad v_0 = v_{in} - 10 \text{ V}$$

i.e., $v_{0\,max} = 15 - 10 = +5$ V

$v_{0\,min} = -15 - 10 = -25$ V. **Ans.**

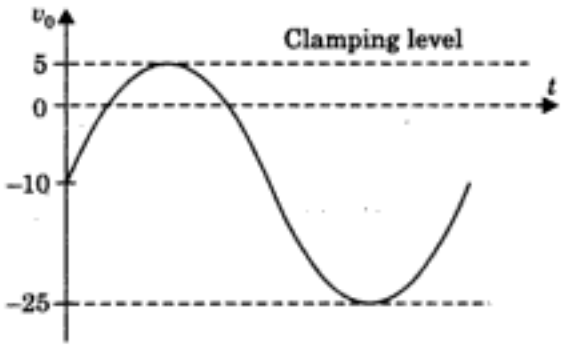


Fig. 3.68(b) Output v_o, with top clamped to 5 V. ($v_o = v_{in} - 10$)

EXAMPLE 3.31

For the DC restorer circuit shown in Fig. 3.69, plot the output voltage versus time waveform.

Solution Assume ideal diode D. Consider the situation from t_1 to t_2. In this time D is forward biased and the capacitor gets charged to a voltage:

$$V_C = +20 + 5 = +25 \text{ V}$$

Thus, in the subsequent waveform a battery of voltage +25 V gets 'series connected' to v_{in}

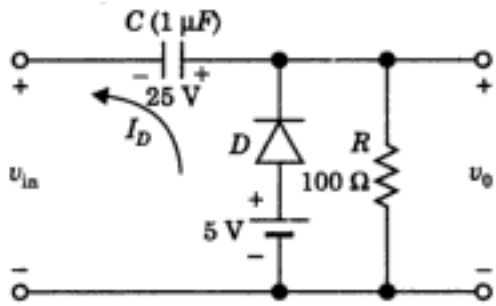


Fig. 3.69(a) DC restorer circuit, Ex. 3.31.

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i.e., $v_0 = v_{in} + 2$

Hence, v_0 is as shown in Fig. 3.70. **Ans.**

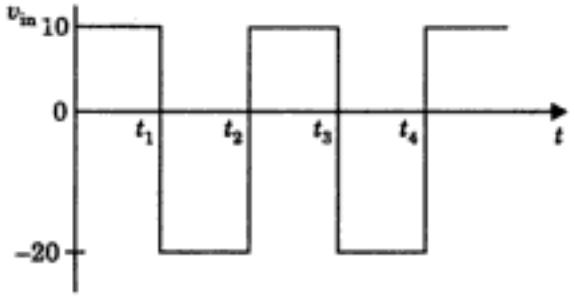


Fig. 3.69(b) Input v_{in} to the DC restorer.

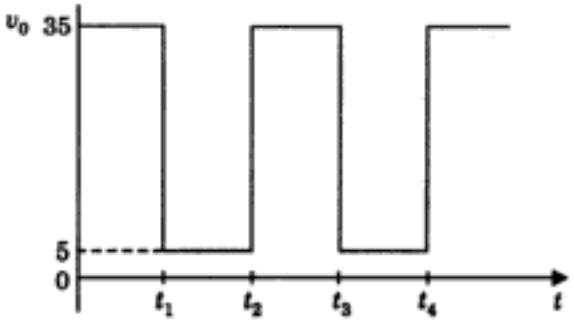


Fig. 3.70 Output voltage versus time waveform ($v_o = v_{in} + 25$).

We have assumed an ideal capacitor C. However, C may slowly get discharged but recuperates during each conducting times such as t_1 to t_2, t_3 to t_4, .., t_{2k+1} to t_{2k+2}.

EXAMPLE 3.32

Plot the output waveform $v_0(t)$ in the clamping circuit shown in Fig. 3.71, with $v_{in}(t)$ as shown:

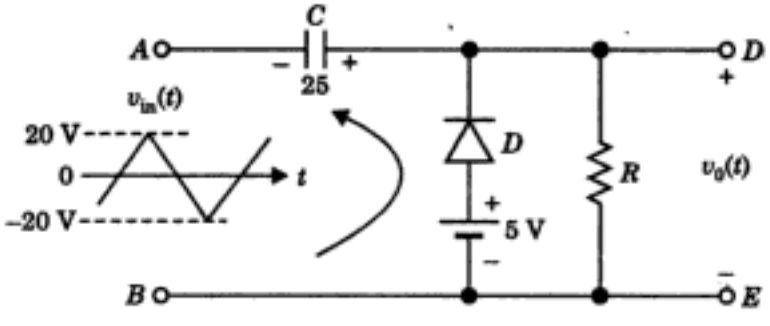


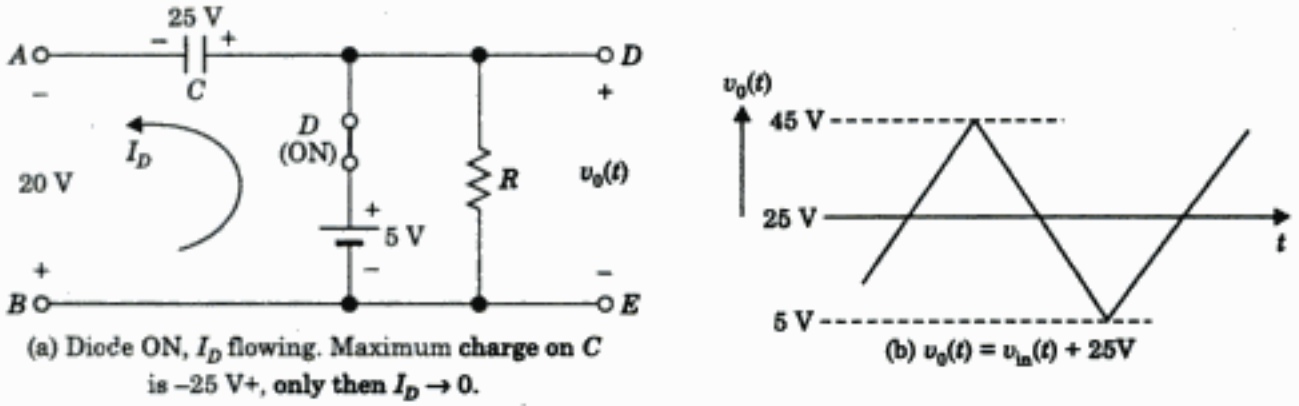
Fig. 3.71 Given clamping circuit, Ex. 3.32

Solution Here, diode D conducts whenever voltage $v_{in}(t)$ is below +5 V i.e. $V_{BA} = 5$ V. The minimum $v_{in}(t)$ is –20 V. The D is ON as long C charges to a voltage such that I_D is positive. Clearly, C must charge to a maximum voltage of –25 V to cause $I_D = 0$. Henceforth

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$$v_0(t) = v_{in}(t) + 25$$

$v_0(t)$ is as shown in Fig. 3.72. We have assumed an ideal capacitor C and a very high value of resistance R.



(a) Diode ON, I_D flowing. Maximum charge on C is –25 V+, only then $I_D \to 0$.

(b) $v_0(t) = v_{in}(t) + 25V$

Fig. 3.72 (a) Conduction of diode D and charging of C (b) Output voltage $v_o(t)$.

In fact, the given clamping circuit will clamp all input voltage $v_{in}(t)$ with bottom to +5 V.

EXAMPLE 3.33

For the circuit shown in Fig. 3.73, determine v_0, for $v_{in} = 10 \sin \omega t$.

Solution $v_{in} = 10 \sin \omega t$

Let $v_{in} + 5 = v_{in}' = 10 \sin \omega t + 5$

Then $v_o = v_{in}' + V_C$

$0 < t < t_1$

$V_C = 0$ initially. So till C remains uncharged, $v_0 = v_{in}'$ from time $0 < t < t_1$. (see curve ABC in Fig. 3.74)

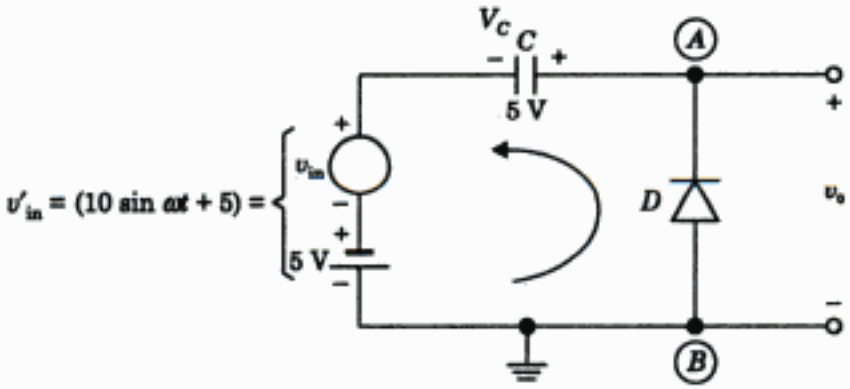


Fig. 3.73 The given circuit, Ex. 3.33.

At t_{1+}

v'_{in} is –ve. Therefore, D is ON and now onwards and $v_0 = 0$, (see curve CD in Fig. 3.74) and V_C follows v_{in}'.

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At t = (3/4)T

V_C has charged to +5 V as shown polarity.

t > (3/4)T

Assuming capacitor C lossless (ideal), a voltage +5 V is retained by C. Diode D cannot conduct since $(v_{in}' + 5)$ never becomes –ve, i.e., point A never goes –ve w.r.t. B, since the least value of $v_{in}' + 5 = 10 \sin \omega t + 5 + 5 = 0$.

Henceforth $v_0 = v_{in}' + v_C = 10 \sin \omega t + 5 + 5 = 10 \sin \omega t + 10$. (see curve *DEF* ... in Fig. 3.74)

Figure 3.74 depicts a sin waveform shifted up by 10 V with peaks at 20 V and troughs at 0 V after $t = (3/4)T$.

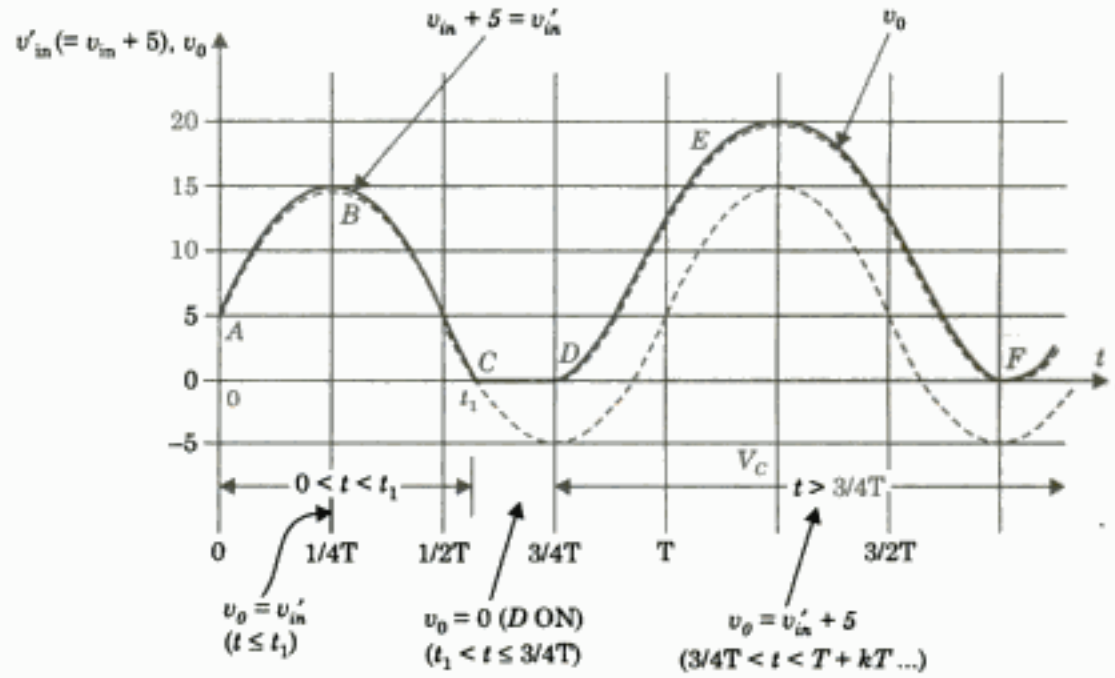


Fig. 3.74

The output waveform is bottom clamped to zero voltage, and is essentially a sine wave. After point $D(t = 3/4T)$ onward, the output v_o remains sine wave with an addition of 5 V.

EXAMPLE 3.34

With the clamping circuit and V_{in} shown in Fig. 3.75 explain step by step the operation of positive swing and negative swing clamping.

Solution (a) *Top (Positive Swing) Clamping Circuit*

From *a* to *b*: *B* swings +ve, diode conducts to hold the potential of *B* at zero volts (since *D* now conducts). Capacitor charges to V_C = V.

From *b* to *c*: *B* remains at zero volts (+ve voltage of input and –ve voltage across *C* neutralizes)

From *c* to *d*: *B* swings –ve and the diode cuts off (Input = 0 V, Output = 0 – V_C = –ve volt)

From d to a: B rises almost negligibly because of the long CR time-constant.

From a to b: B swings +ve, diode conducts near to the peak of the swing. (C restores its last charge if any)

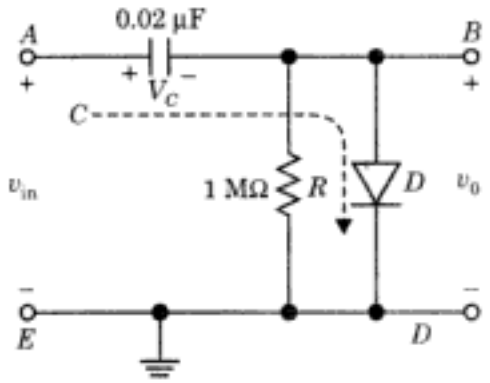


Fig. 3.75 Given circuit, Ex. 3.34.

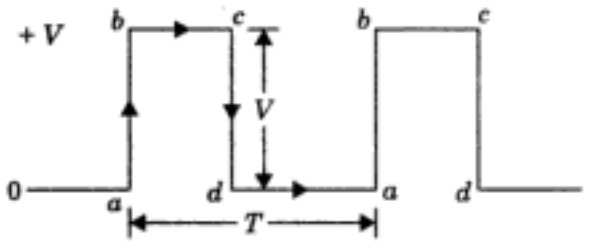
Note: If time constant CR is reduced, the output waveform is still clamped to zero, but the output now rises appreciably from d to a as shown in (*c*). For the circuit shown

$$CR = (0.02 \times 10^{-6})\ (1 \times 10^{6}) = 0.02 \text{ seconds} = 2 \text{ m seconds.}$$

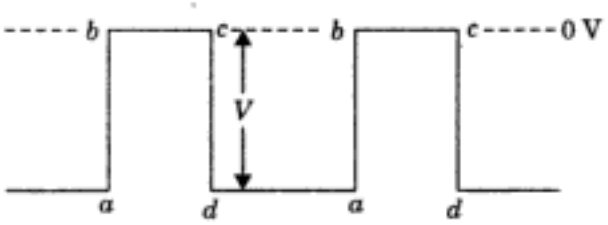
If $T \leq 0.01$ m second, then clamping is fairly good

($\because$ here $e^{-T/CR} = e^{-0.01/2} = e^{-0.005} = 0.995$ $\therefore$ decay of only 0.5% in time T)

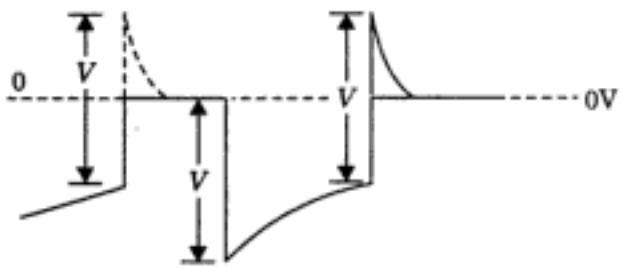
If T lies between 0.01 and 0.2 m seconds, clamping may have some distortion.



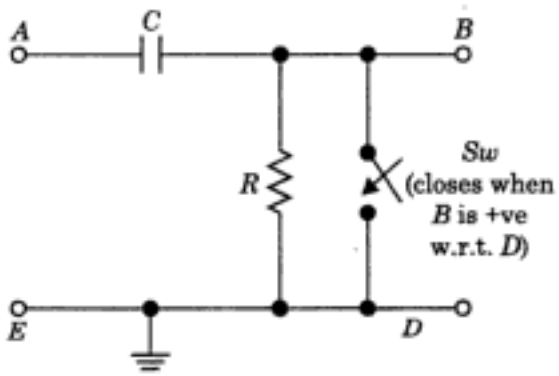
(a) Input v_i



(b) Output v_0 for $CR > T$



(c) Output v_0 for CR > T



(d)

Fig. 3.76 Clamping of positive swings. (a) Input v_i, (b) Output v_o for $CR >> T$, (c) Output v_o for $CR > T$, (d) Action of diode D—ON/OFF.

(b) *Bottom Clamping (Negative Swing Clamping)*

Here, the diode D is reversed and therefore conducts whenever B goes –ve w.r.t. E, making the output $v_0 = 0$ volts. When B is +ve w.r.t. E. Diode is OFF and $v_o = v_i$.

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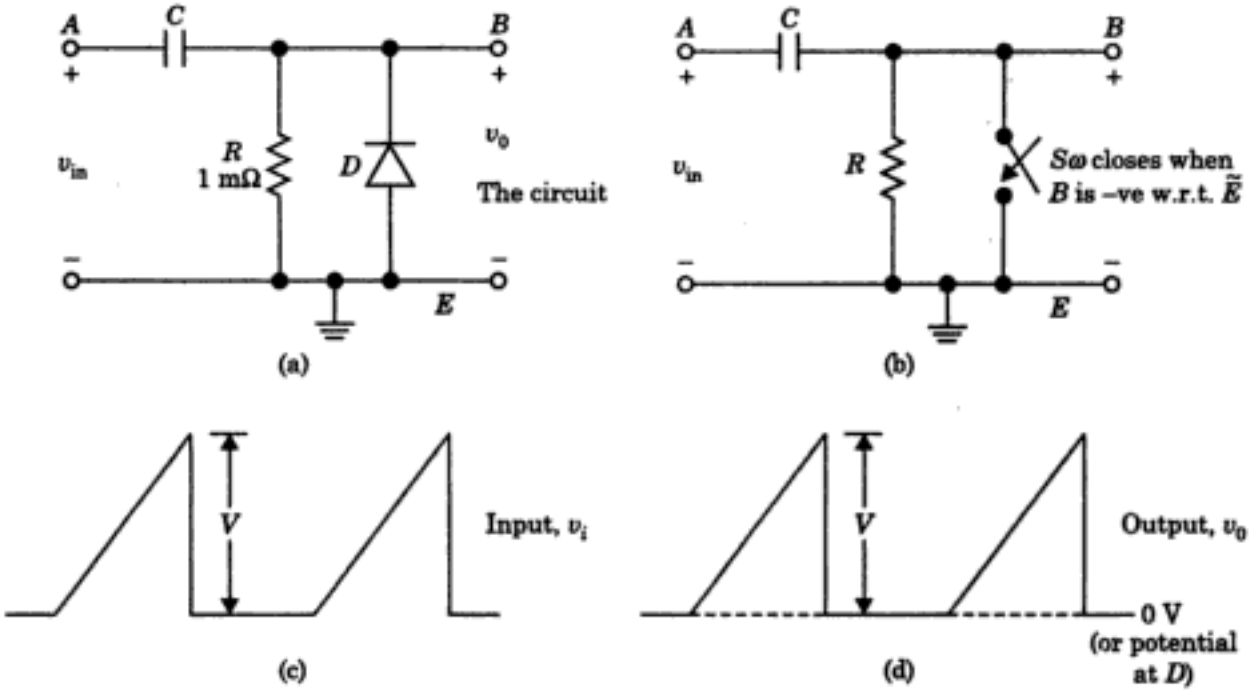


Fig. 3.77 Negative clamping. (a) The clamping circuit, (b) Action of diode D-ON/OFF, (c) Input v_i, (d) Output v_o.

The time constant $CR >> T$ for better performance.

If E is connected to any other voltage than zero, v_o's bottom is clamped to that voltage.

SUMMARY

We have studied various applications of diodes including the zener diode. The following salient points are important:

- Diodes can be used as rectifiers, i.e., half-wave rectifiers and full-wave rectifiers.
- A rectifier converts an AC waveform to a DC waveform.
- A half-wave rectifier uses one diode and allows only alternate +ve half cycles to pass through the diode. The diode has peak inverse voltage (PIV) of V_{max} where the input AC signal is $v_s = V_{max} \sin \omega t$.
- A full-wave rectifier uses two diodes and a centre-tapped transformer. Here each diode has PIV as $2V_{max}$.
- A bridge rectifier uses four identical diodes. It requires no centre-tapped transformer. Each diode in this rectifier has PIV = V_{max}.
- Ripple factor r is a measure of AC ripples in the rectified DC. The value of r is 1.21 (i.e. 121%) for half-wave rectifier and 0.483 (i.e. 48.3%) for full-wave rectifiers.
- Efficiency of half-wave rectifier is 40.5% and that of the full-wave rectifier 81% if we use ideal diodes for rectifiers.

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- A rectifier meter is a Bridge rectifier with its load as the DC (reading average current) ammeter.
- A capacitor filter (a low-pass filter) used in parallel with the load R_L, reduces ripples and helps to obtain almost constant (ripple free) DC output.
- Low-pass filter can be fabricated by using R, C or R, L, C or L, C. However, R-C filters are preferred.
- Voltage multiplier circuit is capable of giving a DC voltage which is multiple of V_{max}, if input $v_s = V_{max} \sin \omega t$.
- A zener diode can be effectively used as a voltage regulator giving a constant output DC voltage of V_Z.
- For effective voltage regulation the unregulated input DC voltage V_{dc} must be greater than V_Z and the value of $(I_{Z\,max} - I_{Z\,min})$ must be more than $(I_{L\,max} - I_{L\,min})$.
- Clipping circuit (a clipper) clips/removes a part of the input waveform. We can design clippers capable of removing any part of the input waveform.
- The clipped waveform (v_0) is a distorted version of the input waveform (v_{in}). We cannot recover v_{in} from v_0.
- A clamping circuit (a clamper) adds or subtracts a DC voltage in the input waveform v_{in} to yield output waveform v_0. A clamper is also called **DC restorer**.
- We can recover v_{in} (the input waveform) completely from v_0 (the clamped output waveform) by adding/subtracting appropriate value of DC voltage in v_0.

REVIEW QUESTIONS

3.1 Draw a sketch of a half-wave rectifier. Derive the expression for (i) DC current, (ii) rms load current when the diode is not ideal, i.e., $V_\gamma \neq 0$, $R_f \neq 0$.

3.2 Draw a sketch of a full-wave rectifier. Derive the expressions (i) DC current, (ii) DC voltage, (iii) voltage regulation for full-wave rectifier.

3.3 Derive the values of ripple factor r and efficiency η for (a) half-wave rectifier, (b) full-wave rectifier.

3.4 Draw Thevenin model for a full-wave rectifier.

3.5 Sketch the circuit of a Bridge rectifier and explain its operation.

3.6 Sketch the circuit of a rectifier meter and explain its operation. What are its limitations?

3.7 Explain the operation of charging and discharging of a capacitor C through a resistor R and DC source voltage V_{dc}. Assume that the capacitor is initially charged to voltage V_{co} before additional charging via a switch K.

3.8 Explain the operation of an RC low pass filter. How does it remove ripple and stabilize the output DC voltage?

3.9 By approximate analysis in an RC low pass filter, determine the Thevenin equivalent of the power supply.

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3.10 Draw a sketch of a voltage doubler. Clearly explain how the doubling of voltage results?

3.11 Repeat 3.10 for a voltage trippler and voltage quadrupler.

3.12 Explain the theory behind the voltage regulation achieved by using a zener diode. What are the necessary conditions to accomplish a reliable voltage regulation?

3.13 What is a Clipper? How can we realize

(i) upper part of input waveform above voltage V_1

(ii) lower part of input waveform below voltage V_2

(iii) output waveform clipped above V_1 and below V_2 simultaneously

3.14 What is a clamping operation? Give simple circuits to get

(i) top clamped to voltage V_1, take $V_1 = 0, -2$ V, +5 V

(ii) bottom clamped to voltage V_2, take $V_2 = 0, -2$ V, 5 V

NUMERICAL PROBLEMS

P3.1 The circuit in Fig. 3.78 implements a complementary-output rectifier. Sketch and clearly label the waveforms of v_0^+ and v_0^-. Assume a 0.7 V drop across each conducting diode. If the magnitude of the average of each output is to be 15 V, find the required amplitude of the sine wave across the entire secondary winding. What is the PIV of each diode?

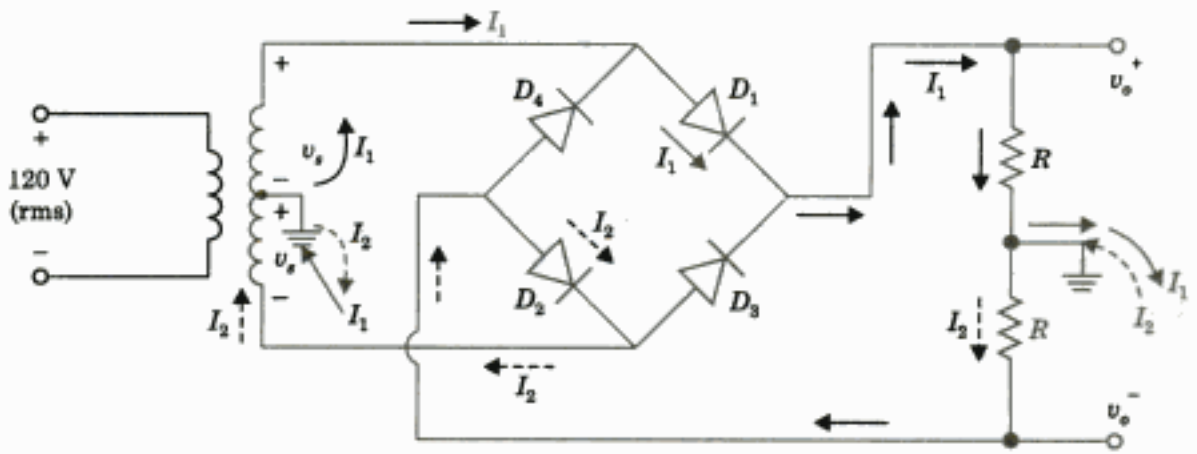


Fig. 3.78 The given figure of complementary rectifier, P3.1.

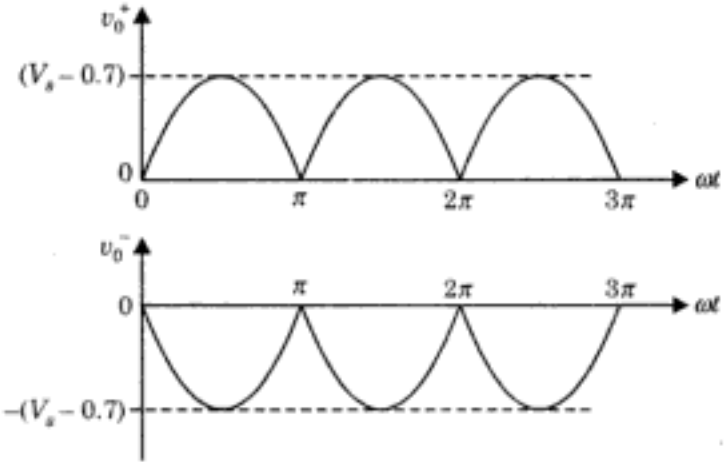
Hint. Let $v_s = V_S \sin \omega t$

The sketches of v_0^+ and v_0^-, assuming that the voltage drop across the conducting paths is 0.7 V.

$$v_0^+\big|_{\text{average}} = \text{Average of } (V_s - 0.7)$$

$$\therefore \quad +15 = \frac{V_s}{\pi/2} - 0.7$$

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$$\therefore \qquad V_s = (15 + 0.7) \times \frac{\pi}{2} = 24.66 \text{ V}$$

$\therefore$ Voltage across the secondary = $2V_s$ = 2 × 24.66 = 49.32 V peak

Let D_1 and D_2 conduct as shown. Then D_3 and D_4 are reverse biased. The voltage across D_4 is $2V_s$ (PIV) = 2 × 24.66 = 49.32 if there were no drop in the conducting paths. As given in the question, there is a voltage drop of 0.7 V in the conducting path. Thus the effective PIV here is 49.32 – 0.7 = 48.62 V. For a safe design we choose diode with PIV of 75 V).

P3.2 A full-wave rectifier uses diodes with forward resistance of 1 Ω each. The transformer secondary is centre-tapped with output 10-0-10 V (rms) and has resistance of 5 Ω for each half section. Calculate:

(a) No load DC voltage; (b) DC output voltage at a load of 100 mA, (c) Percentage regulation at 100 mA; (d) Efficiency, (e) Ripple voltage across the load, (f) PIV of each diode.

[Ans: (a) No load V_{dc} = 9.00316 V, (b) With load $V_{dc} = V_{\text{load}}$ = 8.40316 V, (c) % regulation = 7.14%, (d) Full-wave rectification efficiency = 75.8%, (e) Ripple voltage = 0.483 times I_{dc}, (f) PIV = 28.28 V]

P3.3 For the following circuit, find (i) the maximum and (ii) the minimum value of zener diode current.

[Ans: (i) $I_{Z\,\max}$ = 9 mA, $I_{Z\,\min}$ = 1 mA]

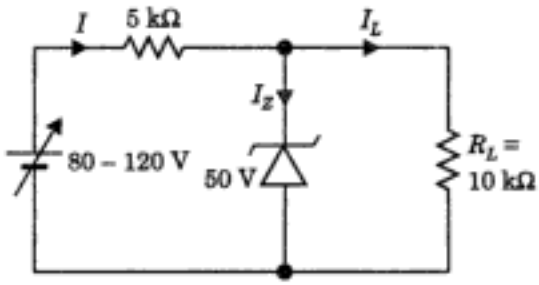


Fig. 3.79 Circuit for P3.2

P3.4 A zener diode with safe zener currents from 1 mA to 5 mA and V_Z = 40 V is used in a power supply regulator meant to give load current of 0 to 8/3 mA. The series resistance is 5 kΩ. What values of unregulated DC voltage can be tolerated to maintain constant load voltage of 40 V?

[Ans. $58\frac{1}{3}$ V to 65 V]

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P3.5 A zener diode with safe zener currents from 2 mA to 10 mA and $V_Z = 40$ V is used in a power supply regulator meant to give load current of zero to 4 mA. The series resistance R_S is 4 kΩ. What value of unregulated DC voltage V_{DC} can be tolerated to maintain a constant load voltage of 40 V?

[Ans. 64 V to 80 V]

P3.6 The circuit shown in Fig. 3.80 is designed with $R_S = 20\ \Omega$. The 5.6 V zener diode provides regulation for 1 mA ≤ I_Z ≤ 300 mA and for a load current of 0 ≤ I_L ≤ 200 mA. Determine the range of amplitudes of the unregulated supply for which the load remains regulated.

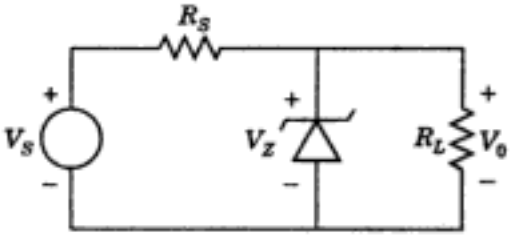


Fig. 3.80 Circuit for P3.6.

[Ans: V_S varies from 9.62 V to 11.6 V]

P3.7 A zener voltage regulator has variable load R_L requiring I_L from 10 mA to 85 mA. With zener diode having $V_Z = 10$ V, $I_{Z\min} = 15$ mA, $I_{Z\max} = 100$ mA, the regulator has $R_S = 40\ \Omega$. Calculate the range of V_{dc} variation permissible. Also, find the zener dissipation power $P_{Z\max}$.

[Ans: $P_{Z\max} = 1$ W, $V_{dc} = 14.4$ V to 14 V]

P3.8 A 10 V zener diode is used to regulate the voltage across the variable load R_L. V_{DC} has the range 13 V ≤ V_{DC} ≤ 16 V and load current is 10 mA ≤ I_L ≤ 85 mA. Given $I_{Z\min}$ as 15 mA, calculate: (i) R_S, (ii) zener diode power dissipation P_Z.

[Ans. (i) $R_S = 30\ \Omega$, (ii) $P_Z = 1.9\ \Omega$]

P3.9 Determine and plot the output voltage for the circuit exhibited in Fig. 3.81. Assume all diodes ideal.

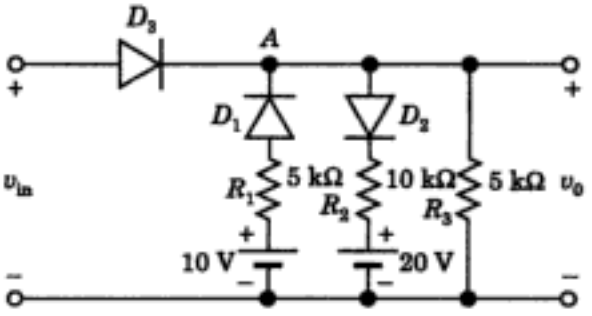


Fig. 3.81 Circuit for P3.9.

Hint. When $v_{in} = 0$, D_1 conducts via 10 V, R_1 and R_3. This gives $V_A = 5$ V, i.e., $v_0 = 5$ V.

Hence D_3 cannot conduct as long as $v_{in} < 5$ V.

$v_{in} < 5$ V D_1 ON, D_3, D_2 OFF

$V_A = 5$ V ∴ $v_0 = 5$ V

$v_{in} > 5$ V D_3 ON, D_1 OFF

As long as $v_{in} < 20$ V, D_2 is also OFF

For $5 < v_{in} < 20$ V, D_3 being ON, $v_0 = v_{in}$

$v_{in} > 20$ V D_3, D_2 ON, D_1 OFF

As $V_A = v_{in} > 20$ V ∴ $v_0 = v_{in}$

Only D_2 is also ON.

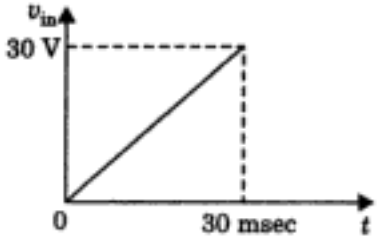


Fig. 3.82 v_i for circuit above.

Here,
$$I_2 = \frac{v_{in} - 20}{10}$$

$$v_0 = v_{in}$$

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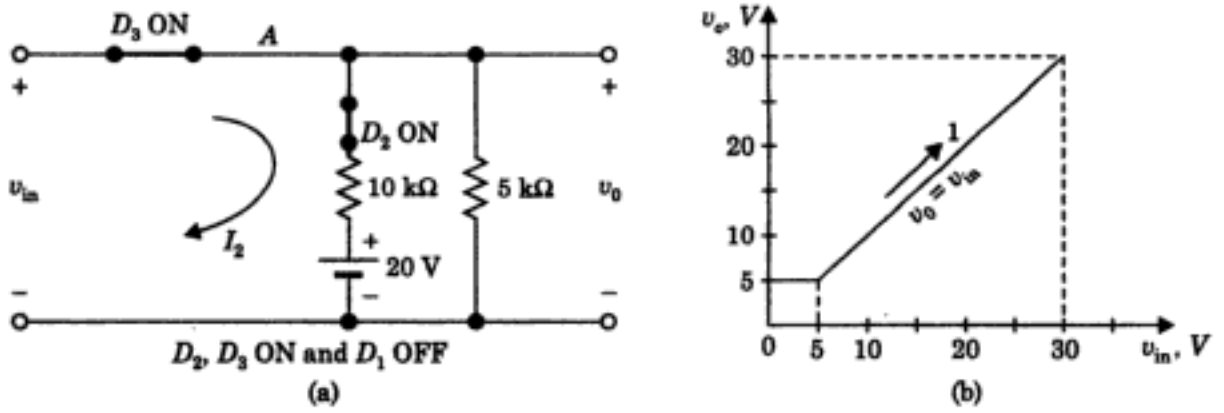


Fig. 3.83 (a) Equivalent circuit when D_2, D_3 are ON and D_1 OFF.
(b) v_{in} – versus v_o graph (Transfer characteristics).

The transfer curve is as shown

$$v_0 = \begin{cases} 5\,V, & v_{in} < 5\,V \\ v_{in}, & v_{in} > 5\,V \end{cases} \quad \textbf{Ans.}$$

P3.10 For the circuit shown in Fig. 3.84, draw the transfer characteristic.

Hint. ***D_1, D_2 both ON***

Not possible, since D_1 requires voltage at $A \geq 2$ V. If it is so then D_2 cannot conduct.

D_1 ON, D_2 OFF

Here current I_1 flows and must be +ve

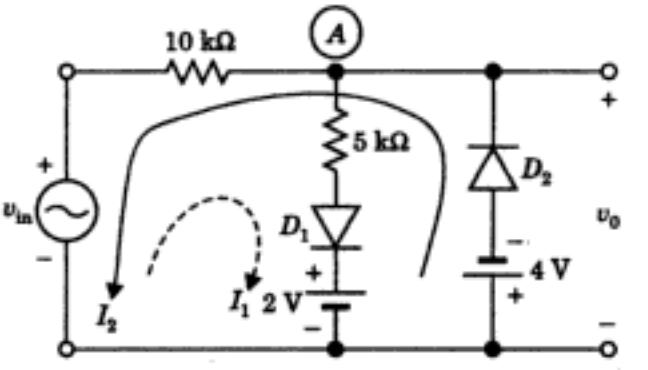


Fig. 3.84 The given circuit for P3.10.

$$I_1 = \frac{(v_{in} - 2)}{(10 + 5)}$$

$$= \frac{1}{15}(v_{in} - 2) \quad \therefore \quad v_{in} > 2 \text{ V for } I_1 \text{ to be +ve}$$

Here $v_0 = 2 + 5 \times I_1$

$$= 2 + 5 \times \frac{1}{15}(v_{in} - 2) = \frac{1}{3}v_{in} + \frac{4}{3}$$

At $v_{in} = 2$, $v_0 = 2$ V, At $v_{in} = +6$ V, $v_0 = 10/3$ V, shown as curve CD, on Fig. 3.85.

D_1 OFF, D_2 ON

Here current I_2 flows and must be +ve

$$I_2 = -\frac{v_{in} + 4}{10} \quad \therefore \quad v_{in} < -4 \quad \text{for } I_2 \text{ to be +ve and } D_2 \text{ to be ON}$$

Here $v_0 = -4$ V, see curve AB in Fig. 3.85.

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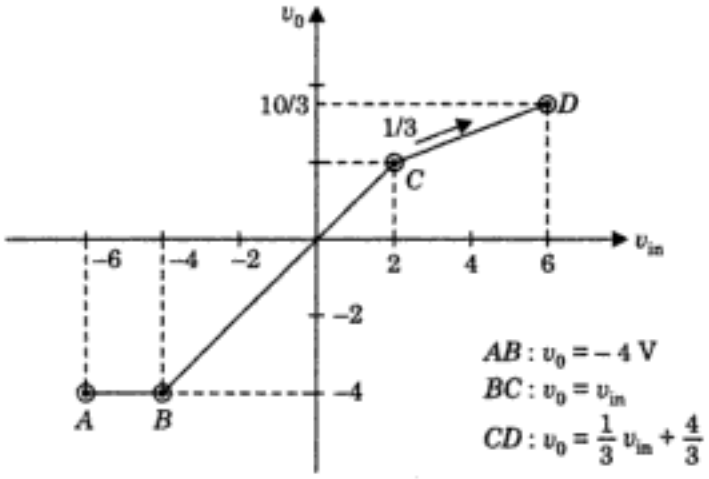


Fig. 3.85 Characteritic (transfer) curve, P3.10.

D_1 OFF, D_2 OFF

In the range $-4 < v_{in} < 2$, at least one diode is ON. Outside this voltage range of v_{in}, D_1 and D_2 are both OFF, and then $v_0 = v_{in}$, see curve *BC* in Fig. 3.85.

P3.11 (a) The input voltage v_{in} to the two-level clipper shown in part of the figure varies linearly from 0 to 150 V. Sketch the output voltage v_0 to the same time scale as the input voltage. Assume ideal diodes.

(b) Repeat (a) for the circuit shown in (b).

Hint.

(a) Let v_{in} be such that D_1 and D_2 conduct. Then to find v_{in} we must have I_1 and I_2 +ve. If D_1 and D_2 both conduct then

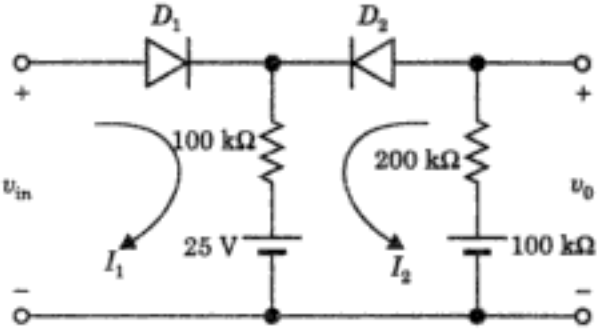


Fig. 3.86(a) Given circuit, P3.11 part (a).

D_1 and D_2 both ON

$$v_{in} - 25 = (100) \times (I_1 + I_2) \qquad (\because D_1 \text{ conducts}) \qquad \text{(i)}$$

and $$(100 - 25) = 200I_2 + 100(I_1 + I_2) \qquad (\because D_2 \text{ conducts}) \qquad \text{(ii)}$$

From Eq. (ii),

$$300I_2 = 75 - 100I_1$$

$$\therefore \quad 100I_2 = 25 - \frac{100}{3} I_1$$

Putting $100I_2 = 25 - \frac{100}{3} I_1$ in Eq. (i), we get

$$v_{in} - 25 = 100I_1 + \left(25 - \frac{100}{3} I_1\right)$$

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$$\therefore \quad v_{in} - 50 = \frac{200}{3} I_1 \quad \text{or} \quad I_1 = \frac{3}{200}(v_{in} - 50)^*$$

$$\therefore \quad I_2 = \frac{1}{100}\left[25 - \frac{100}{3} \times \frac{3}{200}(v_{in} - 50)\right] = \frac{1}{200}(100 - v_{in})^*$$

So that I_1 is +ve, v_{in} must exceed 50 V to make D_1 conduct. Hence for $v_{in} < 50$,

D_1 is OFF, D_2 ON

D_1 OFF and D_2 ON

$$I_1 = 0, \; I_2 = \frac{(100 - 25)}{300} = \frac{1}{4} \text{ mA}$$

$$v_0 = 100 \text{ V} - 200 \times \frac{1}{4} = 100 - 50 = 50 \text{ V}$$

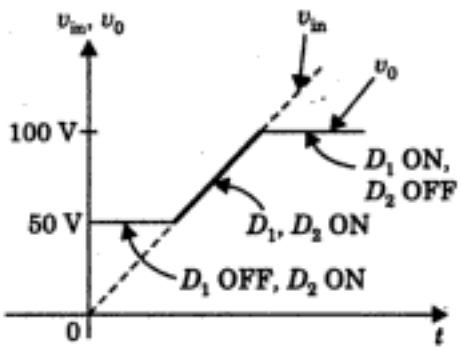


Fig. 3.86(b) v_{in} and v_o for P3.11(a).

For $^*50 < v_i < 100$, D_1 is ON, D_2 ON

$$\therefore \quad v_0 = v_{in}$$

When $v_{in} > 100$ V, D_1 conducts, D_2 OFF

$$\therefore \quad v_0 = 100 \text{ V} \qquad (\because \; I_2 = 0)$$

$\therefore$ v_{in} and v_0 curves are shown in Fig. 3.86(b).

(b) Here we have as follows:

(i) ***When $v_{in} < 25$ V*** $(\therefore \; D_1, D_2 \text{ both OFF})$

$$\therefore \quad v_0 = 25 \text{ V}$$

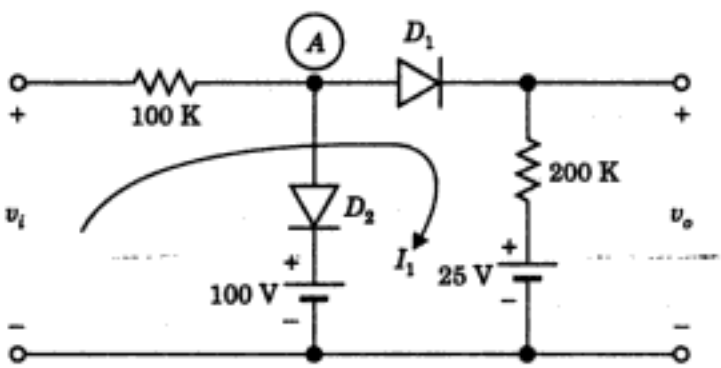


Fig. 3.86(c) The given circuit of clipper, P3.11, part (b).

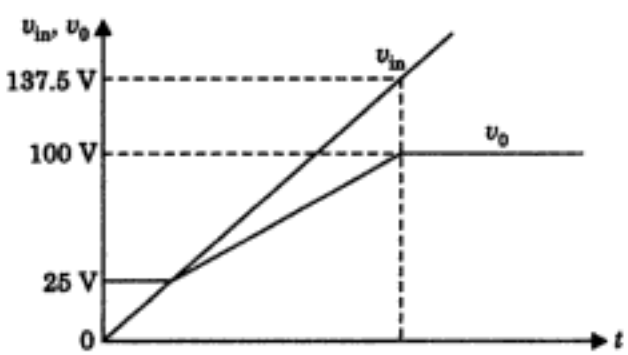


Fig. 3.86(d) v_{in} and v_o for P3.11(b).

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(ii) ***When v_i > 25 V***

$\therefore$ *D_1 ON, D_2 is OFF* provided $V_A < 100$ V (case b)

When D_1 is ON, and D_2 OFF, then $v_A = v_o$ (case b)

say, *D_1 is ON and D_2 OFF*, therefore

$$I_1 = \frac{v_i - 25}{100 + 200} = \frac{(v_i - 25)}{300} \text{ mA}$$

$$v_o = 25 + I_1 \times 200 = 25 + \left[\frac{(v_i - 25)}{300}\right] \times 200$$

$$= 25 + (v_i - 25) \times \frac{2}{3}$$

$$= \frac{25}{3} + \frac{2}{3} v_i$$

As $v_A = v_o$, as soon as v_A (= v_o) reaches 100 V, then D_2 can conduct.

$\therefore$ For case (ii), v_i can vary till $\frac{25}{3} + \frac{2}{3} \times v_i = 100$ V is true

i.e., till $v_{in} = \frac{1}{2}(300 - 25) = \frac{275}{2} = 137.5$ V

then $v_o = 100$ V

(iii) ***When v_i > 137.5 V***, (then *D_1 is ON, D_2 is ON*)

$\therefore$ $v_o = 100$ V only

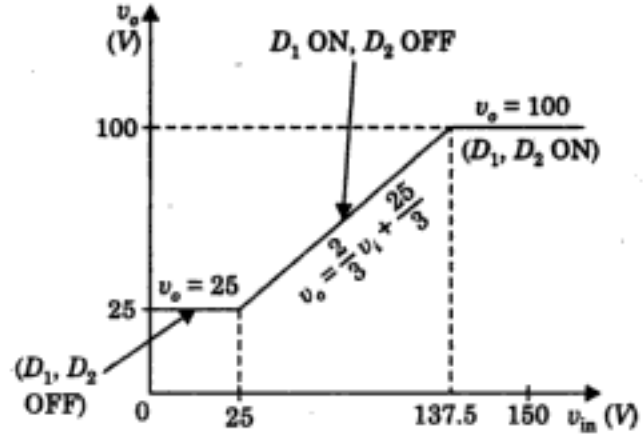


Fig. 3.86(e) v_{in} versus v_o for P3.11(b).

P3.12 (a) Obtain the voltage transfer characteristic of the circuit shown, assuming that the diodes are ideal.

(b) Sketch one cycle of the output voltage, assuming that the input voltage is $v_i(t) = 20 \sin \omega t$.

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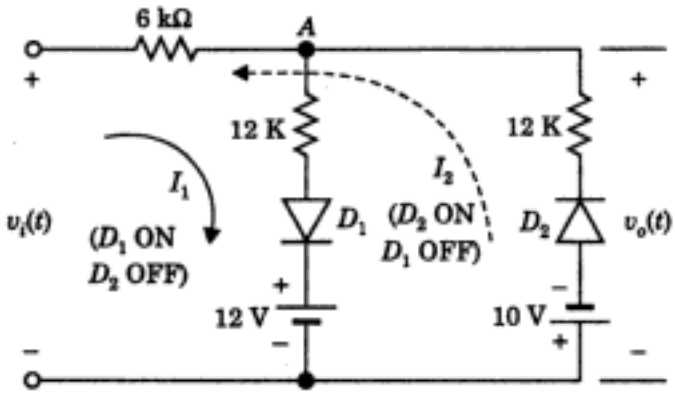


Fig. 3.87(a) Given circuit for P3.12.

Solution (a) ***Let D_1 be ON and D_2 OFF***

Then current I_1 flows and I_1 must be +ve

$$I_1 = \frac{(v_i - 12)}{(6+12)} = -\frac{2}{3} + \frac{v_i}{18}$$

$$I_1 \text{ is +ve for } \frac{v_i}{18} \geq \frac{2}{3} \quad \text{i.e.,} \quad v_i \geq 12 \text{ V}$$

Then $$v_0(t) = 12 + 12I_1 = 12 + 12\left(-\frac{2}{3} + \frac{v_i}{18}\right) = 4 + \frac{2}{3}v_i$$

For $v_i = 20$ V, $v_0 = 17\frac{1}{3}$, for $v_i = 12$ V, $V_0 = 12$ V (see curve CD in Fig. 3.87(b))

(b) ***Now let D_1 be OFF, D_2 ON***, then current I_2 (dash) flows. I_2 must be +ve

$$I_2 = -\frac{(v_i + 10)}{(6+12)} = -\frac{5}{9} - \frac{v_i}{18} = -\frac{1}{18}(10 + v_i)$$

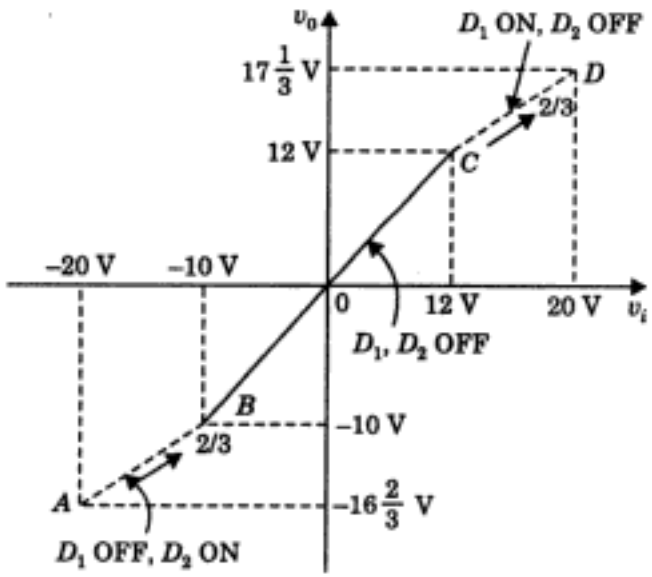


Fig. 3.87(b) Voltage transfer characteristic (v_i versus v_o).

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I_2 is +ve iff $v_i \le -10$ V

$$V_0 = -10 - 12I_2 = -10 - 12\left(\frac{-5}{9} - \frac{v_i}{18}\right) = -\frac{10}{3} + \frac{2}{3}v_i$$

$$V_0\big|_{v_i = -10\text{V}} = -\frac{10}{3} + \frac{2}{3}(-10) = -10\text{V}$$

$$V_0\big|_{v_i = -20\text{V}} = -\frac{10}{3} - \frac{40}{3} = -16\frac{2}{3}\text{ V}$$

To draw voltage transfer characteristic, we have

$$v_0 = \begin{cases} 4 + \frac{2}{3}v_i, & v_i \ge 12\text{ V} \quad (\text{D}_1\ ON, D_2\ OFF) & \text{see } CD \text{ part in Fig. 3.87(b)} \\ v_i, & -10 \le v_i \le 12 \quad (D_1\ OFF, D_2\ OFF) & \text{see } BC \text{ part in Fig. 3.87(b)} \\ -\frac{10}{3} + \frac{2}{3}v_i, & v_i \le -10\text{V} \quad (D_1\ OFF, D_2\ ON) & \text{see } AB \text{ part in Fig. 3.87(b)} \end{cases}$$

The transfer characteristic is as shown in Fig. 3.87(b)

(b) ***For $-10V \le V_i \le 12$, $V_0 = V_i$***

As $V_i = 20 \sin\theta$ V

for $V_i = -10$ V, $\theta = \sin^{-1}\dfrac{-10}{20} = 210° = 1.66\pi$ rads

for $V_i = 12$ V, $\theta = \sin^{-1}\dfrac{12}{20} = 53.13° = 0.295\pi$ rads

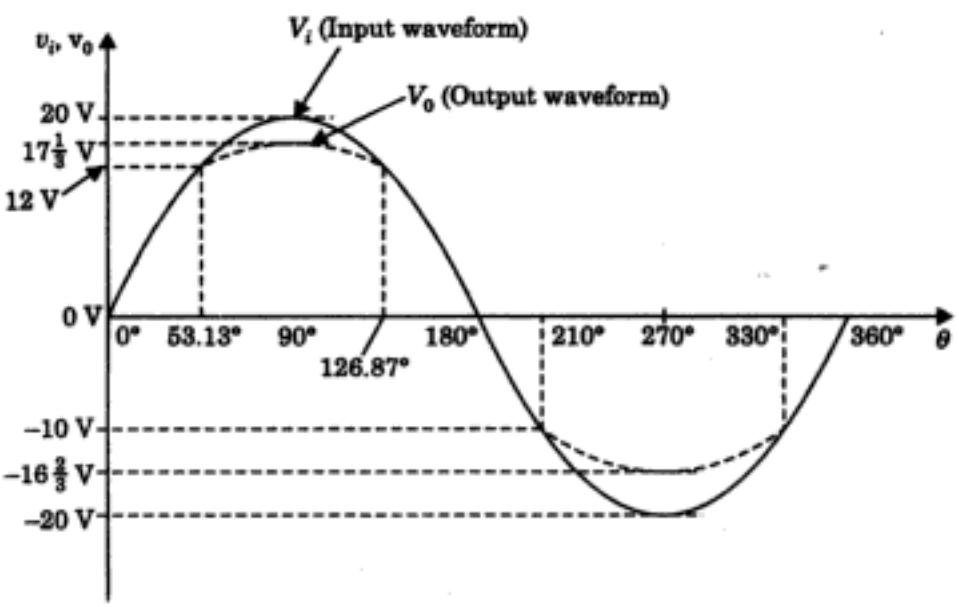


Fig. 3.87(c) Sketch of one cycle of v_0, P3.12(b).

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P3.13 Obtain the voltage transfer characteristic (v_{in} versus v_0) and also find the output voltage $v_0(t)$ for the circuit shown in Fig. Assume ideal diodes.

[**Ans.** $v_0(t) = \frac{2}{3}v_{in} - 5$ for $v_{in}(t) < -15$

$v_0(t) = 4 + \frac{2}{3}v_{in}$ for $v_{in}(t) > 12$

$v_0(t) = v_{in}(t)$ for $-15 \le v_{in}(t) < 12$]

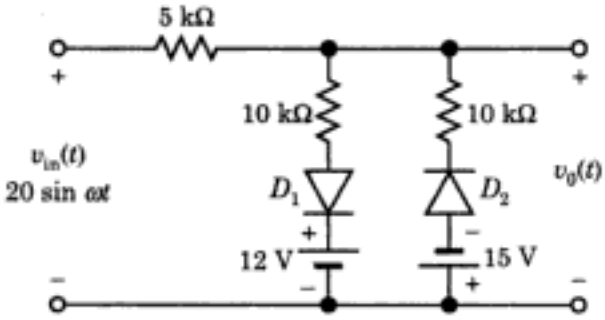


Fig. 3.88(a) The given circuit of P3.13.

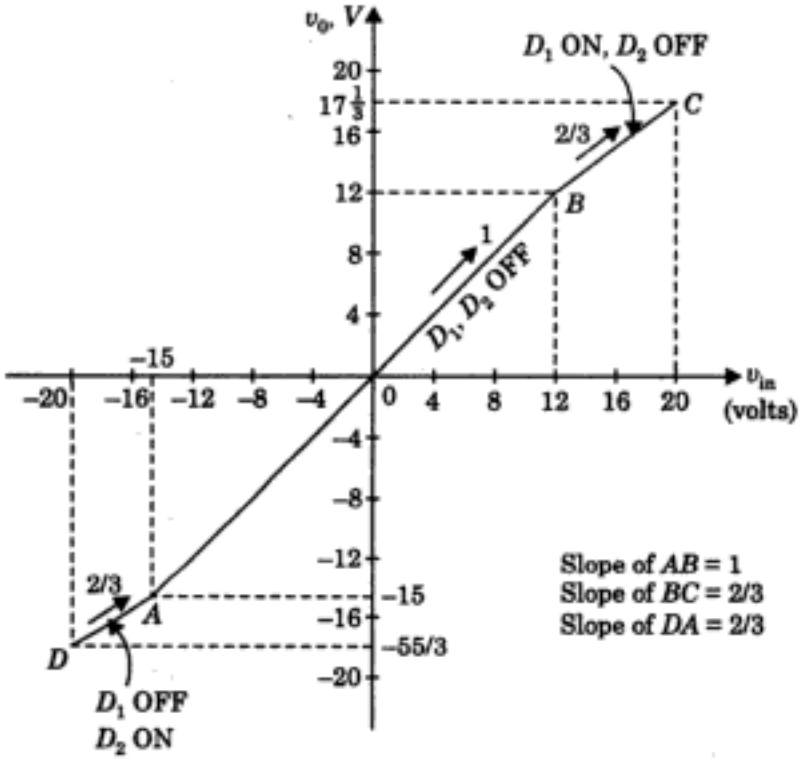


Fig. 3.88(b) The transfer function: $v_{in}(t)$ versus $v_0(t)$.

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CHAPTER 4

Bipolar Junction Transistors (BJTs)

4.1 INTRODUCTION

The development of Electronics and Computer Industry as we see today goes to the invention of the three terminal solid state device called **transistor**. There are two important types of transistors available: Bipolar Junction Transistor (BJT) and Field-Effect Transistor (FET). The important feature of a transistor whether BJT or an FET is that the current through the two terminals can be controlled by a small change in voltage or current applied at the third terminal. Because of this, we can amplify small AC signals (voltage or current) or switch the device from ON state in OFF state and vice versa. The amplifying action of a transistor is commonly used in audio/video amplifiers and the switching mode of operation finds wide applications in high speed digital electronics.

In this chapter, we will discuss the physical principles of operation of the bipolar junction transistor (BJT), its volt-ampere characteristics for different configurations (CB, CE and CC), DC equivalent circuit and Ebers-Moll representation of transistor for large signals. The analysis of transistor circuits under DC conditions has been discussed through a number of solved examples. Field-effect transistor (FET), the second important three terminal device, and which has many advantages over BJT, will be discussed in chapter 7.

4.2 PHYSICAL STRUCTURE OF BJT

The first three terminal solid state device was fabricated at Bell laboratories by a team of Scientists: William Shockley, John Bardeen and Walter H. Brattain on December 23, 1947. The original transistor was a point contact transistor and has gone through many stages of development. It has three layers and is available as pnp and npn transistor as shown in Fig. 4.1(a) and (b) respectively. The three different layers or sections as shown in Fig. 4.1 are identified as the Emitter, Base and Collector regions. In this figure, the thickness of emitter and collector regions has been shown equal, however, in the practical transistors, the emitter area is considerably smaller than the collector area.

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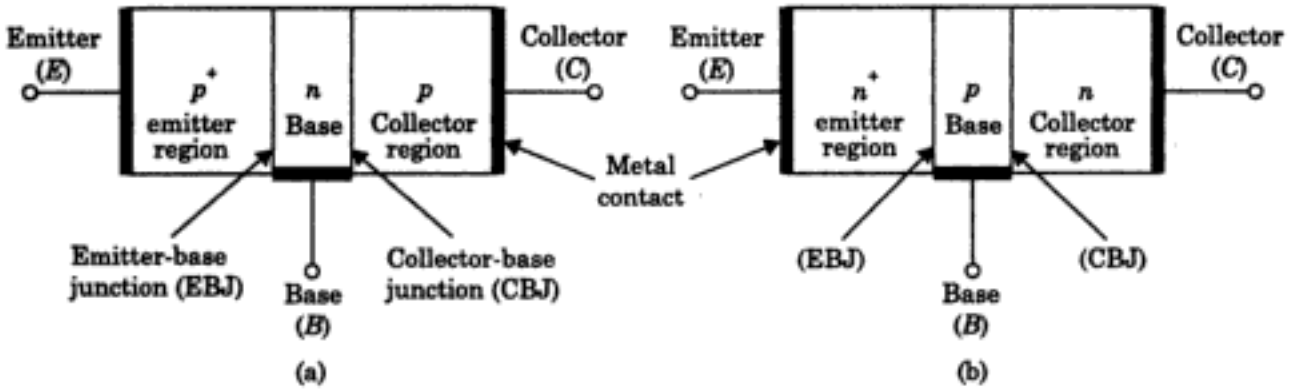


Fig. 4.1 The physical details of (a) a pnp transistor (b) a npn transistor.

The emitter region is heavily doped and, therefore, has been shown as p^+ in the pnp transistor and n^+ in the npn transistor. A high density doping has been used for emitter region so that it is capable of emitting/injecting large number of holes (for pnp) and electrons (for npn) through the base into the collector when emitter-base junction is forward biased. If the collector-base junction is reverse biased, it can be seen that collector will collect the carriers (i.e. holes or electrons) emitted by the emitter region. The surface area of the collector is usually more than that of the emitter so that the collector can handle more power. However, the doping level of the collector need not be high as it is not required to provide many carriers. The base region is a lightly doped, thin layer designed to provide electrical isolation between the emitter and the collector. The base region also provides a contact point needed for the control of emitter-base voltage.

4.3 MODES OF OPERATION

A BJT consists of two p-n junctions: the emitter base junction (EBJ) and collector base junction (CBJ). They are constructed in a special way and connected in series back to back. Each of these junctions can be forward biased or reverse biased. Depending upon the bias conditions of each of these junctions, we can use a BJT in four different modes of operation as shown in Table 4.1.

Table 4.1 Modes of Operation of a BJT

Mode	*Emitter-base junction*	*Collector-base junction*	*Use*
Forward-active	Forward biased	Reverse biased	Normal amplifier (mostly used)
Cut-off	Reverse biased	Reverse biased	Open switch
Saturation	Forward biased	Forward biased	Closed switch
Reverse-active	Reverse biased	Forward biased	Low gain amplifier (rarely used)

Whenever a transistor is to be used as an amplifier, it is biased in the forward active or simply active mode of operation. In switching applications (e.g. logic circuits) a transistor is operated in cut-off and saturation modes.

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4.4 OPERATION OF *pnp* TRANSISTOR IN ACTIVE MODE

It is easy to understand the concept of operation of a bipolar junction transistor in a pnp transistor. Therefore, consider a pnp transistor shown in Fig. 4.2 biased in the forward active mode, that is, emitter-based junction is forward biased (V_{EB} is +ive) and collector-base junction is reverse biased (V_{CB} is –ive). Due to the externally applied voltages V_{EB} and V_{CB}, currents flow in the transistor. The various current components that flow in the transistor are shown in Fig. 4.2. In this discussion, we are assuming that the externally applied voltages V_{EB} and V_{CB} appear across the depletion region of each junction (not shown) and thus the potential is constant within each region. This means that the drift current due to thermally generated carriers has been neglected which in any case is usually very small. Thus, all the current components as shown in Fig. 4.2 are due to diffusion currents.

The emitter current I_E has two components:

1. Hole injected current, I_{pE} due to holes injected from emitter into base.
2. Electron injected current, I_{nE} due to the electrons injected from base into emitter region.

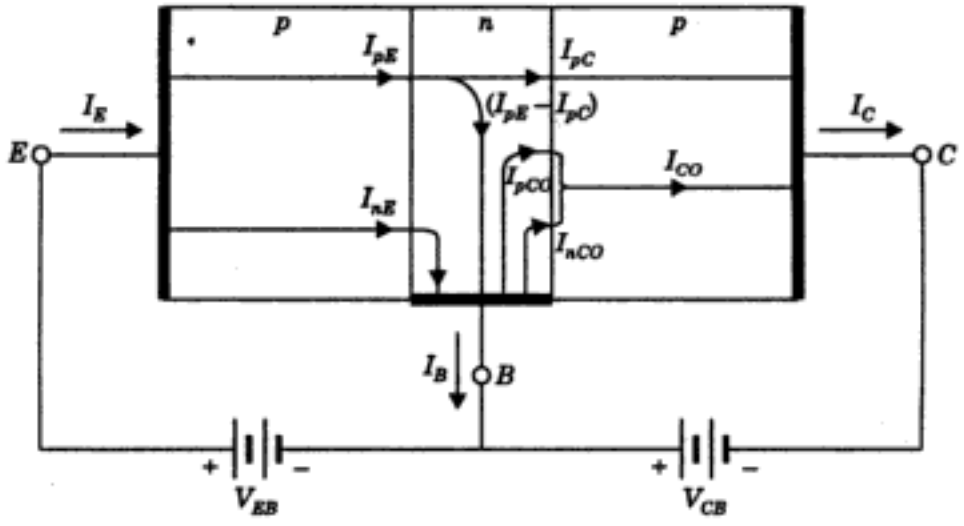


Fig. 4.2 Current components for a pnp transistor biased in the forward active mode (i.e. emitter-base junction (EBJ) forward biased and collector base junction (CBJ) reverse biased).

It may be noted that the electrons crossing from base to emitter constitute a current in the same direction as I_{pE}.

As already stated, emitter region is heavily doped compared to the base region, therefore, the hole current I_{pE} is always much larger compared to electron current I_{nE}. This is in fact a desirable situation as the electrons crossing from base to emitter region never reach the collector and, therefore, do not contribute towards the collector current. The total emitter current I_E is therefore, given by

$$I_E = I_{pE} + I_{nE} \tag{4.1}$$

Now, let us see what happens to the holes injected from the emitter into the base. The base region has excess electrons as it is of *n*-type, therefore, some of the injected holes recombine with the excess electrons available in the base region and get lost. However, as the base region is very thin and has very low doping level, only a few of the injected holes

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of I_{pE} are lost due to the recombination. Thus, most of the injected holes in the curent I_{pE} reach the collector (or are collected by the collector) as the collector base junction is reverse biased. The collector current due to these collected holes has been shown as I_{pC} in Fig. 4.2. The current I_{pC} will be less than I_{pE} and the current $(I_{pE} - I_{pC})$ represents the loss of current due to recombination. It is seen that the electrons also enter into the base region from the external circuit to replenish those lost due to recombination in the base region. These electrons constitute the base current I_B and is positive outwards as shown in Fig. 4.2.

The collector current I_C has one more component besides I_{pC}. As collector base junction is reverse biased, a second component of collector current I_C exists due to reverse saturation collector current I_{CO}. The thermally generated holes (minority carriers) in the base region cross into the collector region and constitute a current component I_{pCO}. Similarly, thermally generated electrons from collector cross into the base region causing current I_{nCO}. The total reverse saturation current I_{CO} as shown in Fig. 4.2 is given by

$$I_{CO} = I_{pCO} + I_{nCO} \tag{4.2}$$

Now, we can write an expression for the total collector current I_C as:

$$I_C = I_{pC} + I_{CO} \tag{4.3}$$

and has the direction such that I_C is going outwards from the collector lead. Thus, for a pnp transistor emitter current is positive entering into the emitter terminal, whereas the base current I_B and collector current I_C are positive when leaving the base and collector terminals respectively.

We define a parameter α (alpha) such that

$$I_{pC} = \alpha I_E \tag{4.4}$$

Note that I_{pC} is always less than I_E i.e. α has a value less than unity. The typical values of α lie in the range of 0.90 to 0.995. Thus, α represents the fraction by which the total emitter current I_E gets reduced before becoming the collector current I_{pC}.

Equation (4.3) may now be written as

$$I_C = \alpha I_E + I_{CO} \tag{4.5}$$

or

$$\alpha = \frac{I_C - I_{CO}}{I_E} \tag{4.6}$$

The parameter α is also called the **large signal current gain** of a transistor connected in common base configuration. It is the ratio of increment in I_C from cut-off to increment in I_E from $I_E = 0$.

It may be pointed out that α is not constant and it varies with the emitter current I_E, the collector-base voltage V_{CB}, the temperature T, besides the type of transistor (npn or pnp). It is also emphasized that Eq. (4.5) is valid only for the transistor biased in the forward-active mode of operation, that is, for emitter-base junction forward biased and collector-base junction reverse biased. In forward active mode α is usually replaced by α_F signifying that it is the forward mode current gain and Eq. (4.5) can be written as

$$I_C = \alpha_F I_E + I_{CO} \tag{4.7}$$

Similarly, if a transistor is used in the reverse-active mode, i.e., collector-base junction is forward biased and emitter-base junction is reverse biased, then Eq. (4.5) is given by

$$I_E = \alpha_R I_C + I_{EO} \tag{4.8}$$

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where α_R represents the reverse mode current gain. The value of α_R is very small compared to α_F due to the difference in doping levels of emitter region and collector region. A transistor is rarely used in reverse active mode as it can not provide gain in this mode.

Now, consider the case when both the junctions are forward biased, that is, transistor is biased in saturation mode. Since collector base junction (CBJ) is forward biased, I_{CO} in Eq. (4.7) must be replaced by the diode current which enters the collector terminal in Fig. 4.2 for V_{CB} positive. That is, the collector current I_C is given by

$$I_C = \alpha_F I_E - I_{CO}(e^{V_{CB}/\eta V_T} - 1) \tag{4.9}$$

It can be seen that if V_{CB} is negative and much greater than V_T, Eq. (4.9) reduces to

$$I_C = \alpha_F I_E + I_{CO}$$

which is same as Eq. (4.7) (as expected).

A similar analysis can be carried out for various current components for a npn transistor biased in the forward active mode. Figure 4.3 shows the biasing of an npn transistor in forward active mode and the various current components due to this.

It can be seen from Fig. 4.3 that for an npn transistor, emitter current I_E is positive when leaving the emitter terminal and currents I_C and I_B are positive when entering the collector and base terminals, respectively. The collector current I_C from Fig. 4.3 is given by

$$\begin{aligned} I_C &= I_{nC} + I_{CO} \\ &= \alpha_F I_E + I_{CO} \end{aligned} \tag{4.10}$$

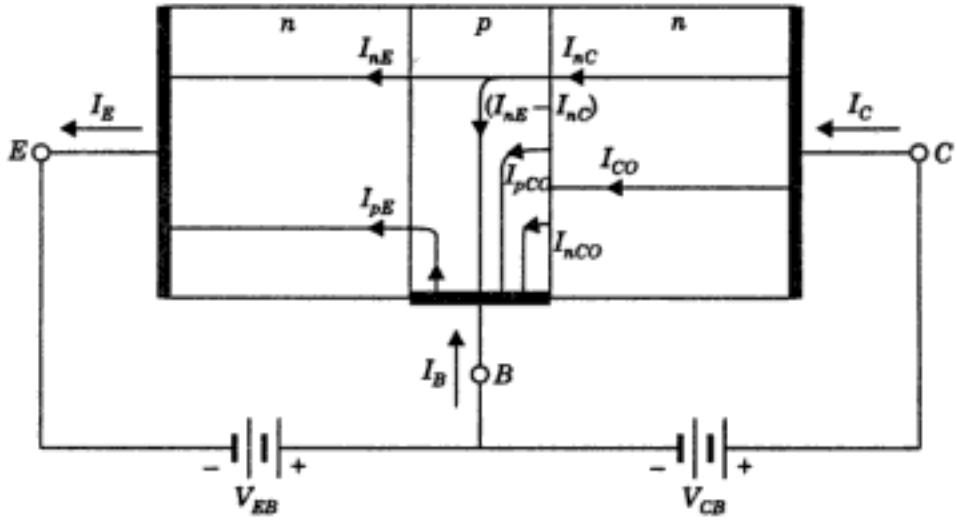


Fig. 4.3 Current components for an npn transistor biased in the forward active mode (i.e. EBJ forward biased and CBJ reverse biased).

4.5 THE EBERS-MOLL MODEL OF A BJT

We studied the physical behaviour of a transistor in the forward active mode of operation. Now, we discuss the quantitative analysis by replacing it with a large signal general model known as the **Ebers-Moll model**. This is a generalized model and can be used to describe the BJT in any of its four possible modes of operation. This model is derived by considering

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that a transistor is made from two p-n junction diodes connected back to back. In practice, however, it is not possible to make a transistor by connecting two p-n junction diodes back to back (Explain why?). The model consists of two diodes and two controlled current sources as shown in Fig. 4.4 for the case of a pnp transistor. In this model, we have replaced the emitter-base junction by a diode producing diode current I_{DE}. Similarly, the junction CBJ has been replaced by a diode, producing diode current I_{DC}.

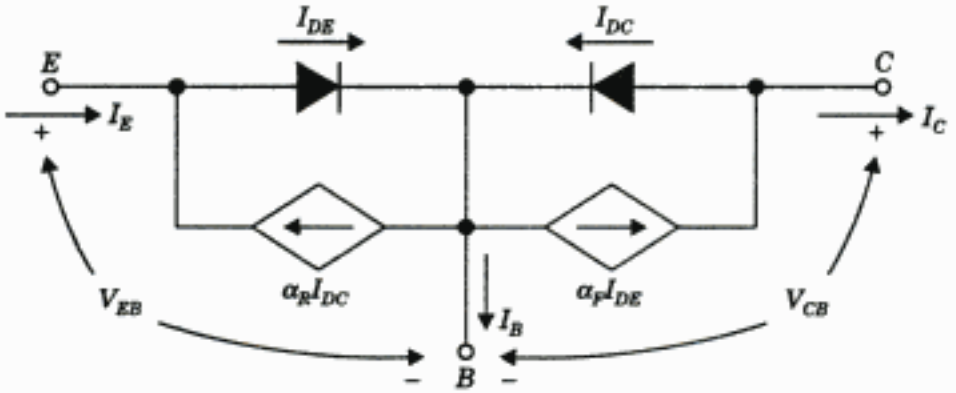


Fig. 4.4 The Ebers-Moll model of a pnp transistor.

The diode currents I_{DE} and I_{DC} are given by the diode equations:

$$I_{DE} = I_{SE}(e^{V_{EB}/V_T} - 1) \tag{4.11}$$

$$I_{DC} = I_{SC}(e^{V_{CB}/V_T} - 1) \tag{4.12}$$

where I_{SE} and I_{SC} are the reverse saturation currents for the two diodes. I_{SC} is usually large compared to I_{SE} as the area of the collector-base junction is much larger than that of emitter base junction (by a factor of 2 to 50).

As seen earlier, the emitter-base junction diode current I_{DE} reaches the collector as $\alpha_F I_{DE}$, where α_F denotes the forward current gain. Similarly, the collector-base junction diode current I_{DC} is transported across the base region and reaches emitter as $\alpha_R I_{DC}$, where α_R denotes the reverse α of a transistor. The value of α_F is close to unity whereas α_R is very small and lies in the range of 0.02 to 0.5 due to the unsymmetrical construction of the transistor.

From **Fig. 4.4**, we may write the terminal currents I_E and I_C as:

$$I_E = I_{DE} - \alpha_R I_{DC} \tag{4.13}$$

$$I_C = \alpha_F I_{DE} - I_{DC} \tag{4.14}$$

Substituting the values of I_{DE} and I_{DC} from Eqs. (4.11) and (4.12) in Eqs. (4.13) and (4.14), we can express terminal currents I_E and I_C in terms of junction voltages V_{EB} and V_{CB}.

$$I_E = I_{SE}(e^{V_{EB}/V_T} - 1) - \alpha_R I_{SC}(e^{V_{CB}/V_T} - 1) \tag{4.15}$$

$$I_C = \alpha_F I_{SE}(e^{V_{EB}/V_T} - 1) - I_{SC}(e^{V_{CB}/V_T} - 1) \tag{4.16}$$

Equations (4.15) and (4.16) are called the **Ebers-Moll (EM) equations**. The four parameters of the EM-model I_{SE}, I_{SC}, α_F and α_R are found to be related as:

$$\alpha_F I_{SE} = \alpha_R I_{SC} \tag{4.17}$$

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This equation is known as the reciprocity condition for the BJT. We can now obtain a relationship between I_E and I_C by putting the value of $I_{SC}(e^{V_{CB}/V_T} - 1)$ from Eq. (4.16) into Eq. (4.15), and simplifying, we get

$$I_E = I_{SE}(e^{V_{EB}/V_T} - 1) - \alpha_R\left[\alpha_F I_{SE}(e^{V_{EB}/V_T} - 1) - I_C\right] \tag{4.18}$$

$$= \alpha_R I_C + (1 - \alpha_R\alpha_F) I_{SE}(e^{V_{EB}/V_T} - 1)$$

$$= \alpha_R I_C + I_{EO}(e^{V_{EB}/V_T} - 1) \tag{4.19}$$

where $$I_{EO} = (1 - \alpha_F\alpha_R) I_{SE} \tag{4.20}$$

and is called the reverse saturation emitter current.

Similarly, we can obtain a relationship

$$I_C = \alpha_F I_E - I_{CO}(e^{V_{CB}/V_T} - 1) \tag{4.21}$$

where $$I_{CO} = (1 - \alpha_F\alpha_R) I_{SC} \tag{4.22}$$

As an application of the EM model, consider a pnp transistor biased in the forward active mode. In active mode, V_{CB} is negative for a pnp transistor and its magnitude is usually much greater than V_T, so Eq. (4.21) can be approximated as:

$$I_C = \alpha_F I_E + I_{CO}$$

which is the standard equation for a transistor biased in the forward active region.

4.6 CIRCUIT SYMBOLS FOR BJTs

The physical structure used so far is good for understanding the transistor operation. However, for circuit analysis, convenient circuit symbols are used as shown in Fig. 4.5.

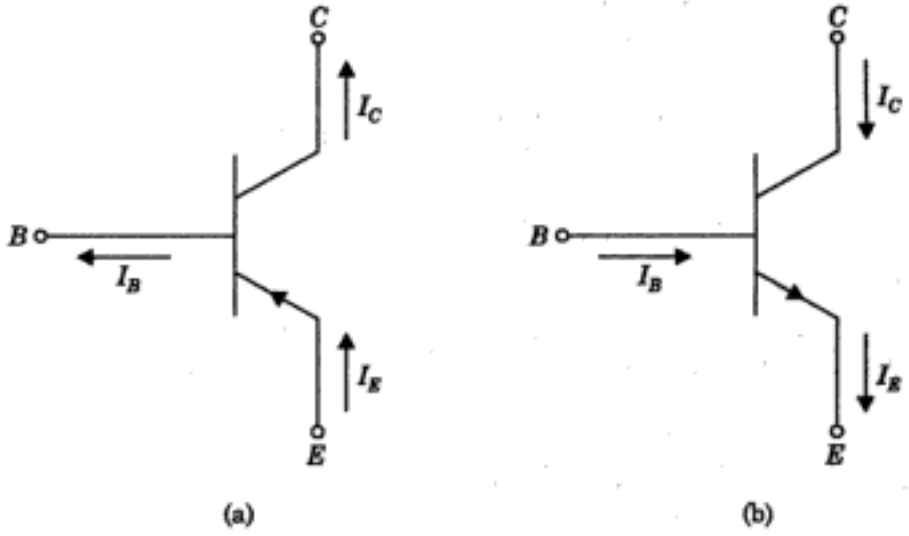


Fig. 4.5 Circuit symbol for (a) pnp transistor (b) npn transistor.

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Note that there is an arrowhead in the emitter electrode. We know that emitter and collector regions of a transistor are of the same type (both are p for pnp transistor and both are n for npn transistor). However, the area and the doping levels of these regions are different. If emitter and collector regions are interchanged, the value of α will be much lower, a value called **reverse** $\alpha(\alpha_R)$. It is, therefore, necessary to specify the emitter region for proper use of the device. The arrowheads in these circuit symbols also indicate the direction of current flow in the emitter when the emitter-base junction is forward biased. All the currents shown in Fig. 4.5 give the actual direction of the currents flowing in the transistor. In both the cases, it can be seen that by KCL

$$I_E = I_B + I_C \tag{4.23}$$

Using the circuit symbols, the biasing of pnp and npn transistors in the active mode can now be shown as in Fig. 4.6(a) and (b) respectively.

The voltage between each pair of terminals is also indicated in Fig. 4.6. Here, V_{EB} represents the voltage drop from emitter to base. It also means that the voltage at the emitter is determined with reference to the voltage at base. For pnp transistor V_{EB} is positive and it is negative for npn transistor. Similarly, V_{CB} is negative for pnp transistor and positive for npn transistor. Clearly, $V_{EB} = V_E - V_B$ and $V_{CB} = V_C - V_B$.

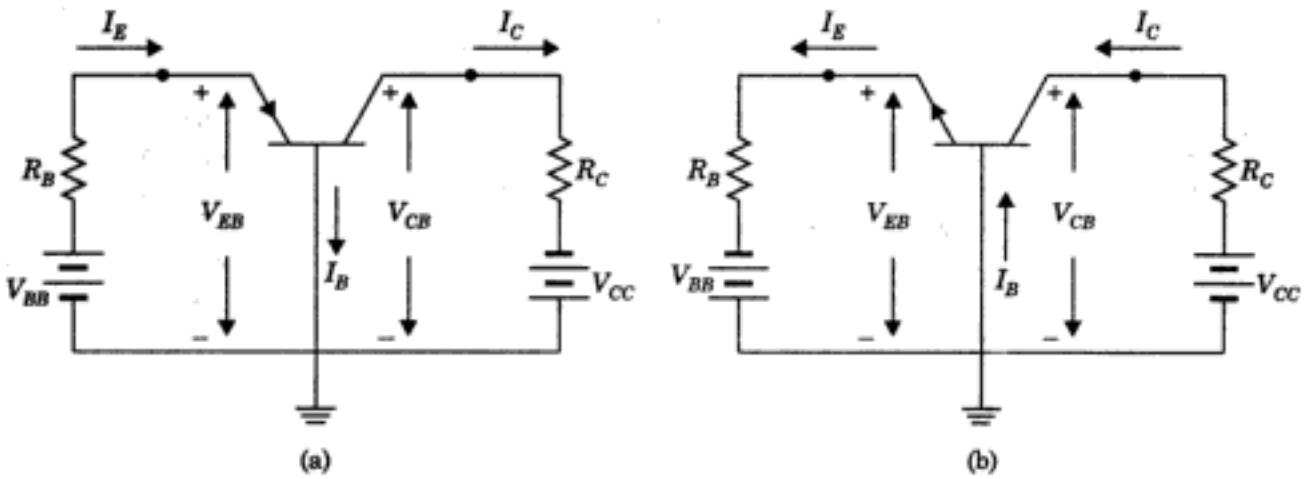


Fig. 4.6 Transistor biasing in forward active region for common base configuration (a) for pnp transistor, (b) for npn transistor.

4.7 VOLT-AMPERE CHARACTERISTICS OF A BJT

Knowing the physical behaviour of a transistor, we can now graphically display its volt-ampere characteristics. There are two sets of volt-ampere characteristics which completely describe the behaviour of a transistor (i) the input characteristics, (ii) the output characteristics. A transistor can be used in any of the three configurations, i.e. common base (CB), common emitter (CE) and common collector (CC) depending upon which terminal is kept common between input and output circuit. We will discuss the volt-ampere characteristics of the transistor for all the three configurations. The special properties of the transistor in configuration CB, CE and CC will be explained in detail in the chapter on amplifiers.

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4.7.1 The Common Base (CB) Configuration

Output characteristics: The output characteristics of a pnp transistor used in CB configuration are shown in Fig. 4.7. As can be seen, output characteristics is a family of curves drawn between the output voltage V_{CB} and output collector current I_C for various values of input emitter current I_E.

There are three important regions of operation marked in Fig. 4.7. These are: active region, saturation region and cut-off region. The volt-ampere characteristics in each of these regions will be explained now.

Active region: In the active region, emitter-base junction is forward biased and the collector base junction is reverse biased. The collector-base voltage, V_{CB} therefore, is shown negative in Fig. 4.7. The relationship

$$I_C = \alpha_F I_E + I_{CO} \tag{4.24}$$

holds good in the active region. For $I_E = 0$, I_C is equal to reverse saturation current I_{CO}. This current is very small (in order of μA) and, therefore, the characteristic curve almost overlaps the horizontal axis as shown in Fig 4.7.

As I_E is increased, the collector current I_C increases as given by Eq. (4.24). The value of I_{CO} is usually so small that it can be neglected and Eq. (4.24) is approximated as

$$I_C \simeq \alpha_F I_E \tag{4.25}$$

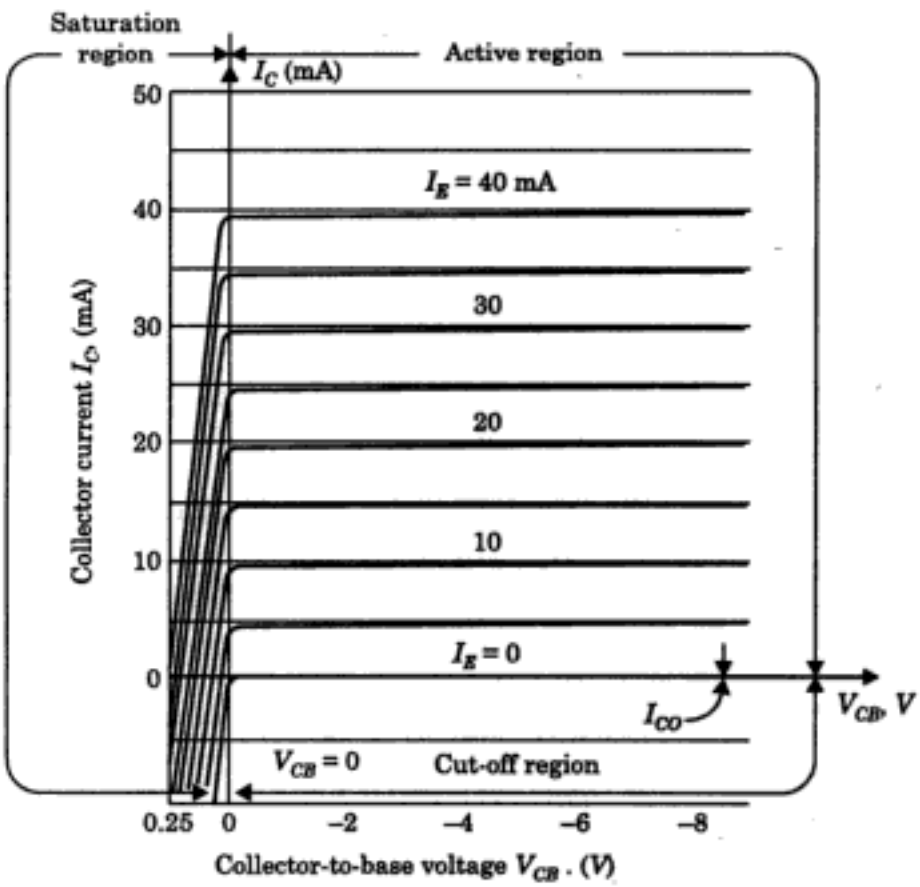


Fig. 4.7 Typical output characteristics of a pnp transistor in CB configuration. The cut-off, active and saturation regions have been indicated.

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We note the following from Eq. (4.25):

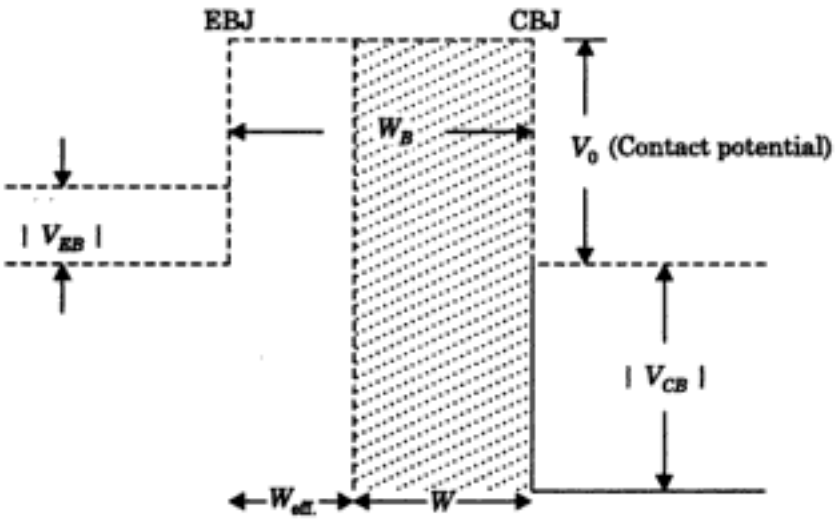
(i) I_C is less than I_E as α_F is always less than unity.

(ii) The collector current I_C is independent of the output voltage V_{CB}.

Theoretically, therefore, the output characteristics should appear as straight horizontal lines. However, as we observe in Fig. 4.7 the collector current I_C increases as $|V_{CB}|$ increases. This increase in collector current I_C is attributed to a phenomenon called **Early Effect** or **Base-Width Modulation**.

Early Effect

Figure 4.8 shows the potential variation of a pnp transistor biased for the active region of operation. When no external voltages are applied, the contact potential or barrier potential has been shown dashed and is equal to V_0. As emitter base junction is forward biased, the potential barrier reduces on the emitter side by $|V_{EB}|$. This also reduces the depletion width in the emitter region which can be neglected and therefore has not been shown. However, for the collector-base junction which is reverse biased, the potential barrier increases by $|V_{CB}|$ and therefore the depletion region increases or penetrates more into the base region and has been shown W. We know that the base region is very lightly doped compared to the collector region. Therefore, depletion region penetrates more into the base region compared to collector region as $|V_{CB}|$ increases. The effective base width $W_{eff} = W_B - W$, therefore, decreases as $|V_{CB}|$ increases.



W_B = Physical width of the base region, W = Depletion region due to reverse bias $|V_{CB}|$ (W region has ions and not free charge carriers), W_{eff} = Effective base width (containing free charge carriers).

Fig. 4.8 Potential variation in a pnp transistor in active region of operation showing base width modulation.

The variation of effective base width W_{eff} with the collector base voltage $|V_{CB}|$ is called **Base-width modulation** or **Early effect**. This results in the following effects:

(i) There is less chances of recombination in the base region as the effective base width or the physical width of the base region reduces from W_B to $(W_B - W)$. The value of α_F, therefore, increases as $|V_{CB}|$ increases causing an increase in collector current I_C ($I_C = \alpha_F I_E$).

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(ii) The concentration gradient of the injected holes p_n (these are the minority carriers in the base region) also increases due to the reduced base width. Since diffusion current is directly proportional to concentration gradient, emitter current I_E also increases.

(iii) For very large values of V_{CB}, the effective base width W_{eff} may be reduced to zero causing extremely large emitter current. This results in the breakdown of the transistor and is called **punch through** or **reach through**. Note that the depletion region has ions and, therefore is conductive. When $|V_{CB}|$ is very large, the full base width W_B becomes ionic and hence conductive. The voltages V_{EB} and V_{CB} have opposite polarity and, therefore, short circuit via the conductive base when $|V_{CB}|$ is very large. This causes a very high break through current.

Cut-off region. The region below $I_E = 0$ characteristic is referred to as the cut-off region. As both the emitter and collector junctions are reverse biased, almost zero currents flow through the transistor and it is in the OFF state.

Saturation region. The region left to the ordinate $V_{CB} = 0$ and above $I_E = 0$ is called the saturation region. In this region both emitter-base junction and collector-base junction are forward biased. As the collector junction is forward biased, holes flow from the p-type collector towards the n-type base and constitute a current in the direction opposite to the direction of positive collector current. Even for small values of V_{CB} positive, large changes in the collector current takes place, and the characteristic falls towards zero as V_{CB} is made more and more positive. Since collector current increases exponentially, I_C may even become negative for large values of forward bias. A transistor is biased in saturation region when used in switching applications such as logic circuits.

Input characteristics: Figure 4.9 shows the input characteristics of a pnp transistor in CB configuration. The input characteristics are drawn between the emitter-base voltage V_{EB} and input emitter current I_E for fixed values of collector-base voltage V_{CB}. For collector open, the curve is seen to be simply the forward characteristics of a emitter base diode. As V_{CB} is made more and more negative, the input characteristic shift towards left due to Early effect. (i.e. the emitter current increases as V_{CB} is made more negative).

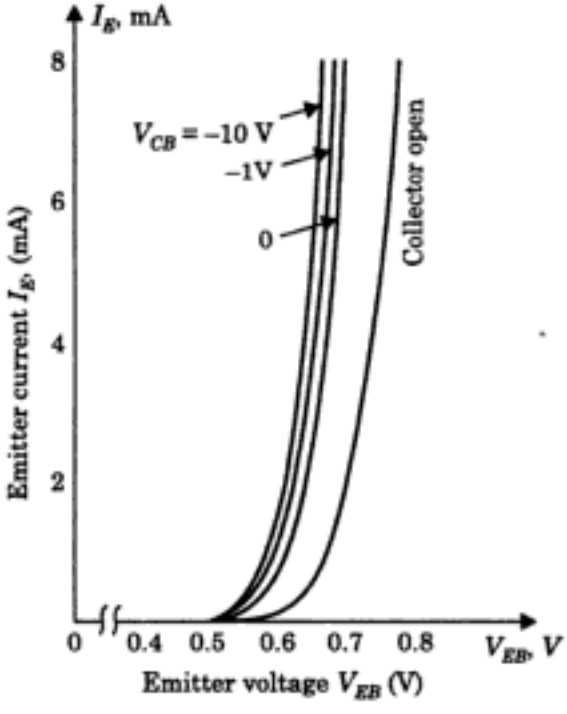


Fig. 4.9 Input characteristics of a pnp transistor in CB configuration.

4.7.2 The Common Emitter (CE) Configuration

Figure 4.10(a) shows an npn transistor biased for CE configuration. Although for understanding the physical behaviour of a transistor, we used a pnp transistor, however, most practical circuits use npn transistor due to its better performance over pnp transistor. The

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output characteristics shown in Fig. 4.10(b) is a plot of the output current I_C vs. output voltage V_{CE} for various values of input base current I_B. Note that base curent, I_B is usually very small of the order of μA for a general purpose transistor.

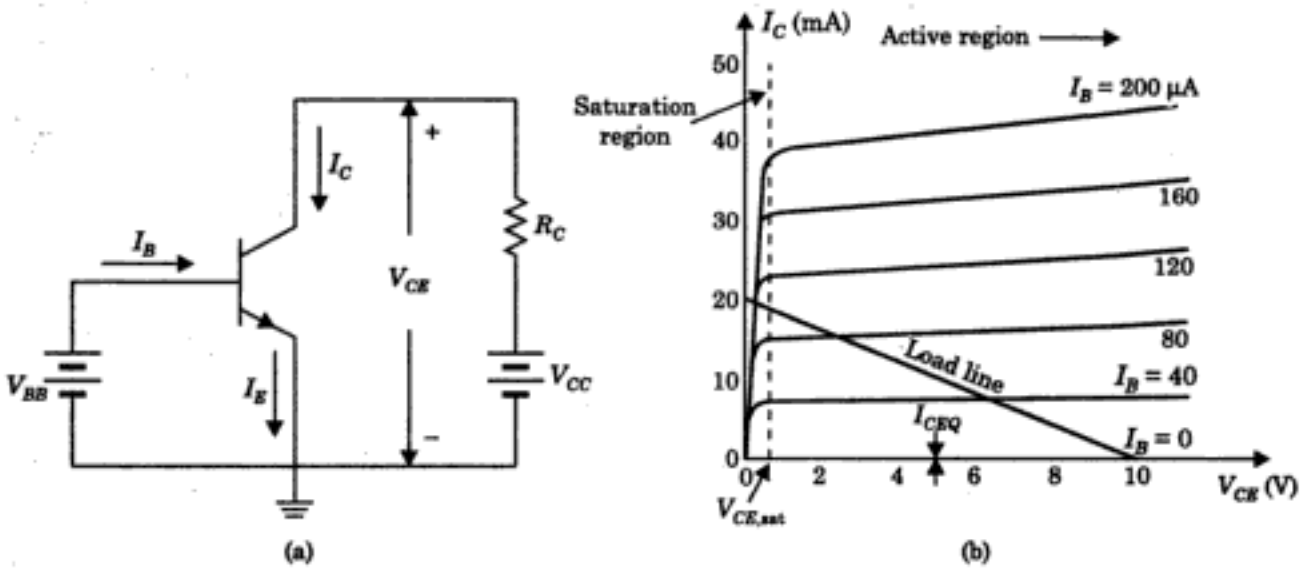


Fig. 4.10 (a) npn transistor biased for CE configuration, (b) Output characteristics with a load line for V_{CC} = 10 V and R_C = 500 Ω.

The output characteristics can be divided into three regions of operation, that is, active, saturation and cut-off as in the case of CB configuration. The region to the right vertical line drawn at $V_{CE} = V_{CE,\,sat}$ (~ 0.2 V) and above the curve for $I_B = 0$ is called the **active region** of operation. In this region the curves for various values of I_B are nearly straight, parallel and equally spaced and therefore, this region is best suited for use as an amplifier. The region left to the vertical line at $V_{CE} = V_{CE,sat}$ is known as the **saturation region**. The cut-off region is not very well defined on the characteristics of a CE transistor.

Active region. In the active region, we know

$$I_C = \alpha_F I_E + I_{CO} \tag{4.26}$$

Also,
$$I_E = I_C + I_B \tag{4.27}$$

Eliminating I_E from Eqs. (4.26) and (4.27), we obtain

$$I_C = \frac{\alpha_F}{1-\alpha_F} I_B + \frac{I_{CO}}{1-\alpha_F} \tag{4.28a}$$

Here, we introduce a parameter β_F, such that

$$\beta_F = \frac{\alpha_F}{1-\alpha_F} \tag{4.28b}$$

Equation (4.28a) now can be rewritten as:

$$I_C = \beta_F I_B + (1+\beta_F) I_{CO} \tag{4.29}$$

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I_{CO} is usually very small compared to I_B, thus we may write

$$I_C \simeq \beta_F I_E \tag{4.30}$$

The parameter $\beta_F (\simeq I_C / I_B)$ is defined as the large signal current gain of a transistor in CE configuration. According to Eq. (4.29a), collector current I_C is independent of the output voltage V_{CE} and the output characteristics should have been straight lines. However, due to Early effect an increase in the current I_C is expected with increase in $|V_{CE}|$. The influence of Early effect is more pronounced in a CE transistor as can be seen from the larger slope of the characteristics compared with *CB* transistor. A simple example will explain the same. Assume that α_F increases from 0.995 to 0.996 (i.e. 0.1%) due to Early Effect as V_{CE} increases from 0 to 10 V. The value of β_F now changes from 0.995/(1 – 0.995) = 200 to 0.996/(1 – 0.996) = 250 which is 25% increase. This example illustrates that a 0.1% increase in the value of α_F is reflected as 25% increase in the value of β_F. This is the reason that the slope of output characteristics for a *CE* transistor is more compared to a *CB* transistor.

There is an important voltage called the **Early voltage** denoted as V_A, which is given in the data sheets of a transistor and helps in finding the output resistance of the transistor. The early voltage V_A is usually determined from the output characteristics of *CE* transistor drawn for various values of emitter-base voltage V_{BE} shown in Fig. 4.11. If the linear portion of the curves are extended backwards on the –ive V_{CE} axis as shown by the dashed lines, we see that all the curves meet at a point $V_{CE} = -V_A$. This voltage V_A is called the **Early voltage** and the typical value lies in the range of 50 to 100 V. The slope of $I_C - V_{CE}$ curves gives the value of inverse of the output resistance of the transistor looking into the collector. The output resistance r_o is, therefore, given by

$$r_0 = \frac{V_A}{I_C} \tag{4.31}$$

where I_C is the value of the collector current at the boundary of the active region for a given V_{BE}.

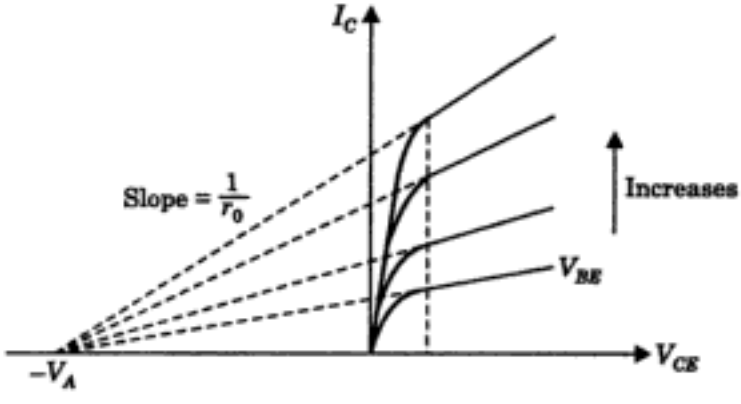


Fig. 4.11 CE output characteristics for an npn transistor with V_{BE} as a parameter. The curves extended backwards meet at the Early Voltage V_A.

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EXAMPLE 4.1

In a CE transistor, at V_{CE} of 1 V, V_{BE} is adjusted to give a collector current of 1 mA. Keeping V_{BE} constant, V_{CE} is increased to 11 V. Find the new value of I_C if the Early voltage V_A is 100 V.

Solution Output resistance r_0 from Eq. (4.31) is:

$$r_0 = \frac{V_A}{I_C} = \frac{100}{1} = 100 \text{ k}\Omega$$

For $V_{CE1} = 1$ V, $I_{C1} = 1$ mA

and for $V_{CE2} = 11$ V, let the collector current be I_{C2}

Therefore, $$r_0 = \frac{11 - 1}{I_{C2} - I}$$

Putting the value of $r_0 = 100$ kΩ, we get

$$I_{C2} = 1.1 \text{ mA} \quad \textbf{Ans.}$$

Cut-off mode. If $I_B = 0$ in Eq. (4.28a), we get

$$I_C\big|_{I_B = 0} = \frac{I_{CO}}{I - \alpha_F} = (1 - \beta_F) I_{CO} \tag{4.32}$$

$$\triangleq I_{CEO}$$

If base terminal is left open as shown in Fig. 4.12(a), then we can achieve $I_B = 0$, The collector current with collector-base reverse biased and base open circuited is designated by the symbol I_{CEO} and is shown in Fig. 4.12(a). The subscript in I_{CEO} means current flowing from *C to E* with third terminal (base) open.

Thus, for $\alpha = 0.996$ and $I_{CO} = 1$ μA,

$$I_{CEO} = \frac{1 \mu A}{1 - 0.996}$$

$$= 250 \text{ μA} = 0.25 \text{ mA}$$

This value of collector current is quite high and we cannot say that the transistor is in cut-off state even though the collector-base junction is reverse biased. Ideally, at cut-off collector current I_C should be zero, however, even if $I_C = I_{CO}$, the BJT is considered to be at cut-off. For a Ge transistor, α is close to unity, so I_{CEO} is very high. So, in order to cut-off a Ge transistor, emitter-base junction is reverse biased by a voltage of the order of 0.1 V. In the case of Si transistor, α is found to be very small (close to zero) while operating at low currents, therefore, $I_C = I_{CO}$ and the transistor is close to cut-off. In actual practice, V_{BE} is made equal to zero, that is, the base is shorted to emitter for a Si transistor. This results in a zero emitter current, i.e. $I_E = 0$. The current that flows from collector to base for collector-base junction reason-biased and $I_E = 0$ is designated as I_{CBO} and is shown in Fig. 4.15(b). The cut-off condition for a CE transistor can be redefined now as:

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$$I_C = I_{CBO} \; ; \; I_E = 0$$

and $V_{BE} = 0$ V for Si transistor

$V_{BE} = 0.1$ V reverse bias for Ge transistor

The collector current I_{CBO} in a practical transistor is usually larger than I_{CO} due to various factors such as surface leakage current, temperature effects and avalanche multiplication.

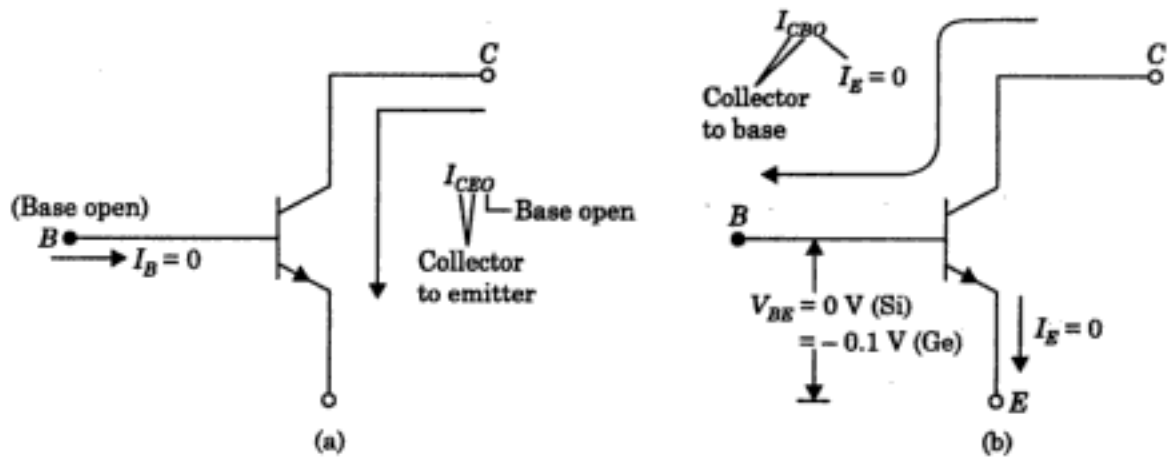


Fig. 4.12 Circuit showing (a) I_{CEO} (b) I_{CBO}.

Saturation mode. In the saturation region, both the emitter base and the collector base junctions are forward biased by at least the cut-in voltage, V_γ ($V_\gamma \approx 0.5$ V for Si and 0.2 V for Ge). The value of V_{BE} for a saturated transistor is usually higher compared to when transistor is operating in the forward active mode. It is usually taken as 0.8 V for Si transistor and 0.3 V for Ge transistor. Consider an npn BJT in the saturation mode shown in Fig. 4.13. In order that collector base junction is forward biased, the voltage at the base should be higher than the collector by, say, 0.5 V to 0.6 V. Assuming $V_{BE} = 0.8$ V and $V_{BC} = 0.6$ V, we find in Fig. 4.13,

$$\begin{aligned} V_{CE} &= V_{CB} + V_{BE} \\ &= -V_{BC} + V_{BE} \\ &= -0.6 \text{ V} + 0.8 \text{ V} \\ &= +0.2 \text{ V} \end{aligned}$$

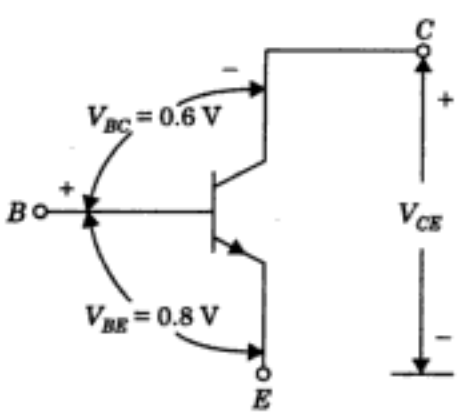


Fig. 4.13 Voltage distribution in an npn transistor for saturation mode.

The voltage V_{CE} for saturation mode is designated as $V_{CE,sat}$. The meaning of the saturation region is further understood by considering Fig. 4.14 where the output characteristics of a BJT in CE configuration has been drawn on an expanded scale in the region 0 to 0.6 V. In Fig. 4.14, the region left of the vertical dashed line drawn at $V_{CE,sat}$ is the saturation region. A load line for $R_C = 500\ \Omega$ and $V_{CC} = 10$ V drawn on these expanded characteristics will appear to be almost flat. It can be seen that at $V_{CE} = V_{CE,sat}$, as the transistor enters into saturation, I_C and V_{CE} do not change appreciably even with large changes in I_B. In Fig. 4.14, I_C is approximately equal to 20 mA for I_B varying form 120 μA to 200 μA.

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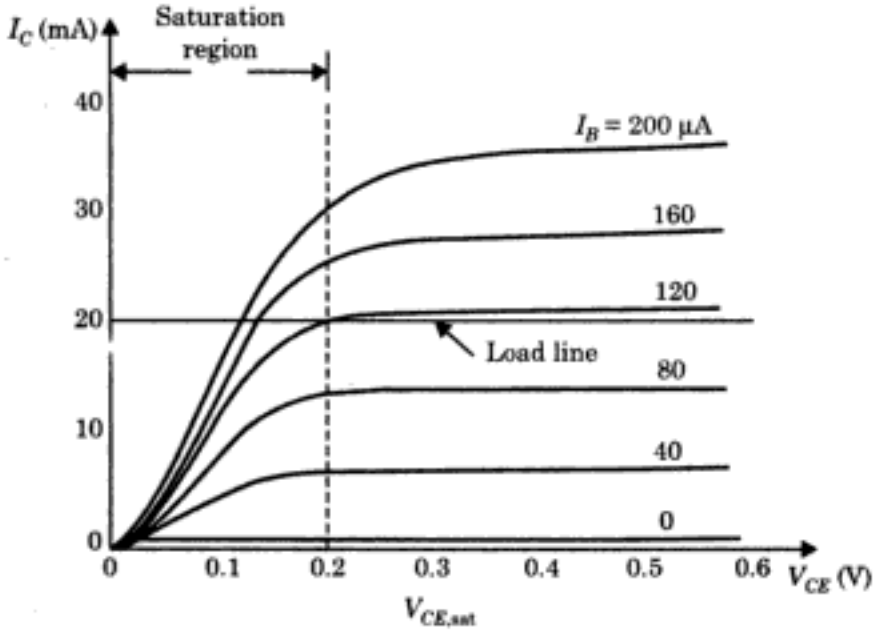


Fig. 4.14 CE output characteristics on the expanded scale in the region 0 to 0.6 V. The load line for R_C = 500 Ω, V_{CC} = 10 V appears almost flat.

Thus, we can say that the collector current I_C has saturated. The value of the collector current in saturation region is designated as $I_{C,sat}$ and is given by

$$I_{C,sat} = \frac{V_{CC} - V_{CE,sat}}{R_C} \tag{4.33}$$

Thus, the minimum base current required to drive a transistor into saturation is:

$$I_{B,min} = \frac{I_{C,sat}}{\beta_F} \tag{4.34}$$

If a transistor has to be operated in the saturation mode, we should design the circuit so that I_B is greater than $I_{B,min}$ by a factor of 2 to 10. The ratio of $I_{C,sat}$ and I_B (to ensure saturation) is called **forced** β and is given by

$$\beta_{forced} = \frac{I_{C,sat}}{I_B} \tag{4.35}$$

In Table 4.2, typical junction voltages required for an npn transistor to be in active, saturation and cut-off mode have been summarized. For pnp transistor, the signs for all the entries in the table will be reversed.

Table 4.2 Typical Junction Voltages for npn Transistor at 25°C

Parameter	*Cut-in voltage*	*Active mode*		*Saturation mode*		*Cut-off mode*
Type of BJT	V_γ	$V_{BE,active}$	$V_{CE,active}$	$V_{BE,sat}$	$V_{CE,sat}$	$V_{BE,cut\text{-}off}$
Si	0.5 V	0.7 V	> 0.2 V	0.8 V	≤ 0.2 V	0 V
Ge	0.1 V	0.2 V	> 0.1 V	0.3 V	≤ 0.1 V	− 0.1 V

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A number of solved examples given in this chapter, section 4.7 gives a further understanding of the various regions of operation of a transistor.

Input characteristics: Figure 4.15 shows the input characteristics of an npn transistor in *CE* configuration, drawn between V_{BE} and I_B for different values of V_{CE}. For $V_{CE} = 0$ V, the input characteristics is essentially that of a forward biased diode. In general, increase in V_{CE} with constant V_{BE} decreases the effective base width due to Early effect. This in turn reduces the base current due to reduced recombination thereby shifting the input characteristics to the right with increasing V_{CE}.

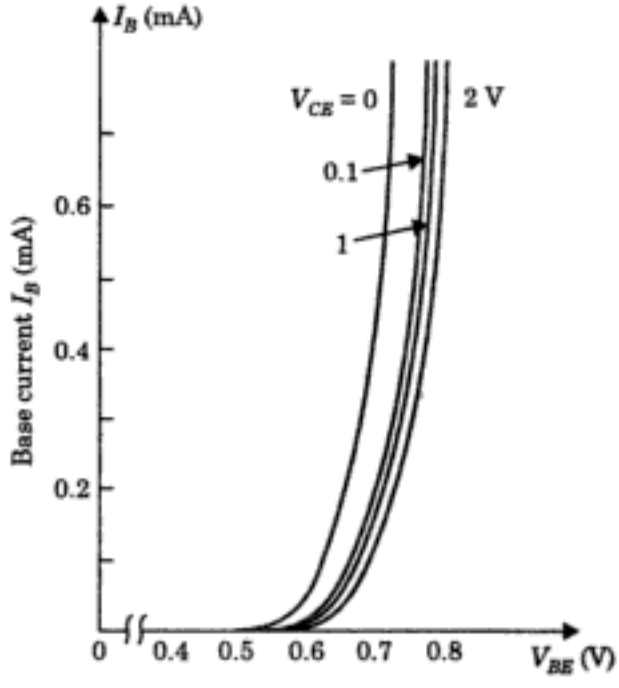


Fig. 4.15 Input characteristics of an npn transistor in CE configuration.

4.7.3 The Common Collector (CC) Configuration

For all practical purposes, the output characteristics of a transistor in CC configuration are similar to that for CE configuration. An npn transistor in CC configuration is shown in Fig. 4.16. Note that transistor has been drawn so that collector is common between input and output circuits.

The output characteristics are a plot of output emitter current I_E vs V_{EC} (emitter to collector voltage) for various values of input base current I_B. Thus, there is only a change of sign in the output voltage on the horizontal axis of the output characteristics of CE configuration. On the vertical axis, I_C can simply be replaced by I_E (assuming $\alpha \approx 1$). Thus, there is no noticeable change in the output characteristic of a transistor in CC configuration from that of CE configuration.

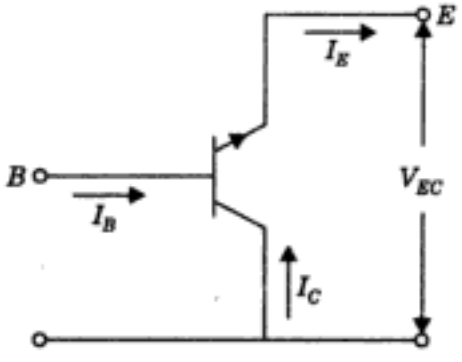


Fig. 4.16 An npn transistor in CC configuration.

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4.8 DC MODELS

Based upon the previous discussion, we can represent a transistor by a dc model for each of the operating regions. These models have been shown for an npn transistor in CE configuration, as this is the most useful configuration for amplification. The model, however, can be used for CB and CC configurations as well. Fig. 4.17(a) shows the dc model for the transistor in active mode of operation. We have seen from Eq. (4.30) that

$$I_C \simeq \beta_F I_B \qquad \text{(neglecting } I_{CO}\text{)}$$

Therefore, we have a controlled current source $\beta_F I_B$ showing that collector current I_C is controlled by base current I_B. Further, base-emitter junction must be forward biased by a voltage $V_{BE,\text{ active}}$ greater than cut-in-voltage V_γ. The value of $V_{BE,\text{ active}}$ is taken as 0.7V for a silicon transistor and 0.2V for Ge transistor as shown in Table 4.2.

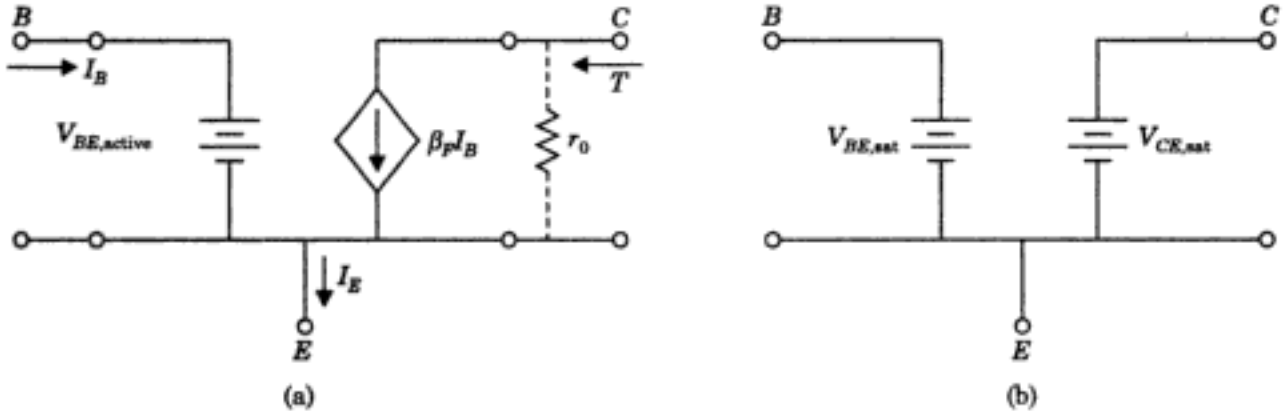


Fig. 4.17 DC model for npn transistor (a) active mode (b) saturation mode.

The resistance r_0 shown dashed in Fig. 4.17(a) is the output resistance due to early effect. Usually, r_0 is very large compared to the load resistance used in the circuit and, therefore is neglected. The dc model in the saturation mode is shown in Fig. 4.17(b). The values of $V_{BE,sat}$ and $V_{CE,sat}$ are given in Table 4.2 for Si and Ge transistors. Under cut-off condition a transistor is often represented by open circuits between each pair of the transistor terminals. This is assuming that the voltage drops due to I_{CBO} are very low and can be neglected.

The dc analysis of transistor circuits is performed for finding the Q-point. For this, we must first know the region of operation. The analysis is started by assuming a particular operating region and then verify the assumption as is shown by the following examples.

EXAMPLE 4.2

Determine the region of operation and all the node voltages and currents for the circuit in Fig. 4.18(a). Assume $\beta_F = 100$.

Solution As emitter-base junction is forward biased by the supply voltage V_{BB}, the transistor is either in forward active region or saturation region. We start with the assumption that the transistor is in active region. We replace the transistor by its dc model valid for active region and obtain the equivalent circuit shown in Fig. 4.18(b).

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In the active region, assume

$$V_{BE,\text{active}} = 0.7 \text{ V}$$

So, the voltage at emitter in Fig. 4.18(b) is

$$\begin{aligned} V_E &= V_{BB} - V_{BE,\text{active}} \\ &= 4 \text{ V} - 0.7 \text{ V} \\ &= 3.3 \text{ V} \end{aligned}$$

Further, we may write

$$\begin{aligned} I_E &= I_B + I_C \\ &= I_B + \beta_F I_B \\ &= (1 + \beta_F) I_B \end{aligned}$$

Writing KVL for base emitter loop, we get

$$V_{BB} - V_{BE,\text{active}} - (1 + \beta_F) I_B R_E = 0$$

Therefore,

$$\begin{aligned} I_B &= \frac{V_{BB} - V_{BE,\text{active}}}{(1 + \beta_F) R_E} \\ &= \frac{4 - 0.7}{(1 + 100)3.3} \\ &= 0.0099 \text{ mA} \end{aligned}$$

So $I_C = 100 \times .0099 = 0.99$ mA

and

$$\begin{aligned} I_E &= I_C + I_E \\ &= 0.99 + 0.0099 \\ &= 0.9999 \\ &\simeq 1 \text{ mA} \end{aligned}$$

The collector voltage V_C is given by

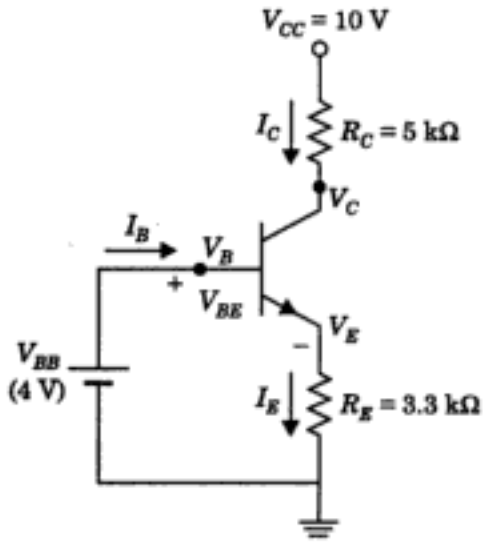
$$\begin{aligned} V_C &= V_{CC} - I_C R_C \\ &= 10 - 0.99 \times 5 \\ &= 5.05 \text{ V} \end{aligned}$$

Thus,

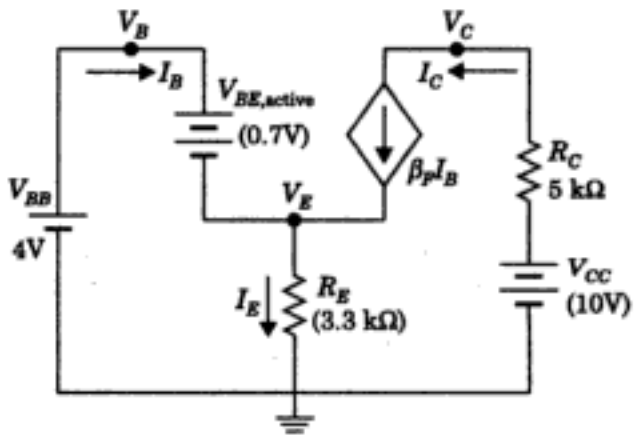
$$V_C = 5.05 \text{ V}, \quad V_E = 3.3 \text{ V}, \quad V_B = 4.0 \text{ V}$$

$$I_C = 0.99 \text{ mA}, \quad I_E = 1 \text{ mA} \text{ and } I_B = 0.0099 \text{ mA}$$

Since the base is at 4 V and the collector is at 5.05 V, so the collector junction is reverse biased by 1.05 V. The transistor is indeed in forward active region as assumed.



(a)



(b)

Fig. 4.18 (a) Circuit for Ex. 4.2
(b) Equivalent circuit.

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EXAMPLE 4.3

Determine the region of operation and the node currents and voltages for the circuit shown in Fig. 4.19.

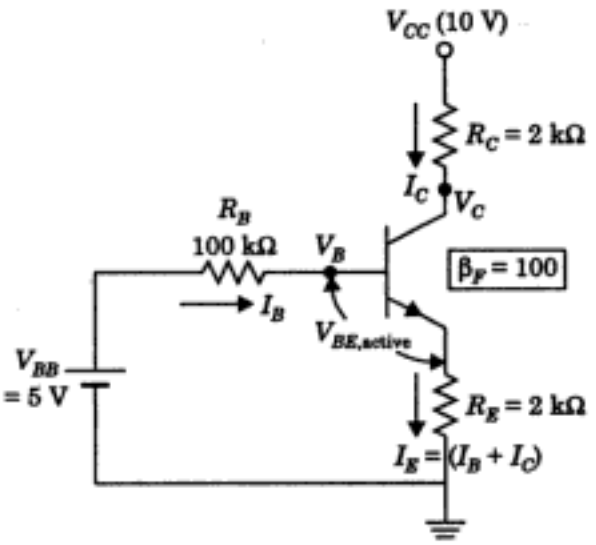


Fig. 4.19 Circuit for Example 4.3.

Solution It is not always necessary to draw the equivalent circuit. One can easily solve directly on the circuit as we do now. Assume that the transistor is in active region so that

$$V_{BE,\text{active}} = 0.7 \text{ V}$$

Applying KVL to the base circuit, we get

$$V_{BB} = I_B R_B + V_{BE,\text{active}} + (I_B + I_C)R_E \qquad \text{(i)}$$

In active region, we have

$$I_C = \beta_F I_B \quad \text{(neglecting } I_{CO}\text{)}$$

Equation (i), therefore, can be written in terms of I_B as:

$$V_{BB} = I_B R_B + V_{BE,\text{active}} + I_B(1 + \beta_F)R_E$$

Solving for I_B gives

$$I_B = \frac{V_{BB} - V_{BE,\text{active}}}{R_B + (1 + \beta_F)R_E}$$

$$= \frac{5 - 0.7}{100 + (101)2} = 0.014 \text{ mA}$$

The mode voltage, V_B is $V_B = V_{BB} - I_B R_B$

$$= 5 - 0.014 \times 100 = 3.6 \text{ V}$$

and, $I_C = \beta_F I_B = 100 \times 0.014 \text{ mA} = 1.4 \text{ mA}$

The voltage V_C at the collector node is:

$$V_C = V_{CC} - I_C R_C$$

$$= 10 - 1.4 \times 2$$

$$= 10 - 2.8 = 7.2 \text{ V}$$

Since base voltage V_B is 3.6 V and collector is at 7.2 V, so collector-base junction is reverse-biased by 3.6V. Thus our assumption that the transistor is in active region is valid.

EXAMPLE 4.4

Analyze the circuit shown in Fig. 4.20 for its region of operation. Assume $\beta_F = 100$.

Solution Assuming that the transistor is in active region of operation and solving for I_B gives

$$I_B = \frac{V_{BB} - V_{BE,\text{active}}}{R_B}$$

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$$= \frac{5 - 0.7}{50}$$

$$= 0.086 \text{ mA}$$

As $I_C = \beta_F I_B$ in active region, so

$$I_C = 100 \times 0.086$$

$$= 8.6 \text{ mA}$$

The voltage at the collector is:

$$V_C = V_{CC} - I_C R_C$$

$$= 10 - 8.6 \times 2$$

$$= 10 - 17.2 = -7.2 \text{ V}$$

Since emitter is grounded, so, $V_C = V_{CE} = -7.2$ V and is found to be negative. Thus our assumption is invalid. Further, it is not possible to obtain a negative value of V_{CE} with a positive collector supply voltage.

So, we must carry out the analysis again by assuming that the transistor is in saturation region (and not in active region).

The circuit has been redrawn as illustrated in Fig. 4.21 showing transistor with saturation voltages $V_{BE,sat} = 0.8$ V and $V_{CE,sat} = 0.2$ V.

From the base loop,

$$I_B = \frac{V_{BB} - V_{BE,sat}}{R_B}$$

$$= \frac{5 - 0.8}{50} = 0.084 \text{ mA}$$

and collector current I_C is:

$$I_C = I_{C,sat} = \frac{V_{CC} - V_{CE,sat}}{R_C}$$

$$= \frac{10 - 0.2}{2} = 4.9 \text{ mA}$$

The minimum value of I_B required to saturate the transistor is:

$$I_{B,min} = \frac{I_{C,sat}}{\beta_F}$$

$$= \frac{4.9 \text{ mA}}{100} = 0.049 \text{ mA}$$

Since I_B in the circuit is calculated as 0.084 mA, so it is greater than $I_{B,min}$. Thus the transistor is indeed in saturation mode.

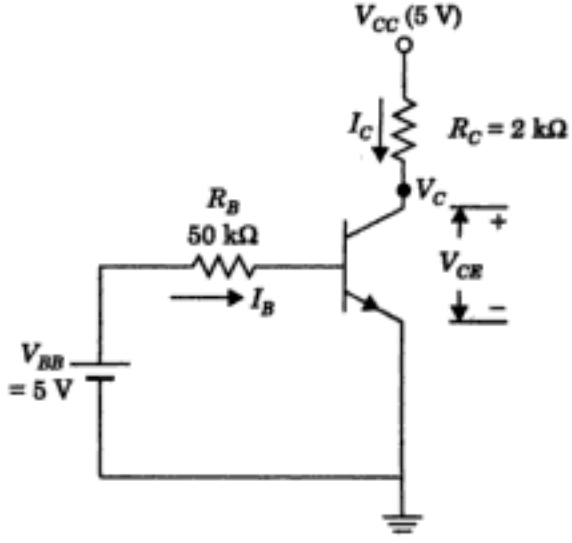


Fig. 4.20 Circuit for Example 4.4.

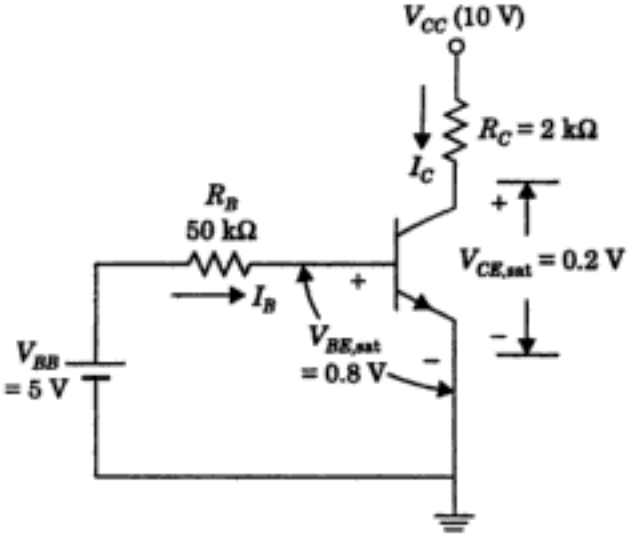


Fig. 4.21 Circuit for Example 4.4 redrawn assuming transistor in saturation.

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EXAMPLE 4.5

For the circuit shown in Fig. 4.22 find the value of R_B so as to drive the transistor into saturation. Assume $\beta_{min} = 50$.

Solution

Assume that the transistor is in saturation so that $V_{BE,sat} = 0.8$ V and $V_{CE,sat} = 0.2$ V. The collector current I_C is given by

$$I_C = I_{C,sat} = \frac{V_{CC} - V_{CE,sat}}{R_C}$$

$$= \frac{10 - 0.2}{1} = 9.8 \text{ mA}$$

The minimum base current required for the saturation is calculated from the minimum value of β_F. Thus,

$$I_{B,min} = \frac{I_{C,sat}}{\beta_{min}}$$

$$= \frac{9.8 \text{ mA}}{50} = 0.196 \text{ mA}$$

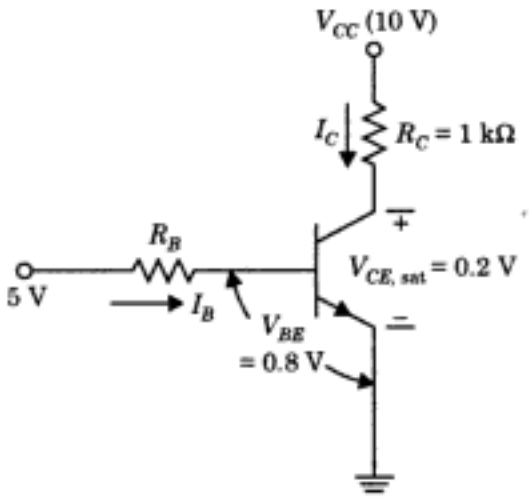


Fig. 4.22 Circuit for Example 4.5.

The value of R_B should be so chosen so that I_B in the circuit is greater than $I_{B,min}$ by a factor of, say, 10 to ensure saturation. Thus, the base current can be taken as:

$$I_B = 10\ I_{B,min}$$
$$= 1.96 \text{ mA}$$

The value of R_B required is, therefore,

$$R_B = \frac{5 - 0.8}{1.96}$$
$$= 2.14 \text{ kΩ}.$$

EXAMPLE 4.6

A pnp transistor is shown in Fig. 4.23. Find the voltage V_{01} and V_{02}. Assume $\beta_F = 100$.

Solution Note the direction of currents in the Fig. 4.23 for pnp transistor. Assume active region of operation, so $V_{BE,active} = -0.7$ V (For pnp, V_{BE} is negative). Writing KVL for base-emitter circuit, [taking $I_E = (1 + \beta_F)I_B$], we have

$$V_{EE} - I_E R_E + V_{BE} - I_B R_B - 2.5 = 0$$

$$10 - 6.8\ (1 + \beta_F)I_B - 0.7 - I_B \times 100 - 2.5 = 0$$

Solving for I_B gives

$$I_B = 0.0086 \text{ mA}$$

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So $I_C = \beta I_B$

$= 0.86$ mA

and $I_E = I_C + I_B$

$= 0.86 + 0.0086$

$= 0.87$ mA

Now, V_{01} is given by

$$V_{01} = V_{CC} + I_C R_C$$

$$= -10 + 0.86 \times 10$$

$$= -10 + 8.6$$

$$= -1.4 \text{ V}$$

and $V_{02} = V_{EE} - I_E R_E$

$= 10 - 0.87 \times 6.8$

$= 4.08$ V

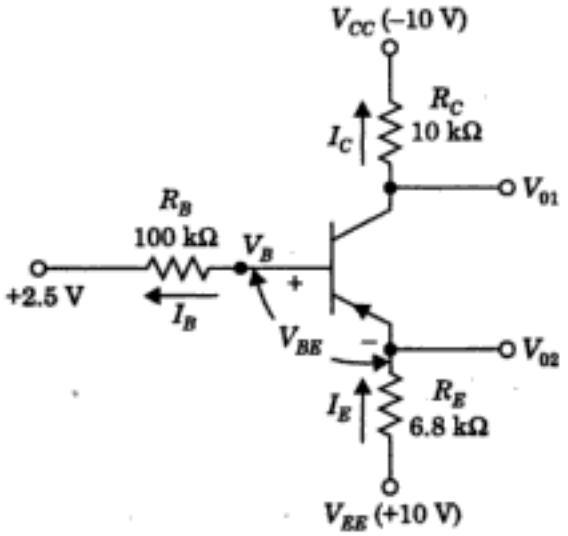


Fig. 4.23 Circuit diagram for Example 4.6 (a pnp transistor).

The voltage at base is given by

$$V_B = 2.5 + 100 \times .0086 = 3.36 \text{ V}$$

As base voltage, V_B is 3.36 V and voltage at collector is −1.4 V, collector base junction is reverse biased. Thus the transistor is indeed in active region as assumed.

EXAMPLE 4.7

The pnp transistor in Fig. 4.24 has $\beta_F = 50$. Find the value of R_C to obtain $V_C = +5$ V. What happens if the transistor is replaced with another transistor having $\beta = 100$?

Solution Assume transistor in active region. Writing KVL for the base circuit gives

$$V_{EE} + V_{BE,\text{active}} - I_B R_B = 0$$

or $$I_B = \frac{V_{EE} + V_{BE,\text{active}}}{R_B}$$

Putting $V_{BE,\text{active}} = -0.7$ V (for pnp transistor)

$$I_B = \frac{10 - 0.7}{100} = 0.093 \text{ mA}$$

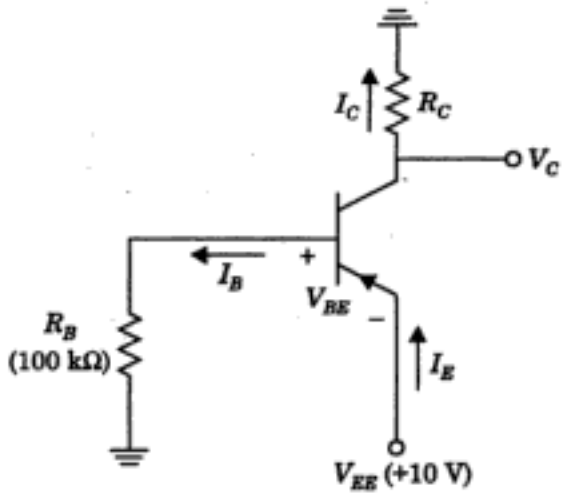


Fig. 4.24 Circuit diagram for Example 4.7 (a pnp transistor).

If $\beta_F = 50$,

$$I_C = \beta_F I_B$$

$$= 50 \times 0.093 = 4.65 \text{ mA}$$

To obtain $V_C = 5$ V

Select $$R_C = \frac{V_C}{I_C}$$

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$$= \frac{5}{4.65}$$

$$= 1.08 \text{ k}\Omega$$

If $\beta_F = 100$,

$$I_C = 100 \times 0.093$$

$$= 9.3 \text{ mA}$$

Now,

$$V_C = I_C R_C$$

$$= 9.3 \times 1.08$$

$$= 10.04 \text{ V}$$

which is greater than the base voltage. The transistor therefore goes into saturation, since collector junction gets forward biased.

EXAMPLE 4.8

Determine the labelled voltages and currents in the circuit shown in Fig. 4.25. Assume $\beta_F = 100$.

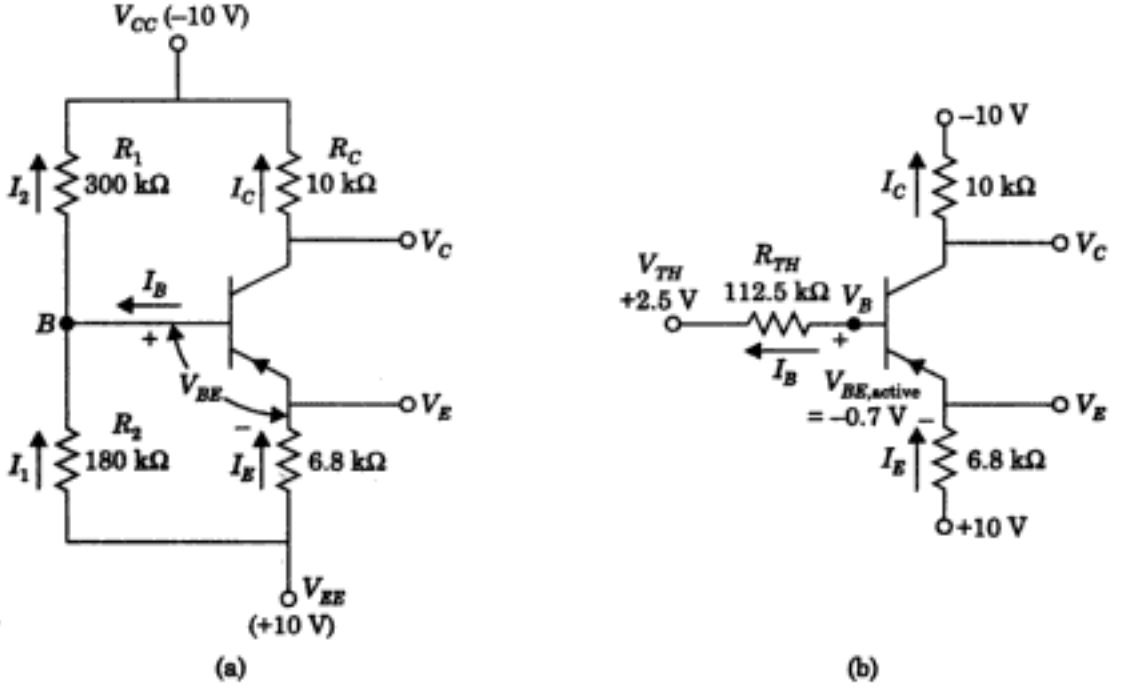


Fig. 4.25 (a) Circuit diagram for Example 4.8, (b) Equivalent circuit.

Solution Assume that the transistor is in active region. So $V_{BE,active} = -0.7$ V. We can simplify the circuit by applying Thevenin's theorem at point B. The equivalent circuit has been redrawn as shown in Fig. 4.25(b).

$$R_{TH} = 180 \parallel 300$$

$$= \frac{180 \times 300}{480} = 112.5 \text{ k}\Omega$$

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$$V_{TH} = V_{EE} - \frac{R_2(V_{EE} - V_{CC})}{(R_1 + R_2)}$$

$$V_{TH} = 10 - \frac{180 \times 20}{480} = 2.5 \text{ V}$$

Writing KVL for the base emitter circuit, we get

$$10 - (I_B + I_C)\ 6.8 - 0.7 - 112.5 \times I_B - 2.5 = 0$$

Using $I_C = \beta_F I_B$, and solving for I_B gives

$$I_B = 0.0085 \text{ mA}$$

So $I_C = \beta_F I_B$

$$= 100 \times 0.0085 = 0.85 \text{ mA}$$

and $I_E = I_B + I_C = 0.86 \text{ mA}$

Now, $V_C = -10 + 10 \times 0.85 = -1.5 \text{ V}$

and $V_E = 10 - 6.8 \times 0.86 = 4.15 \text{ V}$

$\therefore$ $V_B = 4.15 - 0.7 = 3.45 \text{ V}$

Current I_1 in Fig. 4.25 is given by

$$I_1 = \frac{10 - 3.45}{180} = 0.036 \text{ mA}$$

and $I_2 = I_1 + I_B$

$$= 0.036 + 0.0085$$

$$= 0.044 \text{ mA}$$

4.9 AMPLIFYING ACTION OF A TRANSISTOR

The amplifying action in a transistor is achieved because the current from a low resistance input circuit is transferred to a high resistance output circuit. The word transistor has originated from the 'transfer resistance' action taking place inside a transistor. This is further demonstrated by considering a simple CB transistor used as an amplifier shown in Fig. 4.26. The supply voltages V_{BB} and V_{CC} bias the transistor in active region of operation. The AC signal source V_s which has to be amplified is connected in the input circuit and the load resistance R_L across which amplified output is taken is placed in the output circuit. The input resistance R_i of the emitter-base junction is usually small

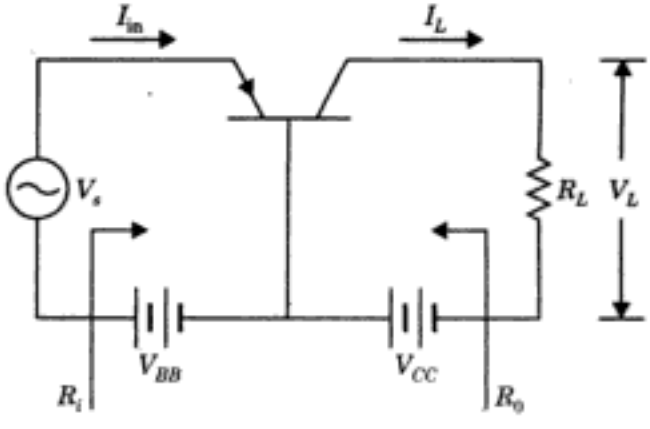


Fig. 4.26 A CB amplifier showing amplifying action in a transistor.

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(as it is forward biased) and is of the order of 10 to 100 Ω only. The output resistance R_0 is quite high of the order of 50 kΩ to 1 MΩ due to reverse biased collector-base junction. The amplifying action of the transistor can be demonstrated by taking a simple example.

If we assume, R_i = 20 Ω, R_0 = 100 kΩ and input signal amplitude V_m = 20 mV, then input current

$$I_{in} = \frac{V_m}{R_i} = \frac{20}{20} = 1 \text{ mA}$$

Assume $\alpha = 1$, so

$$I_L \approx I_{in}$$

The output voltage across load resistance is:

$$V_L = I_L R_L$$
$$= 1 \times 5 = 5 \text{ V}$$

The voltage gain A_V is:

$$A_V = \frac{V_L}{V_m}$$
$$= \frac{5}{20} = 250$$

Thus, a voltage gain of 250 has been achieved. Whenever, we perform AC analysis, all DC supply voltages are assumed to be *replaed by a short circuit.* A transistor when used as a CB amplifier can provide voltage gain from 50 to 300. However, the current gain is always less than unity. Therefore a CB amplifier finds limited applications. However, a CE amplifier provides both voltage gain and current gain and is most extensively used for most of amplification applications.

This simple example taken above only illustrates that a BJT can be used for amplification of small AC signals. In chapter 6, we will analyze the amplification properties of a BJT in different configurations, that is CB, CE and CC in detail.

4.10 TRANSISTOR AS A SWITCH/INVERTER

One of the very important applications of a BJT is its use as a switching device for the computer logic circuits. The circuit shown in Fig. 4.27 (a) can be used as a switch/inverter by proper selection of resistances.

The transistor is made to operate in the two extreme modes, i.e., it operates either in cut-off or saturation mode. Consider an input signal shown in Fig. 4.27(b) applied at the input of the circuit in Fig. 4.27(a). When input $V_{in} = -V_1$, transistor is designed to operate in cut-off state by proper choice of R_B, R_C. Now I_C is close to zero, therefore the output voltage $V_0 \approx V_{CC}$ as shown in Fig. 4.27(c). For $V_{in} = V_2$, transistor goes into saturation or is driven 'ON'. When a transistor is biased in saturation region, we know that $V_{CE} = V_{CE,sat}$. So that the output voltage $V_0 = V_{CE,sat}$ = 0.2 V (~ 0 V). Thus, the output voltage is either high ($\simeq V_{CC}$ for transistor OFF) or low ($\simeq 0\,V$ for transistor ON). So, the circuit is indeed working as a switch or inverter.

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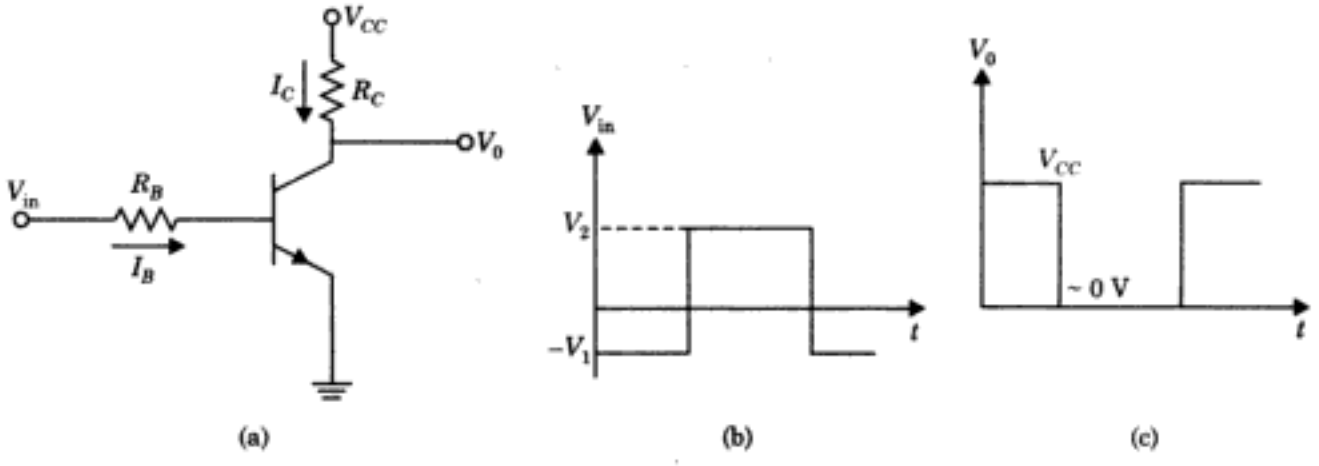


Fig. 4.27 (a) BJT used as a switch/inverter, (b) Input waveform, (c) Output waveform.

EXAMPLE 4.9

In Fig. 4.27, V_{CC} = 10 V, R_B = 180 kΩ, R_C = 2.4 kΩ. Analyze the circuit for a square wave input of amplitude 0 to 10 V. Assume β_F = 125.

Solution For $V_{in} = 0$ V, $I_B = 0$

Assume $I_C = I_{CEO} \approx 0$ mA

Therefore, the voltage drop across $R_C = 0$ V

and $V_0 = V_{CC} = 10$ V

Now, consider the situation when V_{in} = 10 V. Assume that the transistor is in saturation. So $V_{BE,sat}$ = 0.8 V and $V_{CE,sat}$ = 0.2 V.

Now,
$$I_B = \frac{V_{in} - V_{BE,sat}}{R_B}$$
$$= \frac{10 - 0.8}{180} = 0.05 \text{ mA}$$
$$I_{C,sat} = \frac{V_{CC} - V_{CE,sat}}{R_C}$$
$$= \frac{10 - 0.2}{2.4} = 4.08 \text{ mA}$$
$$I_{B,min} = \frac{I_{C,sat}}{\beta_F}$$

and
$$= \frac{4.08}{125} = 0.03 \text{ mA}$$

Since $I_B > I_{B,min}$, so the transistor is in saturation mode and

$$V_0 = V_{CE,sat}$$
$$= 0.2 \text{ V} \approx 0 \text{ V}$$

The circuit is working as a switch or as an inverter.

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BJT switching speed: In a practical transistor, the transistor takes finite time to switch from one state to another as shown by the collector current waveform in Fig. 4.28. As can be seen the collector current does not respond to the input signal immediately. The total time required for the transistor to switch from OFF state to ON state is designated as t_{on} and is defined as

$$t_{on} = t_d + t_r$$

where t_d = Time required for the current to rise to 10 percent of its maximum (saturation) value and is called delay time

t_r = Time required for the current to rise from 10 to 90 percent of the maximum value and is called rise time

Similarly, the total time required for the transistor to switch from ON to OFF state is referred to as t_{off} and is given by

$$t_{off} = t_s + t_f$$

where t_s = storage time taken by the collector current to drop to 90 percent of maximum value of current

t_f = Time required by I_C to fall from 90 percent to 10 percent of $I_{C,sat}$.

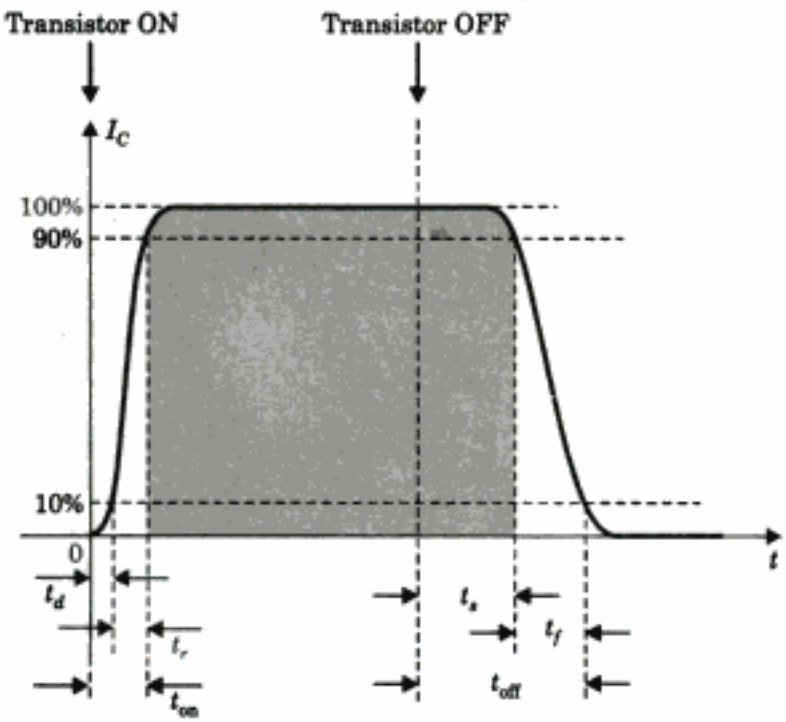


Fig. 4.28 Waveform of collector current displaying the delay time, rise time, storage time and fall time.

The delay time occurs as the minority carriers take time to cross base region and be collected at the collector and attain a value equal to 10 percent of its maximum. The rise time and fall time occur due to the fact that if a base current step is used to saturate the transistor or return it from saturation to cut-off, the transistor collector current must traverse through the active region. The time interval t_s results from the fact that a transistor has excess minority carriers stored in the base when in saturation. The excess storage charge

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has to be removed to turn off the transistor. The storage time, in general, is several times higher than the rise time or fall time. For high speed digital circuits, the storage time is reduced by not driving transistor deep into saturation. A well-known method for preventing a transistor from saturating is the use of *Schottky diode* in a BJT. A BJT using such a diode is called **Schottky transistor**.

SUMMARY

- In a BJT, emitter region is heavily doped compared to the collector region. Base region is the most lightly doped region.
- Area of emitter region is smaller as compared to collector region and the base region is very thin compared to other regions.
- A BJT can operate in one of the three possible modes: Cut off (both junctions reverse biased); active (emitter base junction forward biased and collector base junction reverse biased); saturation (both junctions forward biased).
- For amplifier applications, BJT is operated in the active mode.
- Switching applications make use of the cut off and saturate modes.
- Large signal current gains α_F and β_F are related by the relationships:

$$\alpha_F = \frac{\beta_F}{1+\beta_F};\ \beta_F = \frac{\alpha_F}{1-\alpha_F}$$

  The parameter α_F is always less than unity and β_F is large (50 to 200).
- For a BJT (pnp and npn) biased in forward active mode, $I_C = \alpha_F I_E + I_{CO}$ holds good.
- For a BJT in active mode, DC analysis is carried out by assuming $|V_{BE}| = 0.7$ V.
- The slope of the output characteristics of a transistor in CE configuration is higher than that in CB configuration due to Early Effect.
- Base width modulation for increasing $|V_{CB}|$ results in (i) increase in α_F, (ii) increase in emitter current, I_E, (iii) breakdown or punch through (for large V_{CB}).
- In a saturated Si transistor, $|V_{CE,sat}| = 0.2$ V; $|V_{BE,sat}| = 0.8$ V; $I_{C,sat} = (V_{CC} - V_{CE,sat})/R_C$. The current I_B should be greater than $I_{C,sat}/\beta_{min}$ for transistor to be in saturation.
- At cut-off in a Si transistor, $V_{BE} = 0$ V, $I_C = I_{CBO}$, $I_E = 0$.

REVIEW QUESTIONS

4.1 Show the actual direction of currents I_E, I_B and I_C for (i) pnp (ii) npn transistor biased in active region.

4.2 Which of the transistor currents is always largest? Which is always smallest? Which two currents are almost equal?

4.3 What is the source of leakage current in a transistor?

4.4 Define current gain α_F and explain why it is not constant.

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4.5 Plot the output characteristics of a transistor in CB configuration and indicate the various regions of operation on it. Explain the shape of characteristics.

4.6 Explain the various effects of base width modulation.

4.7 Indicate the active and saturation region on the CE output characteristics of a transistor. Explain why its slope is more compared with the slope of CB output characteristics.

4.8 Give the typical junction voltages for a Si transistor in (i) active region (ii) saturation region.

4.9 Explain the condition for a transistor to saturate.

4.10 Draw the Ebers-Moll model of an npn transistor and write the EM equations.

4.11 Explain the terms I_{CEO} and I_{CBO}. Which of the two is greater?

4.12 Explain the cut-off conditions in a transistor.

4.13 Explain why a transistor is able to amplify AC input signals.

4.14 Explain the working of a transistor as a switch.

4.15 Explain the switching time t_{on} and t_{off} in a BJT.

4.16 How storage time is reduced in a transistor?

NUMERICAL PROBLEMS

P4.1 In a BJT, base current is 7.5 μA and the collector current is 940 μA. Find α_F and β_F for the device.

(Ans: $\alpha_F = 0.992$; $\beta_F = 125.3$**)**

P4.2 The Early voltage for a BJT is 200 V. Find its output resistance at (i) 1 mA, (ii) 100 μA.

(Ans: 200 kΩ, 2.0 MΩ**)**

P4.3 For the circuit shown in Fig. P-3, Find (a) the region of operation of the transistor, (b) V_0. Assume $\beta_F = 100$.

(Ans: Saturation, – 1.65 V**)**

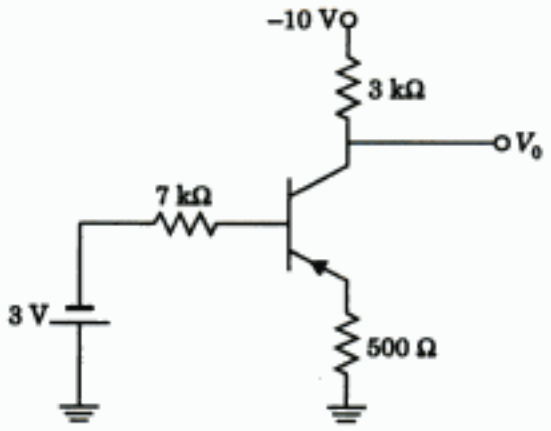


Fig. P-3

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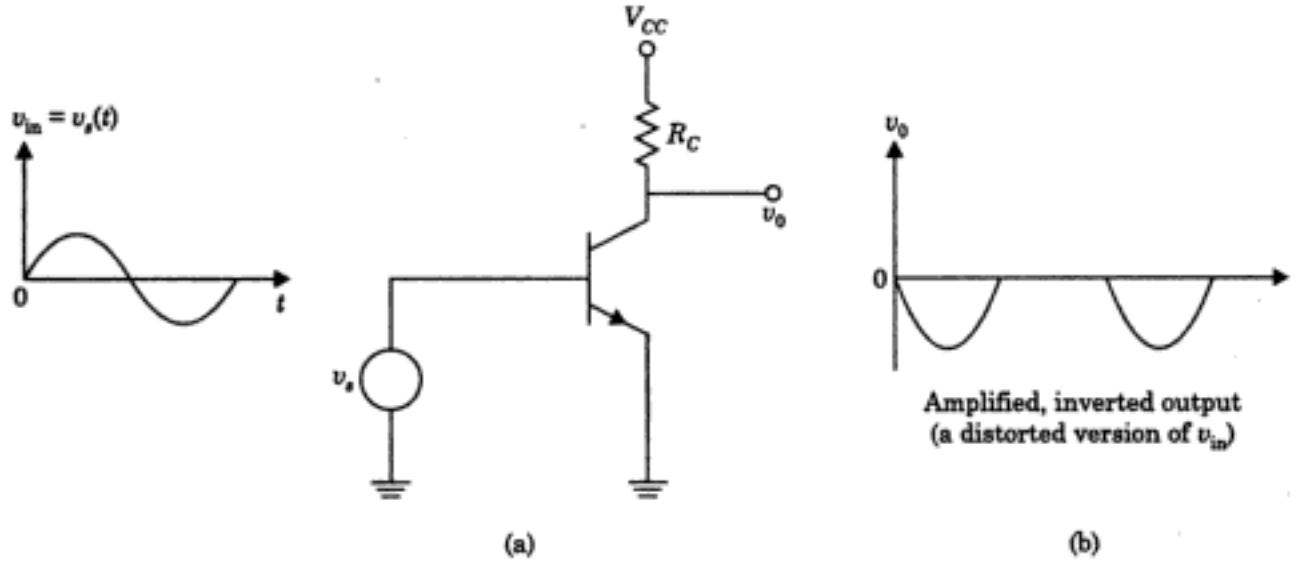


Fig. 5.2 (a) A simple CE amplifier without bias, (b) Output v_0 for sinusoidal input v_s.

input sine signal. It can be seen that during the positive half cycle of the input waveform (for $v_s > V_\gamma$), the base-emitter junction is forward biased and, therefore, the transistor works in the forward active mode. However, for the negative half cycle of the input signal, base emitter junction is reverse biased and transistor goes into cutoff. The output signal waveform available across the load resistance R_C shown in Fig. 5.2(b) is clipped or half wave only. The output voltage waveform also gets inverted due to 180° phase shift introduced by the transistor. Thus, in order to obtain an exact sinusoidal waveform at the output, it is necessary to provide a dc bias in the base circuit so that the base-emitter junction is forward biased even when the input signal is going through the negative half cycle. The problem is solved by placing a dc supply voltage, V_{BB} in the base circuit as shown in Fig. 5.3. Thus, ac signal v_s is superimposed on the dc voltage V_{BB}, so that the emitter junction will remain forward-biased even when input signal is going through its negative half cycle. Now we can get a full wave output waveform. In this circuit we are using two independent supplies V_{CC} and V_{BB} which is usually not desirable. The need for a separate supply is easily eliminated by a fixed bias circuit.

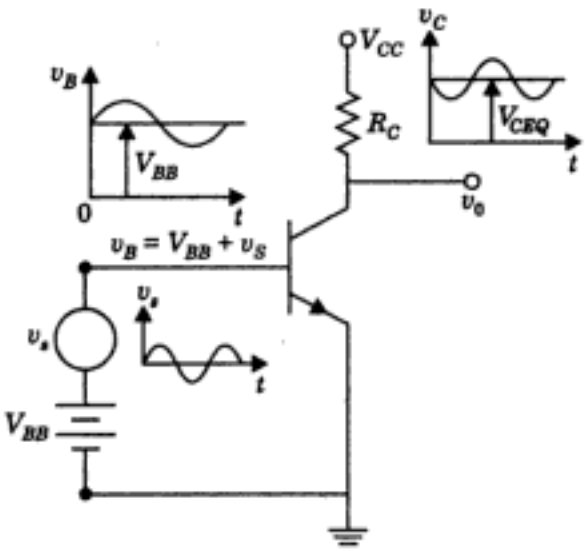


Fig. 5.3 A separate supply, V_{BB}, used to bias the CE amplifier.

5.3 FIXED BIAS CIRCUIT

Figure 5.4(a) shows a fixed bias circuit in which Q-point is established using a single collector supply V_{CC}. By proper selection of the resistance R_B in Fig. 5.4(a), the desired value of base current I_B is established. In any practical amplifier, capacitors C_1 and C_2 are also

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connected as shown in Fig. 5.4(a). The capacitor C_1 couples the ac input signal to the base of the transistor. The value of the capacitor C_1 is chosen large (0.1 μF to 10 μF) so that even at the lowest input signal frequency, its reactance is small enough to act as a short circuit at that frequency. This will ensure that ac input signal will not drop across capacitor C_1 in the entire frequency range of interest. The reactance of the capacitor C_1 is infinite for dc signals and it acts as an open circuit for dc signals. Thus, capacitor C_1 acts both as a coupling capacitor (to couple ac input signal) and blocking capacitor (to block dc signal coming from previous stage or ac signal source). Similarly, capacitor C_2 connected at the output permits only the ac signal across the load resistance R_C to go onto the next stage by blocking dc voltage at collector C. It is necessary to block the dc voltage from going to the next stage, otherwise it will disturb the DC conditions (and hence change the bias voltages) of the next stage.

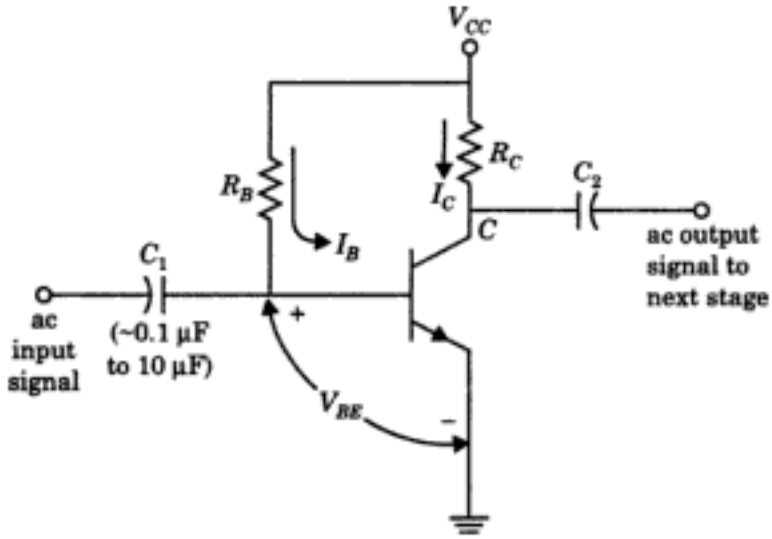


Fig. 5.4(a) A CE amplifier using a fixed-bias circuit.

Analysis of fixed-bias circuit: In order to determine the Quiescent point or the dc operating point of the transistor amplifier shown in Fig. 5.4(a), we draw its dc equivalent circuit. Under dc conditions, both capacitors C_1 and C_2 are open circuit and assuming that the transistor is in forward active mode, the dc equivalent circuit will be as shown in Fig. 5.4(b). (Here transistor has been replaced by its dc model valid for forward active mode).

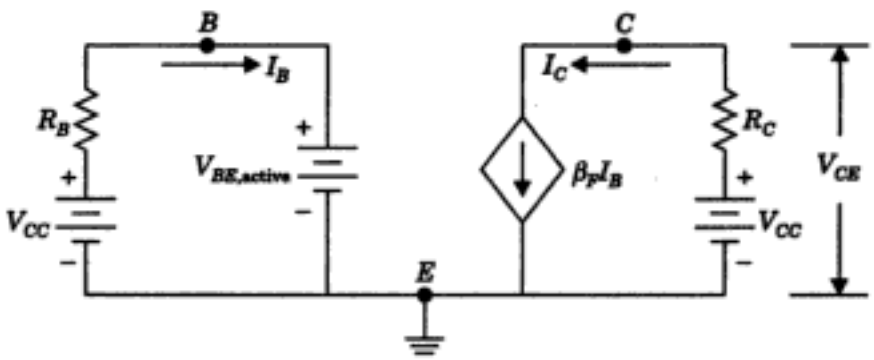


Fig. 5.4(b) DC equivalent circuit for Fig. 5.4(a).

From the base loop,

$$I_B = \frac{V_{CC} - V_{BE,active}}{R_B} \tag{5.1}$$

The value of $V_{BE,active}$ is given as:

$$V_{BE,active} = \begin{cases} 0.2\text{ V} & \text{for Ge transistor} \\ 0.7\text{ V} & \text{for Si transistor} \end{cases}$$

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The Q-point is established by choosing resistance R_B so as to obtain the desired base current. For this base current I_B, the current I_C is readily calculated by using the well known relationship in the active region.

$$I_C \approx \beta_F I_B \qquad \text{(neglecting } I_{CO}\text{)}$$

Now,
$$V_{CE} = V_{CC} - I_C R_C \tag{5.2}$$

Thus, the values of I_B, I_C and V_{CE} completely define the Q-point.

In this analytical method of finding the Q-point, the value of β_F should be known. This circuit is called a fixed-bias circuit as it provides a fixed value of base current for a given R_B.

EXAMPLE 5.1

Design a fixed bias circuit, that is, find R_B and R_C so that $I_B = 40\ \mu A$ and $V_{CE} = 6$ V. Given: $V_{CC} = 12$ V, $\beta_F = 80$ and $V_{BE} = 0.7$ V.

Solution Using Eq. (5.1),

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{12 - 0.7}{40} = 282.5\ \text{k}\Omega$$

and
$$I_C \approx \beta_F I_B$$
$$= 80 \times 40 = 3.2\ \text{mA}$$

Therefore,
$$R_C = \frac{V_{CC} - V_{CE}}{I_C}$$

$$= \frac{12 - 6}{3.2} = 1.875\ \text{k}\Omega$$

Thus, $R_B = 282.5\ \text{k}\Omega$, $R_C = 1.875\ \text{k}\Omega$

5.4 AC AND DC LOAD LINES

Figure 5.5 shows a CE amplifier using fixed bias arrangement. A load resistance R_L is also connected at the output through a coupling capacitor C_2. The capacitor C_2 blocks the dc signal across R_C so that only ac signal is available at the load, R_L. In many applications, it is desirable that dc signal does not flow through the load. For example, in a transistorized radio, speaker is the load and any dc signal flowing through it will cause magnetization of the coil, and produce distortion. Thus, R_L is the actual or practical load in the circuit.

The Q-point will now have to be redefined for the circuit in Fig. 5.5. Under dc conditions, capacitors C_1 and C_2 are open and, therefore, the load in the circuit is R_C only. The corresponding dc load line is shown on the volt-ampere characteristics of an npn transistor in Fig. 5.6. The operating point Q_1 is located at the centre of the load line so as to use a base current swing of 40 μA. However under ac conditions, capacitors C_1 and C_2 are short and

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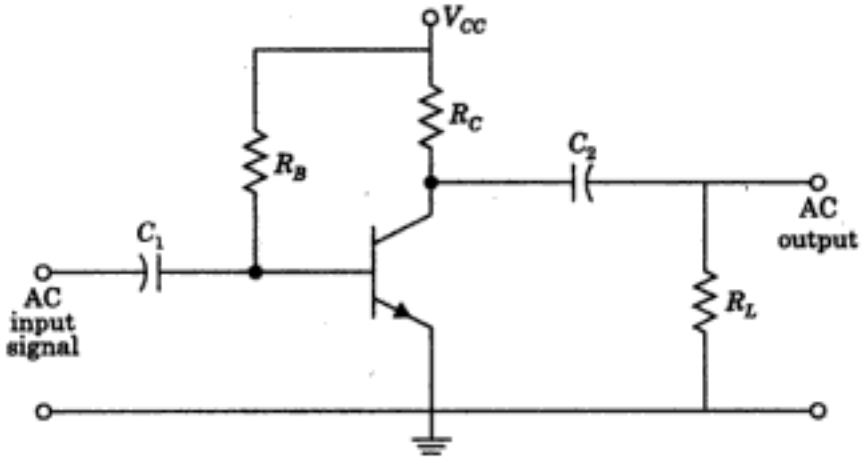


Fig. 5.5 A CE amplifier with an ac load R_L.

the effective load in the circuit is $R_L' = R_C \parallel R_L$. We, therefore, draw an ac load line through the operating point Q_1 with a slope equal to $(-1/R_L')$ as indicated in Fig. 5.6. The resistance R_L is usually less than R_C, so that R_L' will be less than R_C. For example, if $R_C = 4$ k and R_L is 1 k, then $R_L' = 0.8$ k. Thus the slope of the ac load line is more than the dc load line in Fig. 5.6. It can be seen that under ac conditions Q-point is not in the centre of the ac load line and, therefore, it is not the proper choice of Q-point. Thus, if the Q-point is shifted from Q_1 to Q_2 on the dc load line, the ac load line drawn through Q_2 with a slope of $-1/R_L'$ clearly shows that an input base current swing of about 60 μA is easily possible without distortion. The new operating point Q_2 is usually found by trial and error.

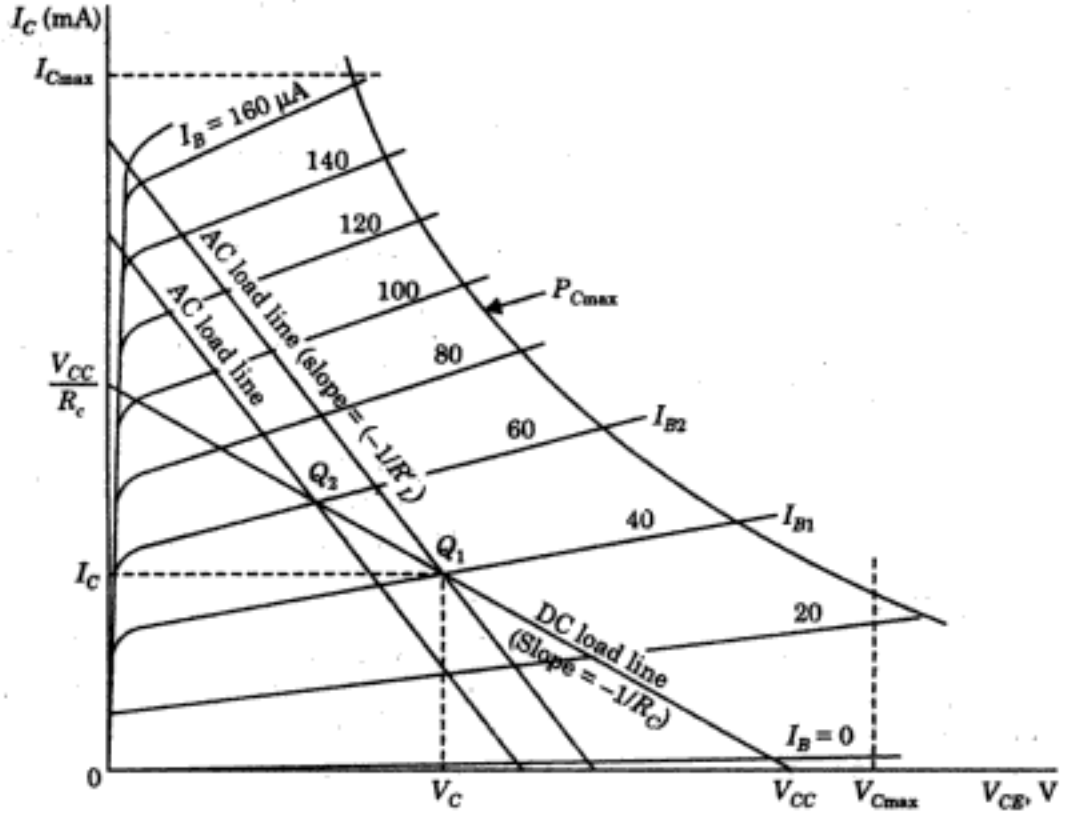


Fig. 5.6 ac and dc load lines on the CE characteristics of a transistor ($R_L' = R_C \| R_L$).

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5.5 OPERATING POINT STABILITY

Once the operating point has been established, it is very important that it remains stable. The various reasons that cause the shift of the Q-point are the following:

1. The wide variation in the current amplification factor β_F (often 5 to 1 or more) of the transistors having the same number due to manufacturing limitations.
2. Variation in the collector reverse saturation current I_{CO} with temperature (I_{CO} doubles for every 10°C rise in temperature).
3. Variation in the quiescent base emitter voltage V_{BEQ} with temperature (V_{BE} falls at the rate of 2.2 mV for rise of every degree in temperature).
4. Variation in the supply voltage due to imperfect regulation.
5. Variation in the circuit resistances due to tolerance and temperature changes.

Out of the above, the two parameters viz. temperature variation and β variation play an important role in effecting the stability of the Q-point, and will be discussed in detail.

Effect of β-variation on Q-point: Figure 5.7 shows the V-I characteristics of an npn transistor for two values of β_F. Solid line curves represent the transistor with lower β_F while dotted line curves are for the transistor of the same type but with a higher β_F. If I_B is fixed, say, at I_{B2} using the fixed bias circuit of Fig. 5.4(a), it can be seen that the replacement of the transistor with higher β_F will shift the operating point from Q_1 to Q_2. Thus, even though the current I_B is fixed, the Q-point is not stable as value of β_F changes.

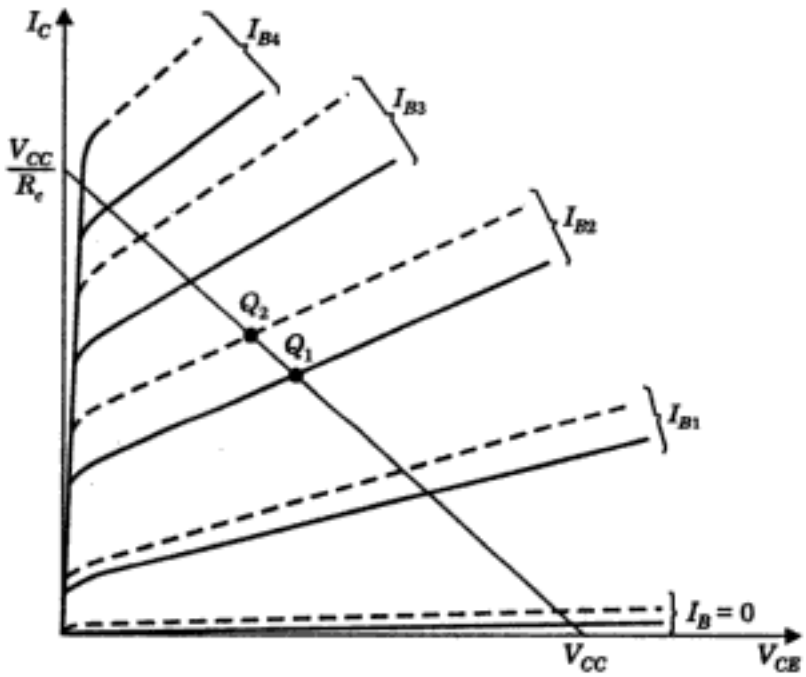


Fig. 5.7 Operating point changes from Q_1 to Q_2 for a transistor with higher β_F.

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Effect of temperature variation on Q-point: We know that I_{CO} doubles for every 10°C rise in temperature. The increase in I_{CO} increases I_C [$\because$ $I_C = \beta_F I_B + (1 + \beta_F) I_{CO}$] which in turn increases the collector junction temperature and I_{CO} further increases. This process is cumulative and changes the *V-I* characteristics of a transistor. Figs. 5.8(a) and (b) shows the output characteristics of an npn transistor at temperature T_1 = 25°C and T_2 = 100°C respectively. It can be seen that the curves have shifted upwards as temperature increases from 25°C to 100°C. Consider that the Q-point has been established using a fixed bias circuit at I_B = 40 μA at 25°C in Fig. 5.8(a). It can be seen that the operating point has shifted upwards at 100°C and is quite close to the saturation region which is not a good choice. We next discuss a circuit that provides a stable operating point against variations in β_F and temperature.

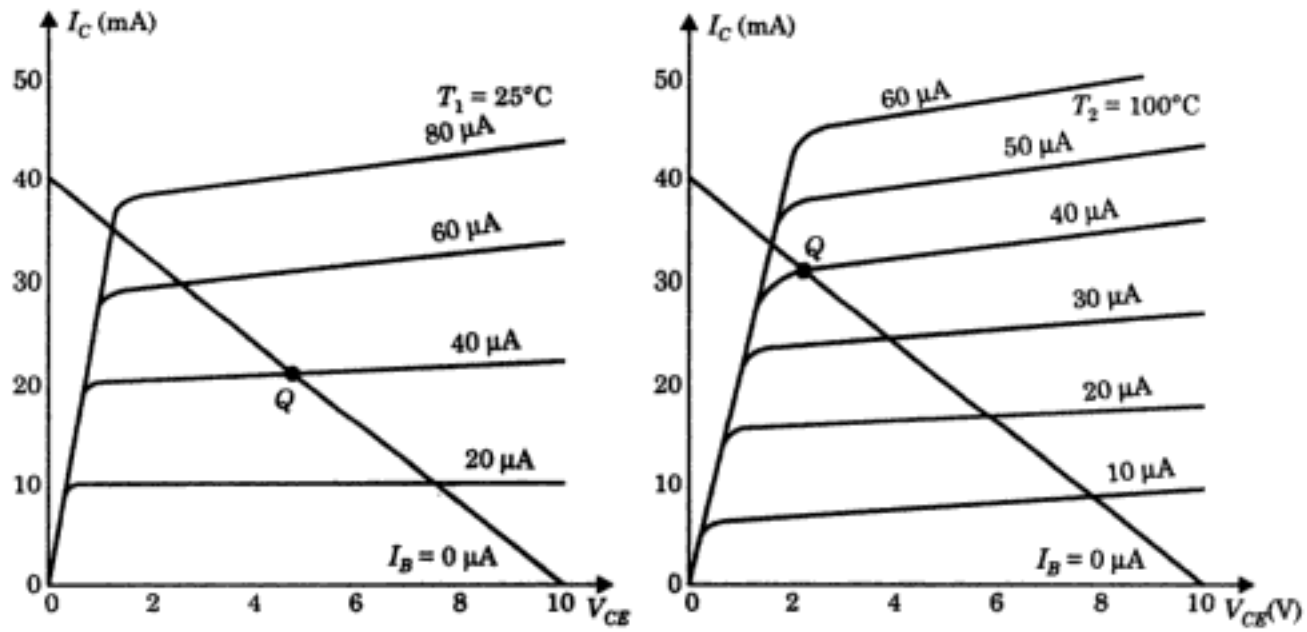


Fig. 5.8 Output characteristics of an npn transistor at (a) 25°C (b) 100°C. Note the change in Q-point.

5.6 SELF BIAS OR EMITTER BIAS

The fixed bias circuit of Fig. 5.4(a) as we have seen does not provide a stable operating point when temperature changes or the transistor is replaced. The reason for instability is that the base current I_B is fixed in the circuit whereas I_C and V_{CE} vary. Thus, in order to get a stable operating point, we must have a biasing circuit in which I_C and V_{CE} are maintained constant whereas I_B is allowed to vary. A circuit that fulfills this requirement is a self bias or emitter bias circuit and is shown in Fig. 5.9(a).

In this circuit, the base voltage is obtained from the supply V_{CC} through the voltage divider R_1 and R_2. The resistance R_E in the emitter branch helps in stabilizing the Q-point.

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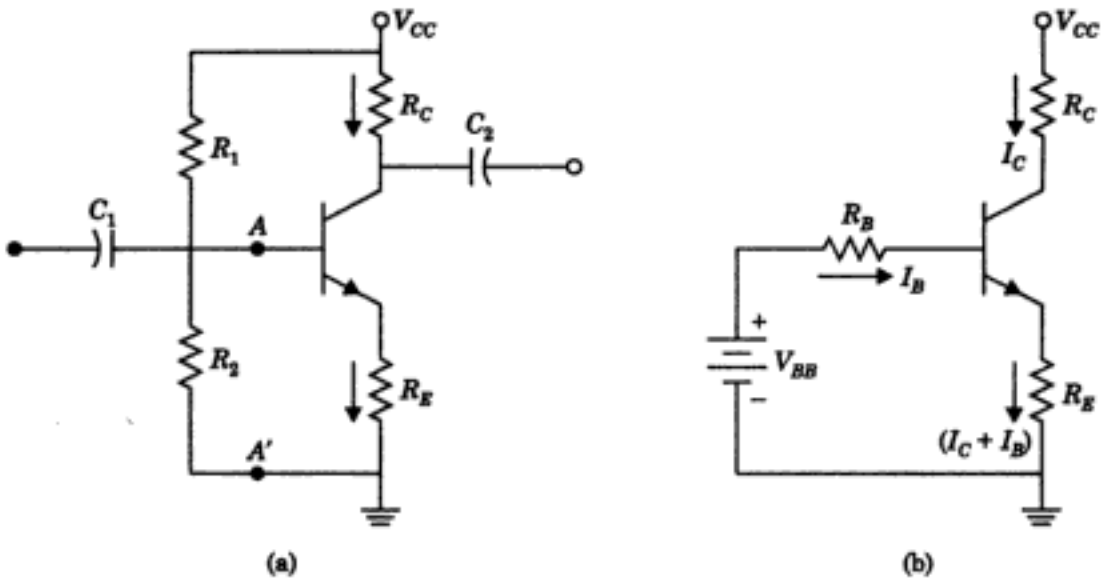


Fig. 5.9 (a) A CE amplifier with self bias, (b) Simplified circuit obtained by applying Thevenin's at AA'.

Analysis: The circuit of Fig. 5.9(a) can be simplified by replacing the voltage divider R_1R_2 network by its Thevenin's equivalent applied at AA'. The simplified circuit so obtained is shown in Fig. 5.9(b) where

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \tag{5.3}$$

and

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \quad (\text{or } R_1 \parallel R_2) \tag{5.4}$$

It may be noted that the capacitors C_1 and C_2 are open circuit under dc conditions. The Q-point analysis of this circuit can be done either (i) analytically (ii) graphically. Both the methods are discussed here.

Analytical method for finding Q-point: The value of β_F must be known in this method. The quiescent base current I_B is determined by applying KVL in the base loop of Fig. 5.9(b):

$$V_{BB} - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0 \tag{5.5}$$

Since $I_C \simeq \beta_F I_B$ in the active region (neglecting I_{CO}), we may write Eq. (5.5) as:

$$V_{BB} = I_B R_B + V_{BE} + (1 + \beta_F) I_B R_E \tag{5.6}$$

Thus,

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (1 + \beta_F) R_E} \tag{5.7}$$

and

$$I_C \simeq \beta_F I_B \tag{5.8}$$

The value of V_{CE} is calculated by writing KVL for the collector loop in Fig. 5.9(b).

$$V_{CC} - I_C R_C - V_{CE} - (I_C + I_B)\, R_E = 0 \tag{5.9}$$

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The value of I_C and I_B has already been calculated, so V_{CE} can be computed from Eq. (5.9).

Graphical method for finding Q-point: The Q-point can be computed graphically on the volt-ampere characteristics of the transistor as shown in Fig. 5.10.

Eliminating I_C from Eqs. (5.5) and (5.9), we obtain

$$V_{BB} = I_B R_B + V_{BE} + R_E I_B + \frac{R_E V_{CC}}{R_E + R_C} - \frac{R_E V_{CE}}{R_E + R_C} \tag{5.10}$$

For each value of I_B on the output characteristics, the value of V_{CE} is computed from Eq. (5.10). The locus of (V_{CE}, I_B) plotted on the CE output characteristics is called the **bias curve** and is shown in Fig. 5.10. The point of intersection of the bias curve with the load line gives the Q-point.

The analytical method is obviously simpler and more popular as value of β_F is usually available for the transistors.

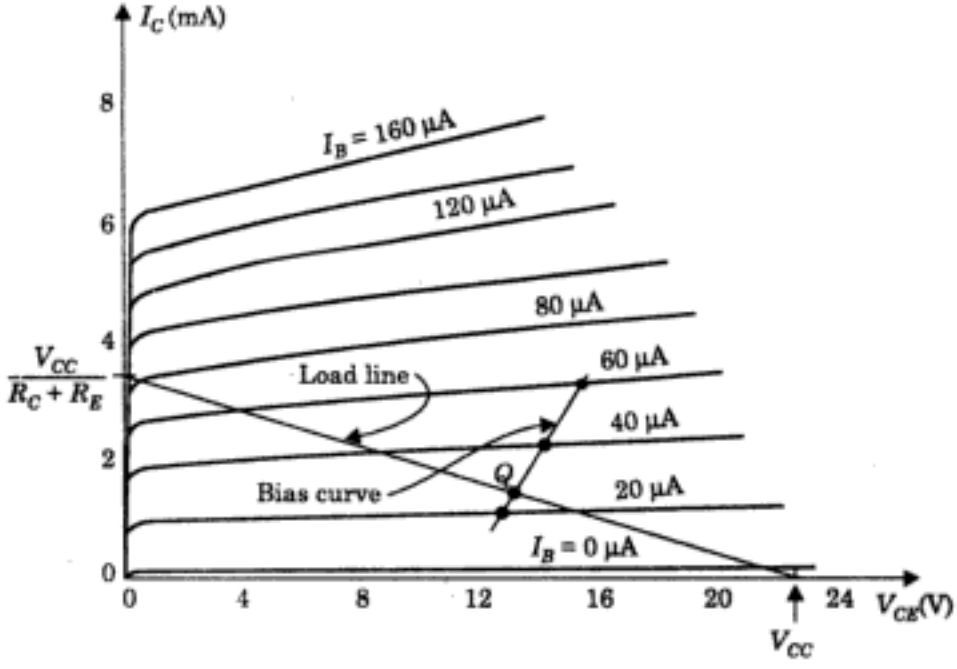


Fig. 5.10 Finding Q-point graphically.

Importance of emitter resistance R_E: The emitter resistance R_E stabilizes the collector current I_C by providing negative feedback in the base emitter circuit. If the collector current, I_C increases due to increase in temperature or due to replacement of device with higher β_F, the voltage drop V_E across R_E also increases. This in turn reduces the base to emitter voltage. The base emitter junction is, therefore, less forward biased and, therefore, reduces the collector current I_C. Thus, any tendency of I_C to increase is nullified by the negative feedback action provided by the emitter resistance R_E. The resistance R_E, therefore, stabilizes the Q-point against variations in the collector current due to change of temperature or device.

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Design constraints: The aim of the self bias circuit is to make collector current I_C insensitive to the variation in temperature or β. This is achieved by imposing the following two constraints in the self bias circuit:

$$V_{BB} >> V_{BE} \tag{5.11}$$

and

$$(1 + \beta_F)R_E >> R_B \tag{5.12}$$

It can be seen that when these two constraints are applied to Eq. (5.7), it reduces to

$$I_B \simeq \frac{V_{BB}}{(1 + \beta_F)R_E} \tag{5.13}$$

For very large β_F,

$$I_B \simeq \frac{V_{BB}}{\beta_F R_E} \tag{5.14}$$

and

$$I_C \simeq \beta_F I_B$$

$$\simeq \frac{V_{BB}}{R_E} \tag{5.15}$$

Thus we can say that, I_C has becomes independent of transistor parameters and is stabilized.

In Fig. 5.9(b), for a given supply voltage V_{CC}, higher the value of V_{BB}, lower will be the sum of voltage across R_C and the collector base junction V_{CB}. We, however desire large voltage across R_C so as to get high voltage gain. We also require large V_{CB} (or V_{CE}) to provide large signal swing. These conflicting requirements are usually compromised by choosing voltage at the base V_B or V_{BB} (neglecting drop across R_B due to I_B) about $1/3V_{CC}$, V_{CB} (or V_{CE}) about $1/3V_{CC}$ and drop $I_C R_C$ across R_C about $1/3V_{CC}$.

In accordance with the second constraint given in (Eq. 5.12), we must choose R_1 and R_2 small so as to keep R_B small. However, if R_1 and R_2 are small, more current will be drawn from the collector supply V_{CC}. Lower values of R_1 and R_2 will also reduce the input resistance of the amplifier which is not a desirable feature. There is again a trade-off involved in this part of design aspect. It can be, however, seen that the current through the divider must be made much larger than the base current. For this, one selects R_1 and R_2 such that the current through R_1R_2 lies in the range of I_E ($\simeq I_C$) to $0.1I_E$ ($\simeq 0.1I_C$).

EXAMPLE 5.2

Determine the Q-point, i.e., V_{CEQ} and I_{CQ} for the self-biased CE amplifier shown in Fig. 5.11(a). Assume $V_{BE} = 0.7$ V and $\beta_F = 50$.

Solution Figure 5.11(b) shows the simplified circuit obtained by using Thevenin's equivalent representation of potential divider RR. Under dc conditions

$$V_{BB} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$= \frac{22 \times 18}{82 + 22} = 3.81 \text{ V}$$

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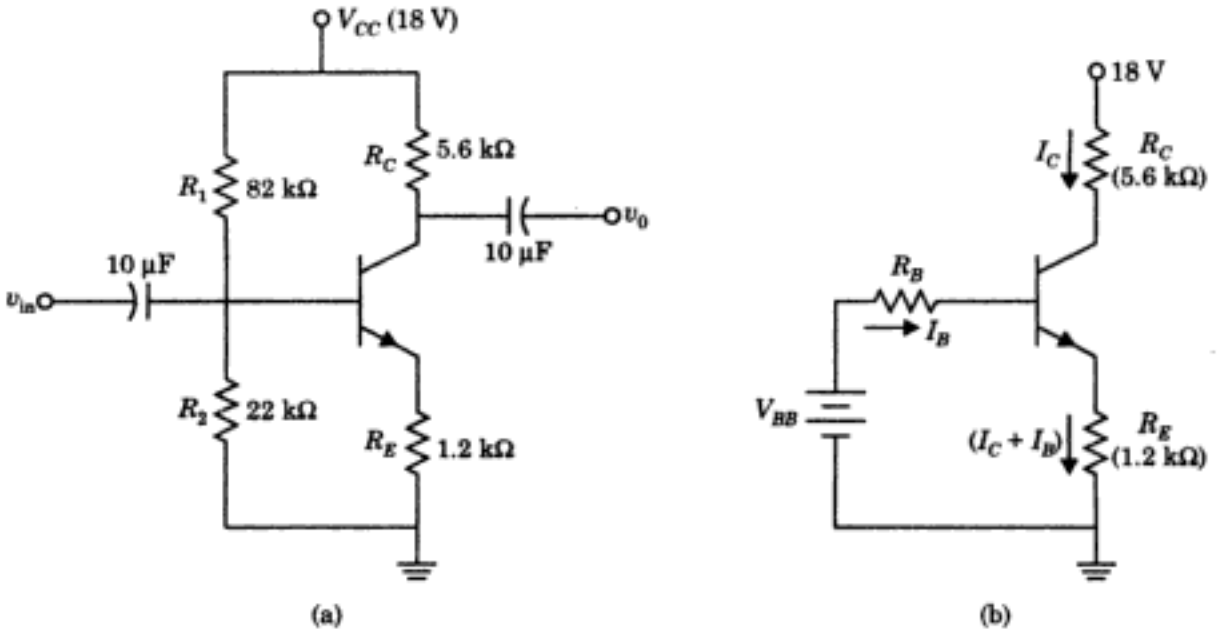


Fig. 5.11 (a) Self-biased CE amplifier for Ex. 5.2, (b) Simplified circuit.

From Eq. (5.4),

$$R_B = R_1 \parallel R_2$$
$$= 82 \parallel 22$$
$$= 17.35 \text{ k}\Omega$$

Also from Eq. (5.7),

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (1 + \beta_F)R_E}$$

$$= \frac{3.81 - 0.7}{17.35 + (51)(1.2)} = 39.6 \text{ μA}$$

and

$$I_C = \beta_F I_B$$
$$= (50)(39.6) = 1.98 \text{ mA}$$

From Eq. (5.9),

$$V_{CE} = V_{CC} - I_C(R_C + R_E) - I_B R_E$$
$$= 18 - (1.98)(5.6 + 1.2) - (39.6)(1.2)$$
$$= 4.49 \text{ V}$$

So

$$\left.\begin{aligned} V_{CEQ} &= 4.49 \text{ V} \\ I_{CQ} &= 1.98 \text{ mA} \end{aligned}\right\} \textbf{ Ans.}$$

EXAMPLE 5.3

Design a self biased circuit to establish the Q-point at $I_C = 1$ mA using a collector supply $V_{CC} = +12$ V. Assume $\beta_F = 100$, $V_{BE} = 0.7$ V.

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Solution Consider the self bias circuit shown in Fig. 5.12.

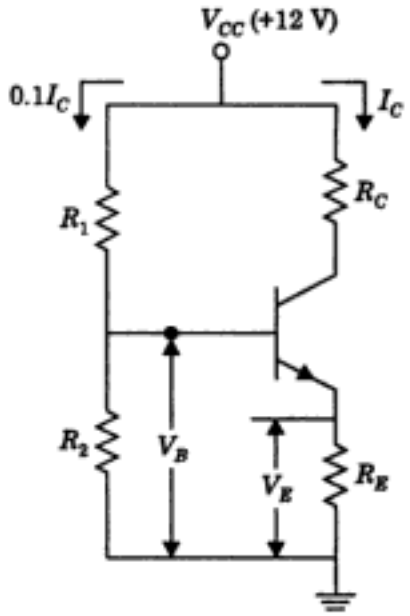


Fig. 5.12 Self bias circuit for Example 5.3.

As suggested in the design constraints, allocate $1/3V_{CC}$ to R_C, another $1/3V_{CC}$ to R_2 leaving $1/3V_{CC}$ for V_{CEQ}.

Thus, $V_B = 4$ V

and $V_E = V_B - V_{BE}$

$= 4 \text{ V} - 0.7 \text{ V} = 3.3 \text{ V}$

Neglecting base current,

$$V_E \doteq I_C R_E$$

Therefore, $$R_E = \frac{V_E}{I_C}$$

$$= \frac{3.3}{1} = 3.3 \text{ k}\Omega$$

Select the current through R_1R_2 equal to $0.1I_C$, i.e., 0.1 mA.

Since $V_{CC} = (R_1 + R_2)(0.1 \text{ mA})$ (I_B has been neglected)

Therefore, $$R_1 + R_2 = \frac{12}{0.1} = 120 \text{ k}\Omega$$

Also $$V_B = 4 \text{ V} = \frac{R_2}{R_1 + R_2} \cdot V_{CC}$$

Solving for R_1 and R_2 gives

$$R_1 = 80 \text{ k}\Omega$$

$$R_2 = 40 \text{ k}\Omega$$

The value of R_C is determined from:

$$I_C R_C = \frac{1}{3} V_{CC} = 4 \text{ V}$$

$\therefore$ $$R_C = \frac{4}{1} = 4 \text{ k}\Omega$$

Thus, $R_1 = 80$ kΩ, $R_2 = 40$ kΩ, $R_C = 4$ kΩ and $R_E = 3.3$ kΩ **Ans.**

If, however, we assume that the current through R_1R_2 is equal to I_C, i.e., 1 mA then $R_1 + R_2 = 12$ KΩ and the new values of R_1 and R_2 are found as: $R_1 = 8$ kΩ, $R_2 = 4$ kΩ.

An improved bias arrangement: Figure 5.13 shows a collector to base bias circuit which provides better stability against β_F variation compared to fixed bias or self bias configurations.

Writing KVL around the indicated loop, we obtain

$$V_{CC} = R_C(I_C + I_B) + I_B R_B + V_{BE} + (I_C + I_B)R_E \quad (5.16)$$

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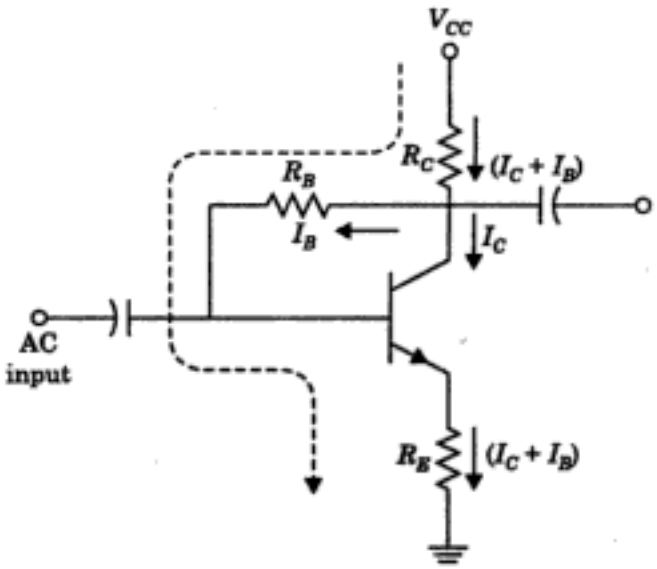


Fig. 5.13 An improved bias arrangement (collector to base bias circuit).

Also $$I_C \simeq \beta_F I_B$$

Solving for I_B yields

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta_F)(R_C + R_E)} \tag{5.17}$$

The quiescent collector current I_{CQ} is obtained by using $I_C \simeq \beta_F I_B$

Thus $$I_{CQ} = \frac{\beta_F (V_{CC} - V_{BE})}{R_B + (1 + \beta_F)(R_C + R_E)} \tag{5.18}$$

$$\simeq \frac{\beta_F (V_{CC} - V_{BE})}{R_B + \beta(R_C + R_E)} \tag{5.19}$$

In general, $\beta_F(R_C + R_E) >> R_B$ ($\because$ of large β_F)

Therefore, $$I_{CQ} \simeq \frac{V_{CC} - V_{BE}}{R_C + R_E} \tag{5.20}$$

The value of V_{CEQ} can be obtained by writing KVL equation for the collector loop.

Now, let us compare the stability of this circuit with that of fixed bias and self bias configurations. For this, rewrite the equation for I_C obtained for all the three configurations

Fixed bias circuit: $$I_C = \frac{\beta_F (V_{CC} - V_{BE})}{R_B} \tag{5.21}$$

Self bias circuit: $$I_C = \frac{\beta_F (V_{BB} - V_{BE})}{R_B + (1 + \beta_F) R_E} \tag{5.22}$$

Improved circuit: (Collector to base bias)

$$I_C = \frac{\beta_F (V_{CC} - V_{BE})}{R_B + \beta_F (R_C + R_E)} \tag{5.23}$$

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It is easily seen from Eq. (5.21) of fixed bias circuit that the collector current I_C is highly sensitive to variations in β_F. Comparing Eq. (5.22) and (5.23), it can be seen that the denominator in Eq. (5.23) will always be more than that in Eq. (5.22). Hence the collector to base bias circuit provides better stability against variations in β_F.

EXAMPLE 5.4

Find V_{CEQ} and I_{CQ} for the amplifier circuit shown in Fig. 5.14. Assume $\beta_F = 45$.

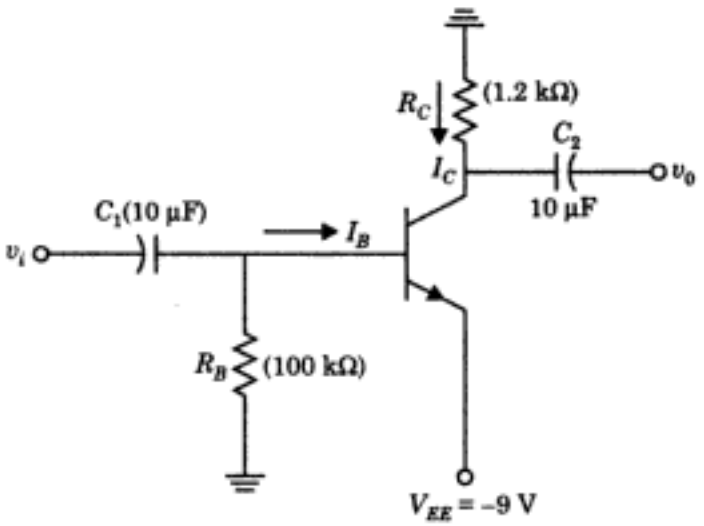


Fig. 5.14 Circuit for Example 5.4.

Solution Applying KVL in the clockwise direction base emitter loop (capacitors C_1 and C_2 are open circuit under dc conditions)

$$-I_B R_B - V_{BE} + V_{EE} = 0$$

$$\therefore \quad I_B = \frac{V_{EE} - V_{BE}}{R_B}$$

$$= \frac{9 - 0.7}{100} = 83\ \mu A$$

and $$I_C \simeq \beta I_B$$

$$= (45)(83) = 3.735\ mA$$

Writing KVL for the collector loop, we have

$$-I_C R_C - V_{CE} + V_{EE} = 0$$

or $$V_{CE} = V_{EE} - I_C R_C$$

$$= 9 - (3.735)\ (1.2)$$

$$= 4.52\ V$$

So $$\left.\begin{aligned} I_{CQ} &= 3.735\ mA \\ V_{CEQ} &= 4.52\ V \end{aligned}\right\}$$ **Ans.**

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EXAMPLE 5.5

Determine the Q-point for the circuit shown in Fig. 5.15. Assume $\beta_F = 120$.

Solution Note there are two supplies V_{CC} and V_{EE} in this circuit. The Thevenin's equivalent voltage V_{BB} and equivalent resistance R_B at the base terminal is determined from the part of the circuit shown in Fig. 5.16(a).

Here $R_B = R_1 \parallel R_2$

$= (8.2) \parallel (2.2)$

$= 1.73\ \text{k}\Omega$

In Fig. 5.16(a),

$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2}$$

$$= \frac{20 + 20}{(8.2 + 2.2)} = \frac{40}{10.4}$$

$= 3.85\ \text{mA}$

So $V_{BB} = IR_2 - V_{EE}$

$= (3.85)(2.2) - 20 = -11.53\ \text{V}$

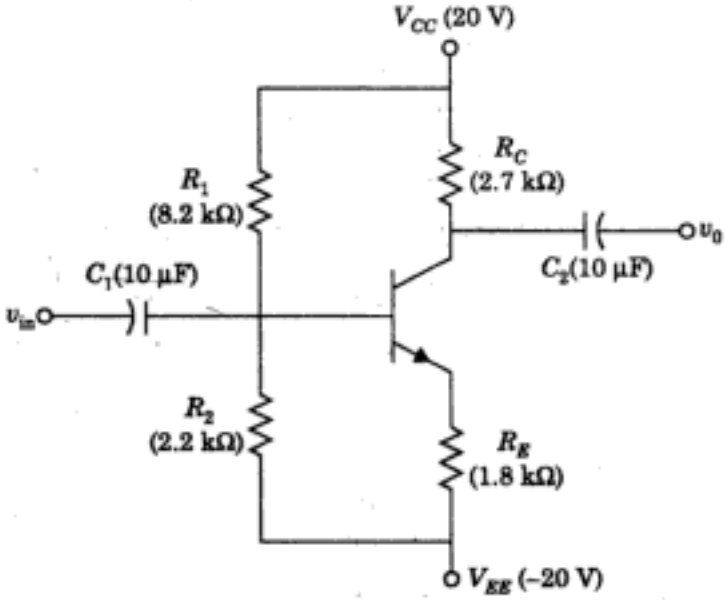


Fig. 5.15 Circuit for Example 5.5.

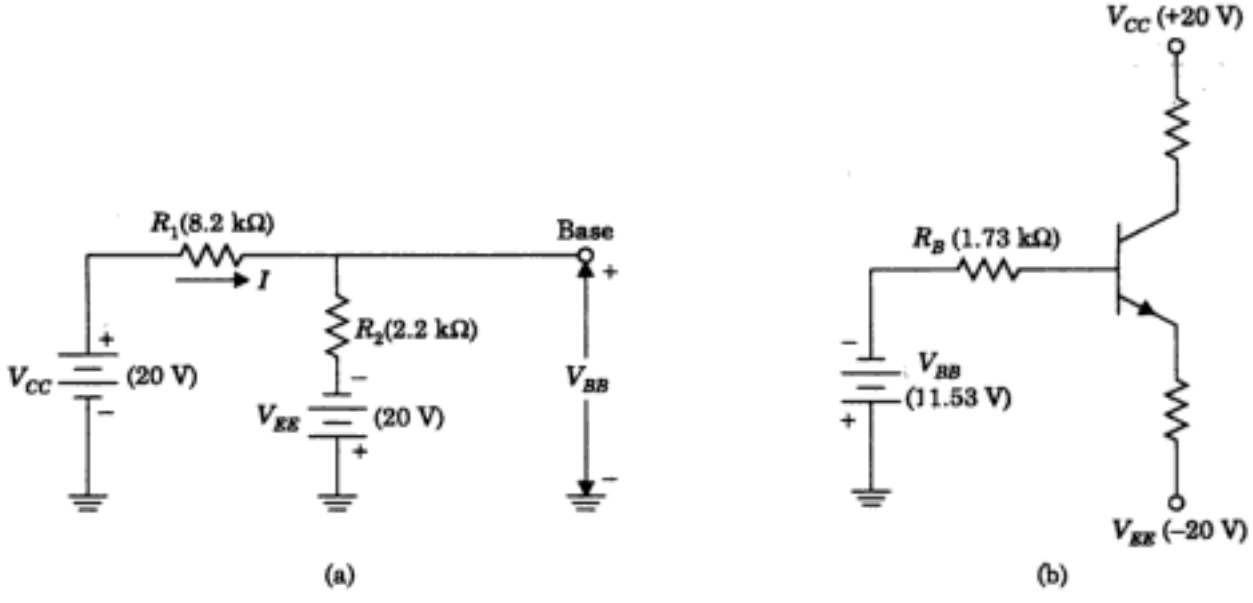


Fig. 5.16 (a) Circuit for determining V_{BB} and R_B (b) Simplified circuit for Example 5.5.

The simplified complete circuit is shown in Fig. 5.16(b). Writing KVL for the base emitter loop gives

$$-V_{BB} - I_B R_B - V_{BE} - (I_C + I_B)R_E + V_{EE} = 0$$

and

$$I_C = \beta_F I_B$$

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Therefore,
$$I_B = \frac{V_{EE} - V_{BB} - V_{BE}}{R_B + (1+\beta_F)R_E}$$
$$= \frac{20 - 11.53 - 0.7}{1.73 + (121)(1.8)}$$
$$= \frac{7.77}{219.53} = 35.39\ \mu A$$

and
$$I_C = \beta I_B$$
$$= (120)(35.39) = 4.25\ mA$$

KVL for the collector loop gives
$$V_{CC} - I_C R_C - V_{CE} - (I_C + I_B)R_E + V_{EE} = 0$$

or
$$V_{CE} = V_{CC} + V_{EE} - I_C(R_C + R_E) - I_B R_E$$
$$= 20 + 2.0 - (4.25)(4.5) - (35.39)(1.8)$$
$$= 20.812\ V$$

$\therefore$ $V_{CEQ} = 20.812\ V$

and $I_{CQ} = 4.25\ mA$ **Ans.**

EXAMPLE 5.6

For the circuit shown in Fig. 5.17, determine R_F so that $I_E = +2$ mA. Assume $\beta_F = 49$.

Solution The current I_1 through R_B is:
$$I_1 = \frac{V_{BE}}{R_B}$$
$$= \frac{0.7}{25} = 28\ \mu A$$

Also
$$I_E = I_C + I_B$$
$$= (1 + \beta_F)I_B$$

Therefore,
$$I_B = \frac{I_E}{1+\beta_F}$$
$$= \frac{2}{1+49} = 40\ \mu A$$

KVL for the indicated loop gives
$$V_{CC} - R_C(I_1 + I_B + I_C) - R_F(I_1 + I_B) - V_{BE} = 0$$

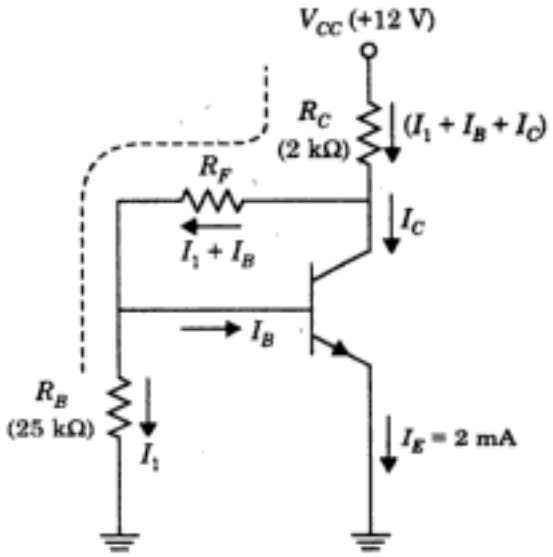


Fig. 5.17 Circuit for Example 5.6.

Solving for R_F gives
$$R_F = \frac{V_{CC} - R_C(I_1 + I_B + I_C) - V_{BE}}{I_1 + I_B} \qquad (I_1 R_B = V_{BE})$$
$$= \frac{V_{CC} - R_C(I_1 + (1+\beta_F)I_B) - V_{BE}}{I_1 + I_B}$$

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$$= \frac{12 - 2(28 + 50 \times 40) - 0.7}{28 + 40}$$

$$= 106.5 \text{ k}\Omega$$

$$R_F = 106.5 \text{ k}\Omega \quad \textbf{Ans.}$$

EXAMPLE 5.7

The circuit in Fig. 5.18 has to be designed to make $V_0 = 0$ V and $V_{CEQ} = 3$ V. Determine R_C and R_E. Assume $\beta = 200$.

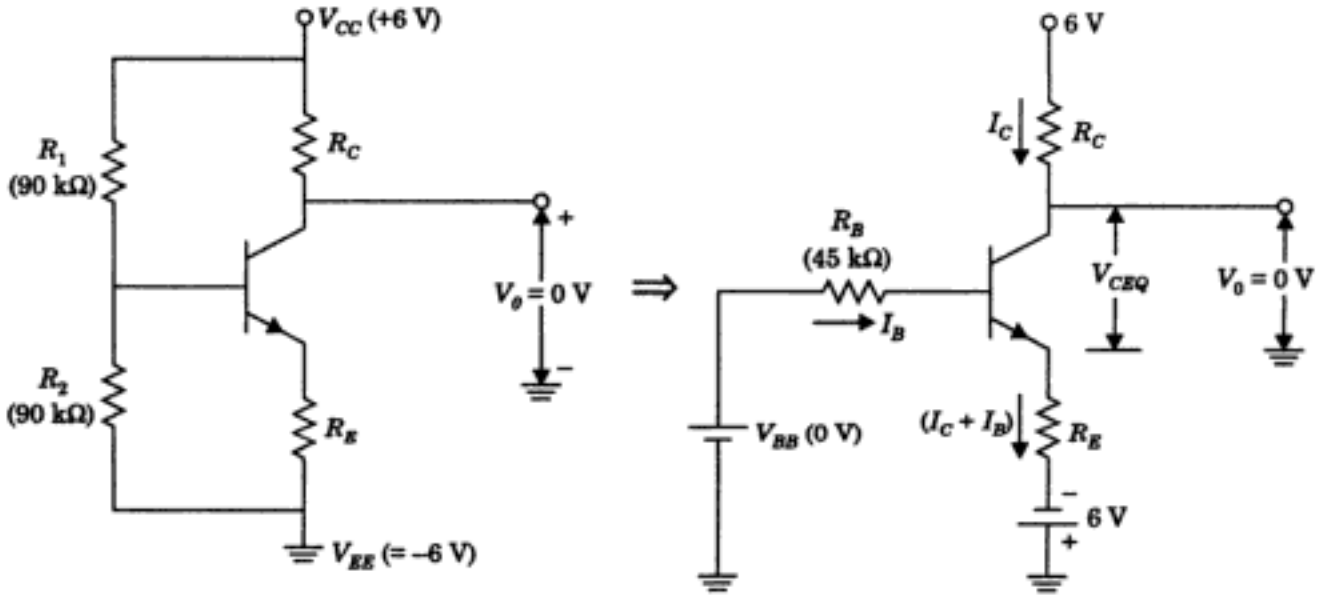


Fig. 5.18 (a) Circuit for Example 5.7, (b) Simplified circuit.

Solution The simplified circuit by replacing the voltage divider network using Thevenin's equivalent is shown in Fig. 5.18(b).

It can be seen

$$R_B = R_1 \parallel R_2$$

$$= \frac{(90)(90)}{90 + 90} = 45 \text{ k}\Omega$$

$$V_{BB} = \frac{R_2(V_{CC} + V_{EE})}{R_1 + R_2} - V_{EE}$$

$$= \frac{(90)(12)}{180} - 6 = 0 \text{ V}$$

Applying KVL in the base emitter loop,

$$I_B R_B + V_{BE} + (I_C + I_B)R_E - 6 = 0 \tag{5.24}$$

In the output loop, we can write

$$-V_{CEQ} - (I_C + I_B)R_E + 6 = 0 \tag{5.25}$$

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So $(I_C + I_B)R_E = 6 - 3 = 3$ V

Now, from Eq. (5.24), we get

$$I_B = \frac{6 - V_{BE} - (I_C + I_B)R_E}{R_B}$$

or
$$I_B = \frac{6 - 0.7 - 3}{45}$$
$$= 51.1\ \mu A$$

and
$$I_C = \beta I_B$$
$$= (200)(51.1)$$
$$= 10.2\ mA$$

Also in the output loop,

$$6 - I_C R_C = 0$$

So
$$R_C = \frac{6}{I_C}$$
$$= \frac{6}{10.2} = 0.588\ k\Omega$$

The value of R_E can be calculated as:

$$(I_C + I_B)R_E = 3\ V$$

$$R_E = \frac{3}{(10.2 + 51.1)} = 0.292\ k\Omega.$$

$$\left.\begin{aligned} R_C &= 0.588\ k\Omega \\ R_E &= 0.291\ k\Omega \end{aligned}\right] \quad \textbf{Ans.}$$

EXAMPLE 5.8

The amplifier circuit shown in Fig. 5.19(a) uses a pnp transistor. Determine V_{CEQ}. Assume $\beta_F = 120$, $V_{BE} = -0.7$ V.

Solution First find Thevenin's equivalent voltage, V_{BB} and resistance R_B:

$$V_{BB} = \frac{R_2 V_{CC}}{R_1 + R_2}$$
$$= \frac{(10)(-18)}{47 + 10}$$
$$= -3.16\ V$$

and
$$R_B = R_1 \parallel R_2$$
$$\frac{(47)(10)}{47 + 10} = 8.24\ k\Omega$$

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Applying KVL in the base emitter loop in the simplified circuit shown in Fig. 5.19(b).

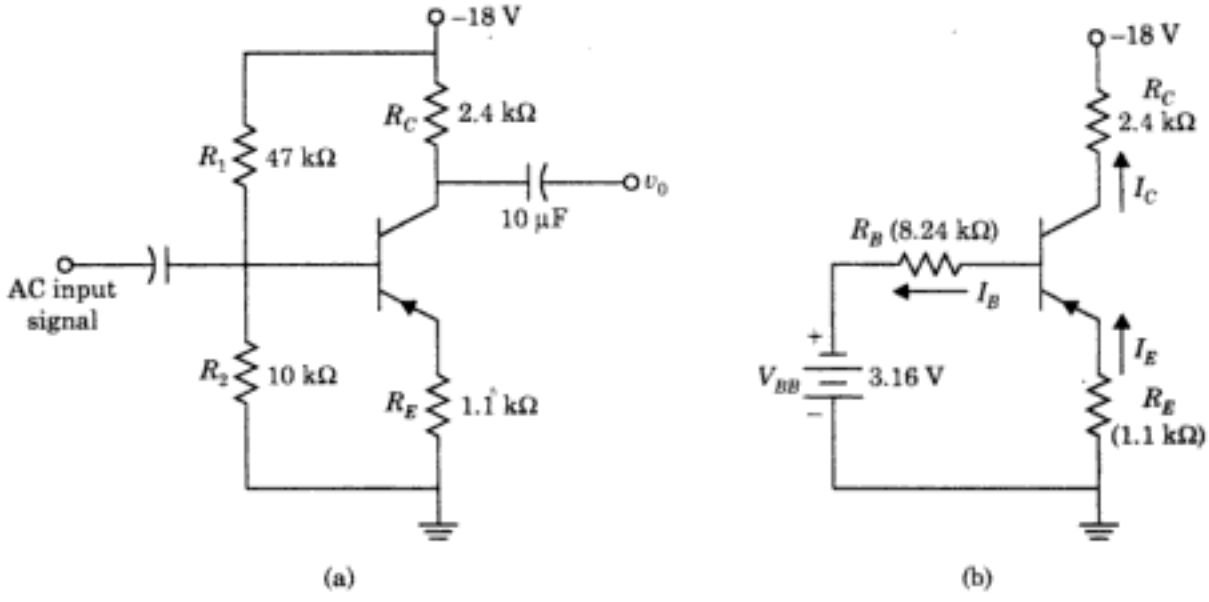


Fig. 5.19 (a) Circuit for Example 5.8 and (b) Simplified circuit.

$$-I_E R_E + V_{BE} - I_B R_B + V_{BB} = 0$$

or $$-(1 + \beta_F) I_B R_E + V_{BE} - I_B R_B + V_{BB} = 0$$

Solving for I_B,

$$I_B = \frac{V_{BB} + V_{BE}}{R_B + (1 + \beta_F) R_E}$$

$$= \frac{3.16 - 0.7}{8.24 + (121)(1.1)}$$

$$= 0.0174 \text{ mA}$$

and $$I_C \simeq \beta I_B$$

$$= (120)(0.0174) = 2.08 \text{ mA}$$

In the collector emitter loop,

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

or $$V_{CE} = -V_{CC} + I_C(R_C + R_E) + I_B R_E \quad (\because \; I_E = I_C + I_B)$$

$$= -18 + (2.08)\,(3.5) + (0.0174)(1.1)$$

$$= -10.7 \text{ V}$$

$\therefore$ $$V_{CEQ} = -10.7 \text{ V}$$ **Ans.**

5.7 STABILITY FACTORS $S(I_{CO})$, $S(V_{BE})$ AND $S(\beta)$

In Section 5.5, we have seen that the operating point drifts due to (i) increase in I_{CO} with increase in temperature (ii) decrease in V_{BE} with increase in temperature, (iii) the variation

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in β due to change of temperature or change of device. A bias circuit that is less sensitive to temperature variations is definitely preferred. The sensitivity of a circuit to variations with its parameters is usually measured in terms of stability factors. A stability factor S is defined for each of the parameters affecting bias stability as:

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

These stability factors* give the change in the collector current due to changes in I_{CO}, V_{BE} and β respectively. It is evident that a circuit which is relatively insensitive to temperature variations will have low stability factors.

We now analyze stability factors for the various bias configurations discussed earlier.

Stability factor $S(I_{CO})$: The stability factor $S(I_{CO})$ is the rate of change of I_C with reverse saturation current I_{CO}, keeping the other two parameters V_{BE} and β constant. Thus,

$$S(I_{CO}) = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\beta=\text{constant}} = \frac{\Delta I_C}{\Delta I_{CO}} \tag{5.26}$$

A simple mathematical expression can be found for $S(I_{CO})$. For a transistor biased in the active region, we know that

$$I_C = \beta I_B + (1 + \beta) I_{CO}^{**} \tag{5.27}$$

Taking partial derivative w.r.t. I_C and assuming β constant,

$$1 = \beta \frac{dI_B}{dI_C} + (1 + \beta) \frac{dI_{CO}}{dI_C} \tag{5.28}$$

$$1 = \beta \frac{dI_B}{dI_C} + (1 + \beta) \frac{1}{S(I_{CO})}$$

---

*In the literature, stability S_B^A is usually defined as:

$$S_B^A = \frac{\Delta A/A}{\Delta B/B}$$

is the ratio of relative variation in parameter A to the relative variation in parameter B. In our discussion, however, we have defined the ratio of variation in parameter A when parameter B varies. It is so, since we are concerned with the Q-point obtained from:

$$V_{CEQ} = V_{CC} - I_{CQ} R_C$$

and we require absolute values (and not relative values) for Q-point parameter calculations.

**There is no difference in β_F and β, as used here, and these are used interchangeably.

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Therefore,
$$S(I_{CO}) = \frac{1+\beta}{1-\beta\dfrac{dI_B}{dI_C}} \tag{5.29}$$

The value of differential $\frac{dI_B}{dI_C}$ in Eq. (5.29) depends upon the biasing configuration. Equation (5.29) thus provides an alternative expression for finding $S(I_{CO})$ of a given circuit.

Fixed-bias

For the fixed bias circuit shown in Fig. 5.4,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{5.30}$$

From Eq. (5.30), it can be seen that the current I_B is independent of I_C, hence $\frac{dI_B}{dI_C}$ is zero.

Putting the value of $\frac{dI_B}{dI_C} = 0$ in Eq. (5.29), we obtain,
$$S(I_{CO}) = 1 + \beta \tag{5.31}$$

If the value of β is 100, $S(I_{CO}) = 101$ which is quite large. The fixed bias circuit, therefore, has very poor thermal stability.

Self bias circuit

Rewriting Eq. (5.5) for the base loop of self bias circuit shown in Fig. 5.9(b),
$$V_{BB} = I_B R_B + V_{BE} + (I_C + I_B)R_E \tag{5.32}$$

Differentiating Eq. (5.32) w.r.t. I_C and assuming V_{BE} constant, we have
$$0 = R_B\frac{dI_B}{dI_C} + R_E\left(1 + \frac{dI_B}{dI_C}\right) \tag{5.33}$$

So
$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_E + R_B} \tag{5.34}$$

Substituting the value of $\frac{dI_B}{dI_C}$ in Eq. (5.29), we obtain
$$S(I_{CO}) = \frac{(1+\beta)}{1+\beta\dfrac{R_E}{R_E + R_B}} \tag{5.35}$$

$$= (1+\beta)\frac{R_E + R_B}{(1+\beta)R_E + R_B}$$

$$= (1+\beta)\frac{1 + R_B/R_E}{1 + \beta + R_B/R_E} \tag{5.36}$$

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For $$\frac{R_B}{R_E} << 1,$$

$$S(I_{CO}) \approx 1$$

The value of the stability factor $S(I_{CO})$ increases with the increase of ratio R_B/R_E and becomes $(1 + \beta)$ as $R_B/R_E \to \infty$. Typical variation of stability factor $S(I_{CO})$ with the resistance ratio R_B/R_E is shown in Fig. 5.20.

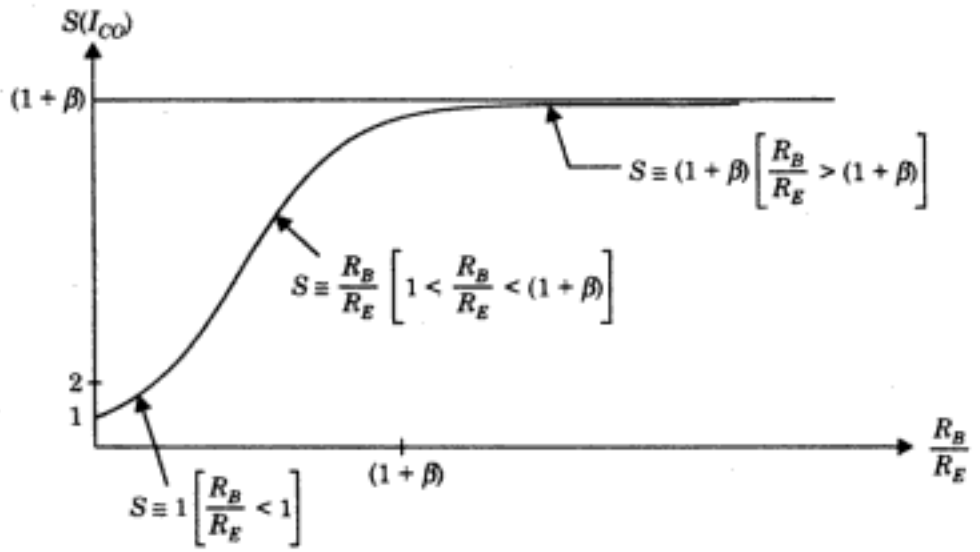


Fig. 5.20 Variation of stability factor $S(I_{CO})$ with the resistor ratio R_B/R_E for the self bias configuration.

Stability factor $S(V_{BE})$

The variation of I_C with V_{BE} is given by the stability factor $S(V_{BE})$ and is defined by

$$S(V_{BE}) = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\beta=\text{constant}} = \frac{\Delta I_C}{\Delta V_{BE}} \tag{5.37}$$

where both I_{CO} and β are considered constant.

Fixed-bias

For the fixed bias circuit,

$$I_C = \beta \frac{V_{CC} - V_{BE}}{R_B} \tag{5.38}$$

Therefore, $$S(V_{BE}) = \frac{dI_C}{dV_{BE}} = \frac{-\beta}{R_B} \tag{5.39}$$

Self-bias

It is seen that for self bias circuit

$$I_C = \beta \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta)R_E} \tag{5.40}$$

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Thus,
$$S(V_{BE}) = \frac{dI_C}{dV_{BE}}$$

$$= \frac{-\beta}{R_B + (1+\beta)R_E} \tag{5.41}$$

$$= \frac{-\beta/R_E}{R_B/R_E + (1+\beta)} \tag{5.42}$$

If $(1 + \beta) >> \frac{R_B}{R_E}$ and $\beta >> 1$, then

$$S(V_{BE}) = \frac{-\beta/R_E}{1+\beta} \simeq -\frac{1}{R_E} \tag{5.43}$$

Better stability can be achieved by keeping the emitter resistance R_E high.

Stability factor S(β)

The stability factor $S(\beta)$ is defined as:

$$S(\beta) = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO}, \beta = \text{constant}} = \frac{\Delta I_C}{\Delta \beta} \tag{5.44}$$

The mathematical derivation of $S(\beta)$ is quite complex compared to that for $S(I_{CO})$ and $S(V_{BE})$. The derivation, therefore, is not included in the text. The result, however, for the more commonly used self bias configuration is:

$$S(\beta) = \frac{I_{C1}(1 + R_B/R_E)}{\beta_1(1 + \beta_2 + R_B/R_E)} \tag{5.45}$$

Here, I_{C1} and β_1 define the parameters at the original condition and β_2 is the new value of beta. Equation (5.45) is also expressed as:

$$S(\beta) = \frac{I_{C1}S'(I_{CO})}{\beta_1(1 + \beta_2)} \tag{5.46}$$

where $S'(I_{CO})$ is the value of $S(I_{CO})$ at $\beta = \beta_2$. Using Eq. (5.36), we get

$$S'(I_{CO}) = (1 + \beta_2)\frac{1 + R_B/R_E}{1 + \beta_2 + R_B/R_E} \tag{5.47}$$

Cumulative effect of I_{CO}, V_{BE} and β on the operating point stability

Stability factors $S(I_{CO})$, $S(V_{BE})$ and $S(\beta)$ were defined in Section 5.7 as partial derivatives of the collector current I_C w.r.t. I_{CO}, V_{BE} and β, respectively. Each of the partial derivatives were calculated with the other two parameters assumed constant. In a practical situation, however, it is more important to compute the total change in the collector current due to changes in all the three variable quantities I_{CO}, V_{EB} and β over a specified temperature change. Thus, by taking the total differential of

$$I_C = f(I_{CO}, V_{BE}, \beta) \tag{5.48}$$

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We may write

$$\Delta I_C = \frac{\partial I_C}{\partial I_{CO}} \Delta I_{CO} + \frac{\partial I_C}{\partial V_{BE}} \Delta V_{BE} + \frac{\partial I_C}{\partial \beta} \Delta\beta \tag{5.49}$$

$$= S(I_{CO})\Delta I_{CO} + S(V_{BE})\Delta V_{BE} + S(\beta)\Delta\beta \tag{5.50}$$

This equation appears to be complex, but it may be noted that each component is simply the stability factor for the given configuration multiplied by the change in the parameter between the temperature limits of interest.

Many circuits for commercial applications are required to operate from 0° to 70°C and those used in aerospace, automatic and military applications must operate from –55°C to between 100°C and 150°C. Manufacturers provide device data for the range –65°C to 175°C to accomodate wide variety of applications. Table 5.1 shows the changes in I_{CO}, V_{BE} and β with increase in temperature for a typical silicon transistor.

Table 5.1 Variation of Silicon Transistor Parameters with Temperature

T°C	I_{CO}(nA)	V_{BE}(V)	β
–65	0.2×10^{-3}	0.85	20
25	0.1	0.65	50
100	20	0.48	80
175	3.3×10^{3}	0.30	120

We now take a few examples to illustrate how to compute the total change in the collector current due to changes in the three parameters I_{CO}, V_{BE} and β over a specified temperature range.

EXAMPLE 5.9

For the circuit shown in Fig. 5.21, a silicon transistor with $\beta = 50$ at 25°C is used and it is desired that $V_{CE} = 5$ V. Determine (i) R_B (ii) the stability factor $S(I_{CO})$ (iii) the value of I_C at 100°C.

Solution Applying KVL to the collector emitter circuit,

(i) $24 = 10\,(I_C + I_B) + V_{CE} + 0.5\,(I_C + I_B)$

$= 10.5\,(1 + \beta)I_B + 5$

So $I_B = \dfrac{24 - 5}{10.5\,(51)} = 0.035$ mA

and $I_C = 50 I_B$

$= (50)(0.035) = 1.75$ mA

Also,

$V_{CE} = I_B R_B + V_{BE}$

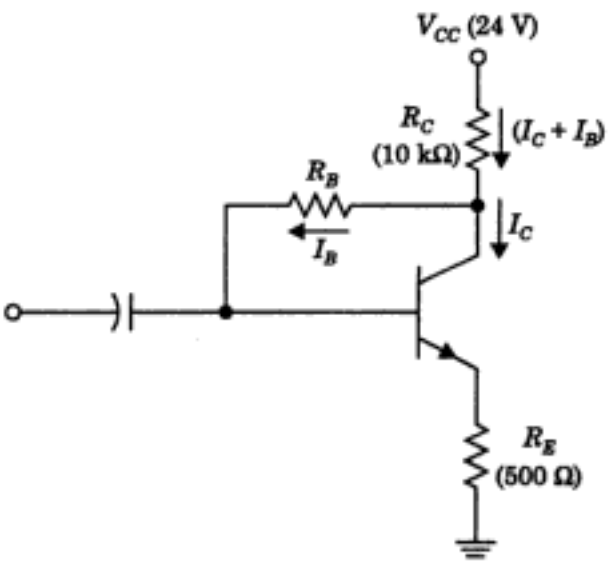


Fig. 5.21 Circuit for Example 5.9.

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So
$$R_B = \frac{V_{CE} - V_{BE}}{I_B}$$
$$= \frac{5 - 0.7}{0.035} = 122.8 \text{ k}\Omega$$

(ii) Note that it is the improved collector to base bias circuit discussed earlier. The expression of $S(I_{CO})$ derived for self-biased circuit is not valid here. We therefore first derive an expression for $S(I_{CO})$ from the basic definition, that is,

$$S(I_{CO}) = \frac{dI_C}{dI_{CO}}$$

writing KVL for the collector base circuit,

$$V_{CC} = (I_C + I_B)(R_C + R_E) + I_B R_B + V_{BE}$$

and using $I_C = \beta I_B + (1 + \beta) I_{CO}$

Eliminating I_B and simplifying, we get

$$I_C \left[1 + \frac{\beta(R_C + R_E)}{R_C + R_E + R_B}\right] = (1 + \beta) I_{CO} + \frac{\beta(V_{CC} - V_{BE})}{R_C + R_E + R_B}$$

Differentiating w.r.t. I_{CO}, we get

$$S(I_{CO}) = \frac{dI_C}{dI_{CO}} = \frac{1 + \beta}{1 + \beta \dfrac{(R_C + R_E)}{R_C + R_E + R_B}}$$

Putting the values, we get

$$S(I_{CO}) = \frac{51}{1 + 50 \dfrac{10.5}{133.3}}$$
$$= \frac{51}{1 + 3.9} = 10.4$$

(iii) The incremental change in I_C at 100°C is

$$\Delta I_C = S(I_{CO})\, \Delta I_{CO} \quad \text{[From Table 5.1]}$$
$$= 10.4\ (20 - 0.1) \text{ nA}$$
$$= 10.4\ (19.9) = 0.2 \text{ mA}$$

The value of I_C at 100°C is

$$I_{C\ 100°C} = 1.75 + 0.2$$
$$= 1.95 \text{ mA}$$

EXAMPLE 5.10

Determine the stability factor and the change in I_C for temperature variation of 25°C to 100°C for the self bias circuit. Assume $\beta = 100$.

(i) $S(I_{CO})$ for $R_B/R_E = 10$

(ii) $S(V_{BE})$ for $R_B = 240$ kΩ, $R_E = 1$ kΩ

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Solution (i) Using Eq. (5.36),

$$S(I_{CO}) = (1+\beta)\frac{1+R_B/R_E}{1+\beta+R_B/R_E}$$

$$= 101\frac{(1+10)}{(1+100+10)} = 101\left(\frac{11}{111}\right) = 10$$

and

$$\Delta I_C = S(I_{CO})\Delta I_{CO}$$

$$= (10)(20 - 0.1)\text{ nA} \qquad \text{[Taking data from Table 5.1]}$$

$$= (10)(19.9)\text{ nA}$$

$$= 199\text{ nA} = 0.199\ \mu\text{A}$$

(ii) From Eq. (5.41)

$$S(V_{BE}) = \frac{-\beta}{R_B + (1+\beta)R_E}$$

$$= \frac{-100}{240 + (101)1}$$

$$= \frac{-100}{341} = -0.293\times10^{-3}$$

and

$$\Delta I_C = S(V_{BE})\Delta V_{BE}$$

$$= (-0.293\times10^{-3})(0.48 - 0.65) \qquad \text{[using Table 5.1]}$$

$$= (-0.293\times10^{-3})(-0.17)$$

$$\simeq 50\ \mu\text{A}$$

EXAMPLE 5.11

Determine $S(\beta)$ and the value of I_C at 100°C, for a self bias circuit. Given: I_C at 25°C = 2 mA and the ratio $R_B/R_E = 10$. Take data from Table 5.1.

Solution From Eq. (5.45),

$$S(\beta) = \frac{I_{C1}(1+R_B/R_E)}{\beta_1(1+\beta_2+R_B/R_E)}$$

$$= \frac{2\times10^{-3}(1+10)}{50(1+80+10)}$$

$$= \frac{22\times10^{-3}}{4550} = 4.83\times10^{-6}$$

and

$$\Delta I_C = S(\beta)(\Delta\beta)$$

$$= 4.83\times10^{-6}\,(80 - 50)$$

$$= (4.83\times10^{-6})(30)$$

$$\simeq 0.145\text{ mA}$$

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The value of I_C at 100°C is:

$$I_C|_{100°C} = 2 + 0.145$$
$$= 2.145 \text{ mA.}$$

EXAMPLE 5.12

For the self biased circuit of Fig. 5.9(b), the ratio $R_B/R_E = 2$ and $R_E = 4.7$ kΩ. The collector supply voltage V_{CC} and R_C are so adjusted to establish $I_C = 2$ mA at 25°C (room temperature). Determine the variation of I_C over the temperature range –65°C to 175°C for the silicon transistor. Take data required from Table 5.1.

Solution At 25°C, $\beta = 50$, and $R_B/R_E = 2$ (Given).

Using Eq. (5.36),

$$S(I_{CO})|_{25°C} = (1+\beta)\frac{1+R_B/R_E}{1+\beta+R_B/R_E}$$

$$= 51\frac{1+2}{51+2} = 2.89$$

Using Eq. (5.41),

$$S(V_{BE})|_{25°C} = \frac{-\beta/R_E}{1+\beta+R_B/R_E}$$

$$= \frac{-50/4.7}{1+50+2} = -0.2\times10^{-3}$$

Using Eq. (5.45),

$$S(\beta) = \frac{I_{C1}(1+R_B/R_E)}{\beta_1(1+\beta_2+R_B/R_E)}$$

So $$S(\beta)|_{-65°C} = \frac{2\times10^{-3}(1+2)}{50(1+20+2)} = 5.2 \text{ μA}$$

and $$S(\beta)|_{175°C} = \frac{2\times10^{-3}(1+2)}{50(1+120+2)} = 0.97 \text{ μA}$$

From Eq. (5.50) $$\Delta I_C = S(I_{CO})\Delta I_{CO} + S(V_{BE})\Delta V_{BE} + S(\beta)\Delta\beta$$

Taking data from Table 5.1, we get

$$\Delta I_C(-65°) = 2.89(0.2\times10^{-3} - 0.1)10^{-9} - 0.2\times10^{-3}(0.85 - 0.65) + 5.2\times10^{-6}(20 - 50)$$
$$= -2.89\times0.099\times10^{-9} - 0.2\times10^{-3}\times0.2 - 5.2\times10^{-6}\times30$$
$$= -0.286\times10^{-9} - 0.04\times10^{-3} - 156\times10^{-6}$$
$$= -0.196286 \text{ mA}$$

and $$\Delta I_C(175°) = 2.89(3.3\times10^{3} - 0.1)\times10^{-9} - 0.2\times10^{-3}(0.30 - 0.65) + 5.2\times10^{-6}(120 - 50)$$

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$$= 2.89 \times 3.3 \times 10^{3} \times 10^{-9} + 0.2 \times 10^{-3} \times 0.35 + 5.2 \times 10^{-6} \times 70$$
$$= 9.537 \times 10^{-6} + 70 \times 10^{-6} + 364 \times 10^{-6}$$
$$= 443.5 \times 10^{-6} = 0.443 \text{ mA}$$

Hence, the collector current at –65°C is:

$$= (2.0 - 0.196) = 1.804 \text{ mA}$$

That is, the collector current reduces.

The collector current at 175°C is:

$$= (2.0 + 0.443) = 2.443 \text{ mA}$$

$$I_C|_{-65°C} = 1.804 \text{ mA}$$
$$I_C|_{175°C} = 2.443 \text{ mA}$$

Ans.

5.8 BIASING TECHNIQUES FOR BJT INTEGRATED CIRCUITS (ICs)

The various biasing circuits discussed earlier are not suitable for the design of IC amplifiers. These biasing circuits, in general, need two to three resistors of large values as well as large coupling and bypass capacitors. It is quite uneconomical to fabricate large values of resistors and impossible to fabricate large capacitors in IC circuits. The biasing of IC circuits, therefore, is quite different from that employed in discrete BJT amplifiers. The biasing in integrated circuits is based on the use of constant current sources. In this section, we shall study various constant current sources.

5.8.1 Constant Current Source (Current Mirror)

A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of the collector voltage. In the basic circuit shown in Fig. 5.22 transistors Q_1 and Q_2 are matched as the circuit is fabricated using IC technology. It may be noted that bases and emitters of Q_1 and Q_2 are tied together and thus have the same V_{BE}. In addition, transistor Q_1 is connected as a diode by shorting its collector to base.

The input current I_{ref} flows through the diode-connected transistor Q_1 and thus establishes a voltage across Q_1. This voltage in turn appears between the base and emitter of Q_2. Since Q_2 is identical to Q_1, the emitter current of Q_2 will be equal to the emitter current of Q_1 which is approximately equal to I_{ref}. Thus, we can say that as long as Q_2 is maintained in the active region, its collector current $I_{C2} = I_0$ will be

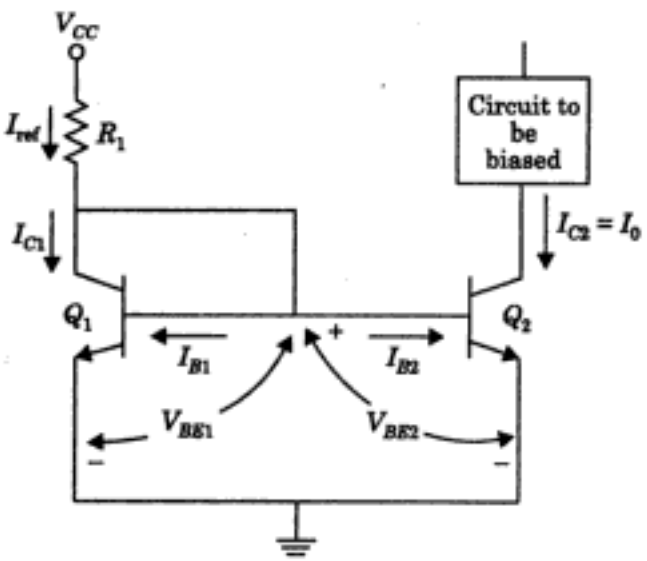


Fig. 5.22 The basic BJT current mirror ($V_{BE1} = V_{BE2}$).

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approximately equal to I_{ref}. Since the output current I_0 is a reflection or mirror of the reference current I_{ref}, the circuit is often referred to as a current mirror.

This mirror effect is however, valid only for large values of β. To study the effect of β on the operation of the current mirror circuit, we analyze it further.

The collector currents I_{C1} and I_{C2} for transistors Q_1 and Q_2 can be approximately expressed as

$$I_{C1} \cong \alpha_F I_{ES}\, e^{V_{BE1}/V_T} \tag{5.51}$$

$$I_{C2} \cong \alpha_F I_{ES}\, e^{V_{BE2}/V_T} \tag{5.52}$$

From Eqs. (5.51) and (5.52), we may write

$$\frac{I_{C2}}{I_{C1}} = e^{(V_{BE2} - V_{BE1})/V_T} \tag{5.53}$$

Since $V_{BE1} = V_{BE2}$, we obtain

$$I_{C2} = I_{C1} = I_C = I_0$$

Also since both the transistors are identical, $\beta_1 = \beta_2 = \beta$. KCL at the collector of Q_1 gives

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} \tag{5.54}$$

$$= I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2}$$

$$= I_C \left(1 + \frac{2}{\beta}\right) \tag{5.55}$$

Solving Eq. (5.55), I_C may be expressed as:

$$I_C = \frac{\beta}{\beta + 2} I_{ref} \tag{5.56}$$

where I_{ref} from Fig. 5.22 can be seen to be

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \cong \frac{V_{CC}}{R_1} \quad \text{(as } V_{BE} = 0.7 \text{ V is small)} \tag{5.57}$$

It can be seen from Eq. (5.56) that, for $\beta >> 1$, $\beta/(\beta + 2)$ is almost unity so that the output current I_0 is equal to the reference current I_{ref} which for a given R_1 is constant. Typically I_0 varies by about 3% for $50 \leq \beta \leq 200$.

The circuit, however, operates as a constant current source as long as Q_2 remains in the active region. From the volt-ampere characteristics of Q_2 shown in Fig. 5.23, it can be seen that for $V_{CE2} < 0.3$ V, Q_2 is saturated. For $V_{CE2} > 0.3$ V, transistor operates in the active region and I_{C2} is essentially constant.

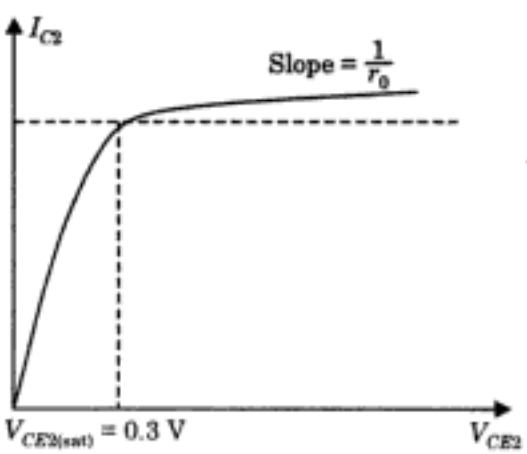


Fig. 5.23 Volt-ampere characteristics of transistor Q_2.

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The slight increase in I_{C2} is due to Early effect. The 1/slope of the curve in this region equals to the reciprocal of the output resistance r_0 of the current source.

The consequence of Early effect is to deviate I_{C1}/I_{C2} from unity. This, however, is not being discussed here. For all practical purposes, Early voltage may be assumed to be infinite, so that $r_0 \to \infty$ and I_{C2} is constant.

EXAMPLE 5.13

The current mirror of Fig. 5.22 is to provide a 1.0 mA current with V_{CC} = 10 V. Assume $\beta = 125$ and V_{BE} = 0.7 V. Determine (i) the value of R_1 (ii) value of R_1 for I_C = 10 μA.

Solution (i) From Eq. (5.56), we have

$$1.0 = \frac{125}{125+2} \times \frac{10-0.7}{R_1}$$

$$R_1 = 9.15 \text{ k}\Omega$$

(ii) Again using Eq. (5.56), the value of R_1 is found to be

$$R_1 = \frac{125}{125+2} \times \frac{10-0.7}{10} = 915 \text{ k}\Omega$$

We find that for small values of output current, we require large resistance R_1.

5.8.2 Widlar Current Source

The basic current mirror of Fig. 5.22 has a limitation. Whenever we need low value current source as in Example 5.13 part (b), the value of the resistance R_1 required is sufficiently high and can not be fabricated economically in IC circuits. Figure 5.24 shows a widlar current source which is particularly suitable for low value of currents. The circuit differs from the basic current mirror only in the resistance R_E that is included in the emitter lead of Q_2. It can be seen that due to R_E, the base-emitter voltage V_{BE2} is less than V_{BE1} and consequently current I_0 is smaller than I_{C1}.

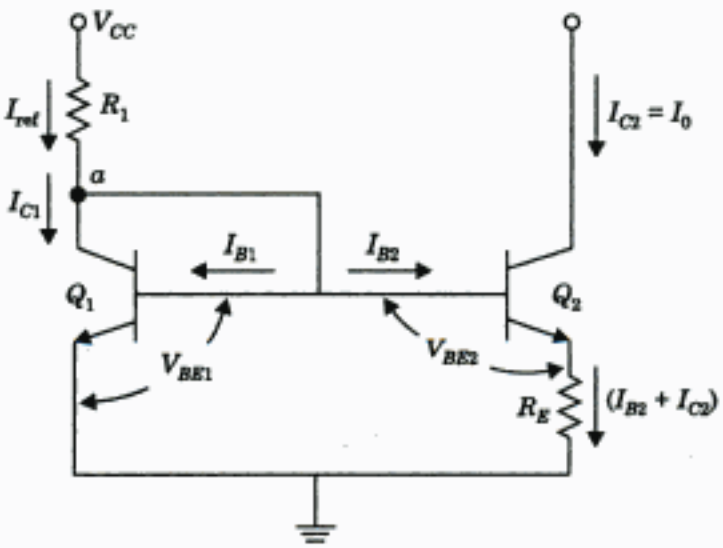


Fig. 5.24 Widlar current source ($V_{BE2} < V_{BE1}$).

The ratio of collector currents I_{C1} and I_{C2} using Eqs. (5.51) and (5.52) is given by

$$\frac{I_{C1}}{I_{C2}} = e^{(V_{BE1} - V_{BE2})/V_T} \qquad (5.58)$$

Taking natural logarithm of both sides, we get

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) \qquad (5.59)$$

Writing KVL for the emitter base loop,

$$V_{BE1} = V_{BE2} + (I_{B2} + I_{C2})R_E \tag{5.60}$$

or
$$V_{BE1} - V_{BE2} = \left(\frac{1}{\beta} + 1\right) I_{C2} R_E \qquad \left(\because \; I_{B2} = \frac{I_{C2}}{\beta}\right) \tag{5.61}$$

From Eqs. (5.59) and (5.61), we obtain

$$\left(\frac{1}{\beta} + 1\right) I_{C2} R_E = V_T \ln \frac{I_{C1}}{I_{C2}} \tag{5.62}$$

or
$$R_E = \frac{V_T}{\left(1 + \frac{1}{\beta}\right) I_{C2}} \ln \frac{I_{C1}}{I_{C2}} \tag{5.63}$$

A relation between I_{C1} and the reference current I_{ref} is obtained by writing KCL at the collector point of Q_1 (node a):

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} \tag{5.64}$$

$$= I_{C1}\left(1 + \frac{1}{\beta}\right) + \frac{I_{C2}}{\beta} \tag{5.65}$$

(Assuming $\beta_1 = \beta_2 = \beta$ for identical transistors)

In the widlar current source $I_{C2} << I_{C1}$, therefore, the term I_{C2}/β may be neglected in Eq. (5.65). Thus,

$$I_{ref} \cong I_{C1}\left(1 + \frac{1}{\beta}\right) \tag{5.66}$$

or
$$I_{C1} = \frac{\beta}{\beta + 1} I_{ref} \tag{5.67}$$

where
$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \tag{5.68}$$

For $\beta >> 1$,
$$I_{C1} \cong I_{ref} \tag{5.69}$$

The design and advantages of Widlar current source are illustrated in Example 5.14.

EXAMPLE 5.14

Design a Widlar current source for generating a constant current $I_0 = 10\ \mu A$. Assume $V_{CC} = 10$ V, $V_{BE} = 0.7$ V, $\beta = 125$. Use $V_T = 25$ mV.

Solution For the Widlar current source of Fig. 5.24, we must first decide a suitable value for I_{ref}. If we choose $I_{ref} = 1$ mA, then R_1 is given by

$$R_1 = \frac{10 - 0.7}{1} = 9.3\ k\Omega$$

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The value of R_E is determined from Eq. (5.63):

$$R_E = \frac{0.025}{\left(1+\frac{1}{125}\right)10\times10^{-6}} \ln\left(\frac{1}{10}\right)$$

$$= 11.5 \text{ k}\Omega$$

It is clearly seen that Widlar circuit allows the generation of small constant using relatively small resistors.

Modified Widlar Current Sources

Sometimes, it is convenient to use emitter resistance in both the transistors Q_1 and Q_2 as shown in Fig. 5.25. If $R_1 = R_2$ the currents $I_{C1} = I_{C2}$. The circuit can also be used to provide different currents in Q_1 and Q_2.

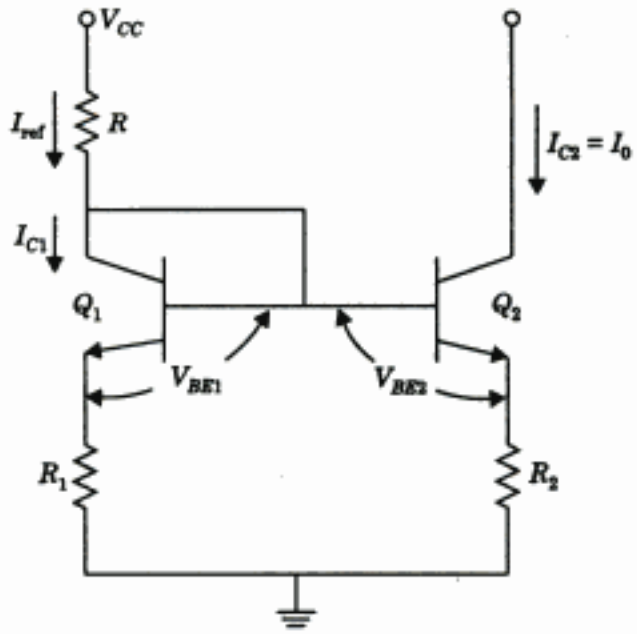


Fig. 5.25 A current mirror with magnification ($I_{C2}/I_{C1} \approx R_1/R_2$).

Analysis

Rewriting Eq. (5.53) as:

$$V_{BE2} - V_{BE1} = V_T \ln \frac{I_{C2}}{I_{C1}} \tag{5.70}$$

Writing KVL in the base emitter loop,

$$V_{BE2} - V_{BE1} = I_{C1}R_1 - I_{C2}R_2 \quad \text{(Neglecting base current)} \tag{5.71}$$

From Eq. (5.71) and Eq. (5.72), we get

$$I_{C1}R_1 - I_{C2}R_2 = V_T \ln \frac{I_{C2}}{I_{C1}} \tag{5.72}$$

$$\frac{I_{C2}}{I_{C1}}\frac{R_2}{R_1} = 1 - \frac{V_T}{I_{C1}R_1} \ln \frac{I_{C2}}{I_{C1}} \tag{5.73}$$

$$\frac{I_{C2}}{I_{C1}} = \frac{R_1}{R_2}\left(1 - \frac{V_T}{I_{C1}R_1} \ln \frac{I_{C2}}{I_{C1}}\right) \tag{5.74}$$

For the range $0.1 < \frac{I_{C2}}{I_{C1}} < 10$, we can assume $\frac{I_{C2}}{I_{C1}} \cong \frac{R_1}{R_2}$. Thus, even large ratio I_{C2}/I_{C1} (say 10) is easily obtained by the modified circuit.

5.8.3 Current Repeaters

The basic current mirror of Fig. 5.22 can be used to source current to more than one load. Such a circuit is called current repeater and is shown in Fig. 5.26. If all the transistors are identical then the current

$$I_C = I_{C1} = \ldots \ldots = I_{CN} \cong I_{ref}$$

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It can be seen from Fig. 5.26 at node a,

$$I_{ref} = I_C + I_B + NI_B \quad \text{(Assuming identical transistors)} \tag{5.75}$$

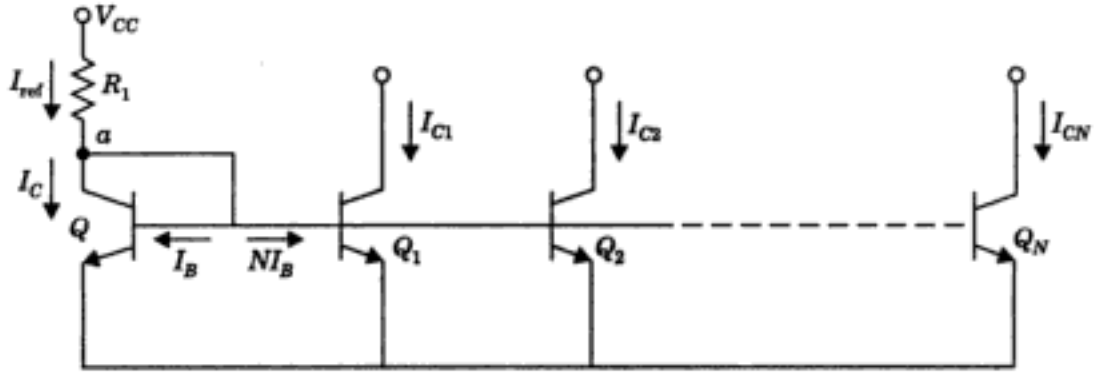


Fig. 5.26 A current repeater to source current to N transistors Q_1, Q_2 ... Q_N.

$$= I_C + \frac{(1+N)}{\beta} I_C$$

$$= I_C \left(1 + \frac{(1+N)}{\beta}\right) \tag{5.76}$$

Thus,
$$I_C = I_{ref} \frac{\beta}{\beta + 1 + N} \tag{5.77}$$

It is possible to achieve different values of I_{C1}, I_{C2}, ..., ..., I_{CN} by scaling the emitter area of transistors Q_1, Q_2, ..., ..., Q_N. The same can also be achieved by using emitter resistance as illustrated by Example 5.15.

EXAMPLE 5.15

For the circuit shown in Fig. 5.27 determine I_{C1}, I_{C2} and I_{C3}. Assume $\beta = 125$, $V_{BE} = 0.7$ V.

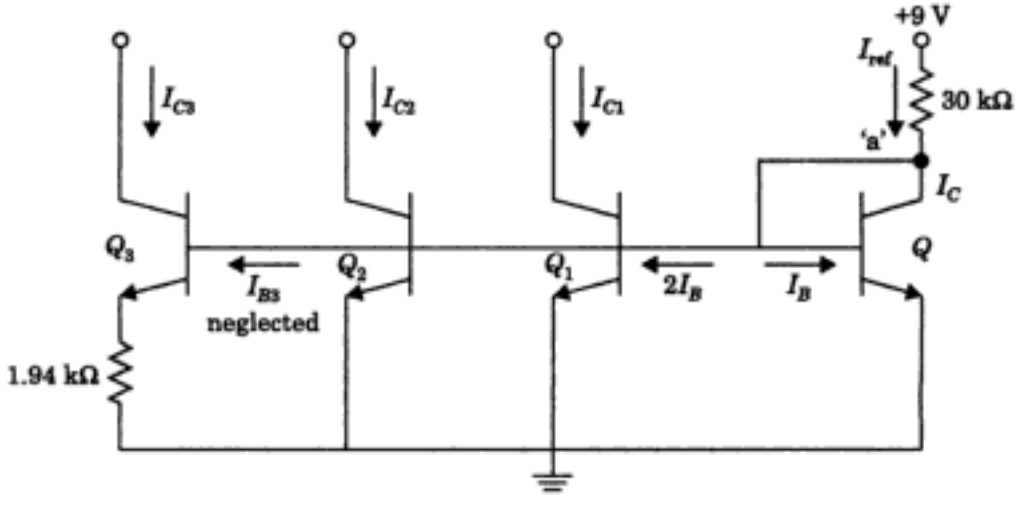


Fig. 5.27 Circuit for Example 5.15.

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Solution

$$I_{ref} = \frac{9 - 0.7}{30} = 0.277 \text{ mA}$$

Also at node a,

$$I_{ref} = I_C + 3I_B \qquad \text{(Assume } I_{B3} \text{ of Widlar source negligible)}$$

$$= I_C\left(1 + \frac{3}{\beta}\right)$$

$$I_C = I_{ref}\left(\frac{\beta}{3 + \beta}\right)$$

Putting the values and solving, we get

$$I_{C1} = I_{C2} = 0.271 \text{ mA}$$

Calculate I_{C3} using Eq. (2.74), gives

$$1.94 = \frac{0.025}{I_{C3}\left(1 + \frac{1}{125}\right)} \ln \frac{0.271}{I_{C3}}$$

Solving the transcendental equation by trial and error, we obtain

$$I_{C3} = 0.0287 \text{ mA}$$

So, we see that it is possible to design a current source capable of giving different constant currents as per the requirement of different loads.

5.8.4 Improved Current Source Circuits

A good current source must meet two requirements. The first is that the output current, I_0 should be independent of β and secondly the output resistance of the current source should be very high. The need for high output resistance current source can be seen because the common-mode gain of the differential amplifier (used as basic building block in op amps) can only be reduced by using high resistance current sources. Also, all differential amplifiers invariably use current source as a load. Thus, to obtain high voltage gain a large output resistance load is required. Now, we discuss two circuits that exhibit reduced dependence on β or increased output resistance.

A current source with gain: The circuit shown in Fig. 5.28 includes a transistor Q_3 whose emitter current supplies the base currents of Q_1 and Q_2. The expression for the source current $I_0 = I_{C2}$ can be derived by writing KCL at node a

$$I_{ref} = I_{C1} + I_{B3}$$

$$= I_{C1} + \frac{I_{E3}}{1 + \beta}$$

$$= I_{C2} + \frac{I_{E3}}{1 + \beta} \qquad (V_{BE1} = V_{BE2};\ I_{C1} = I_{C2} = I_0) \tag{5.78}$$

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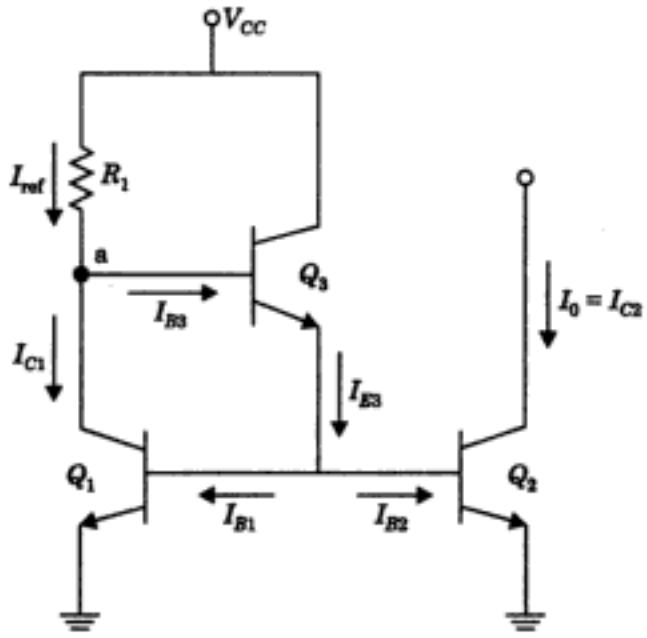


Fig. 5.28 A current source with gain.

Also $$I_{E3} = I_{B1} + I_{B2}$$
$$= 2I_B \qquad \text{(since } Q_1 \text{ and } Q_2 \text{ are identical)}$$

Thus, $$I_{ref} = I_{C1} + \frac{2I_B}{1+\beta} \tag{5.79}$$

$$= I_C + \frac{2I_C}{\beta(1+\beta)}$$

$$= I_C \left(1 + \frac{2}{\beta(1+\beta)}\right)$$

or $$I_0 = I_C = I_{ref} \frac{\beta(1+\beta)}{\beta^2 + \beta + 2} \tag{5.80}$$

where $$I_{ref} = \frac{V_{CC} - 2V_{BE}}{R_1}$$

It is easily seen from Eq. (5.80) that the output current is essentially independent of β. The output resistance of the current source is only r_0. It can, however, be increased by using emitter resistances in Q_1 and Q_2 as is done in the modified Widlar source circuit in Fig. 5.25. The two emitter resistors can also be used to make I_0 different from I_{ref}.

Wilson current source: The final current source shown in Fig. 5.29 provides an output current I_0, which is very nearly equal to I_{ref} and also exhibits a very high output resistance.

Analysis

Since $$V_{BE1} = V_{BE2}$$
$$I_{C1} = I_{C2}$$

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and $I_{B1} = I_{B2} = I_B$

At node b,

$$I_{E3} = 2I_B + I_{C2}$$

$$= \left(\frac{2}{\beta} + 1\right) I_{C2} \qquad (5.81)$$

I_{E3} is also equal to

$$I_{E3} = I_{C3} + I_{B3}$$

$$= I_{C3}\left(1 + \frac{1}{\beta}\right) \qquad (5.82)$$

From Eqs. (5.81) and (5.82), we obtain

$$I_{C3}\left(1 + \frac{1}{\beta}\right) = I_{C2}\left(1 + \frac{2}{\beta}\right)$$

$$I_{C3} = I_0 = \left(\frac{\beta + 2}{\beta + 1}\right) I_{C2} \qquad (5.83)$$

Since $I_{C1} = I_{C2}$

$$I_0 = \left(\frac{\beta + 2}{\beta + 1}\right) I_{C1} \qquad (5.84)$$

At node a,

$$I_{ref} = I_{C1} + I_{B3}$$

$$= \frac{\beta + 1}{\beta + 2} I_0 + \frac{I_0}{\beta}$$

$$= \frac{\beta^2 + 2\beta + 2}{\beta^2 + 2\beta} I_0$$

or $$I_0 = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2} I_{ref} \qquad (5.85)$$

where $$I_{ref} = \frac{V_{CC} - 2V_{BE}}{R_1} \qquad (5.86)$$

The difference $$I_0 - I_{ref} = \frac{2}{\beta^2 + 2\beta + 2} I_{ref} \qquad (5.87)$$

is extremely small error for modest values of β. The output resistance of a Wilson current mirror is substantially greater $\left(\cong \beta \frac{r_0}{2}\right)$ than that of the simple current mirror or Widlar current mirror.

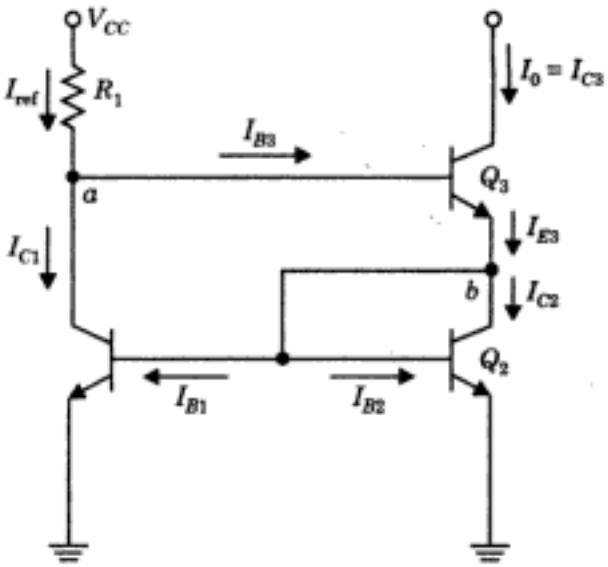


Fig. 5.29 A Wilson current source.

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EXAMPLE 5.16

For the circuit shown in Fig. 5.30, determine the value of I_0 for $\beta = 100$. Assume $V_{BE} = 0.7$ V.

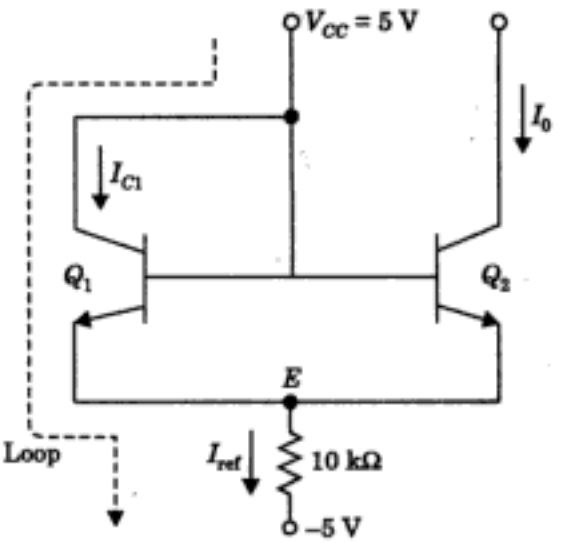


Fig. 5.30 Circuit for Example 5.16.

Solution

Writing KVL for the indicated loop

$$5 - V_{BE} - 10 \times I_{ref} + 5 = 0$$

$$I_{ref} = \frac{10 - 0.7}{10} = 0.93 \text{ mA}$$

At emitter node E,

$$I_{ref} = 2I_E$$

(Assuming identical transistors)

$$I_{ref} = 2(I_C + I_B)$$

$$= 2I_C\left(1 + \frac{1}{\beta}\right)$$

Then $$I_C = \frac{\beta}{2(1+\beta)} I_{ref} = 0.46 \text{ mA}$$

Due to mirror effect

$$I_0 = I_{C1} = I_C = 0.46 \text{ mA}$$

EXAMPLE 5.17

For the circuit shown in Fig. 5.31,

(i) Determine I_{C1} and I_{C2}.

(ii) Find R_C so that $V_0 = 6$ V. Assume $\beta = 200$.

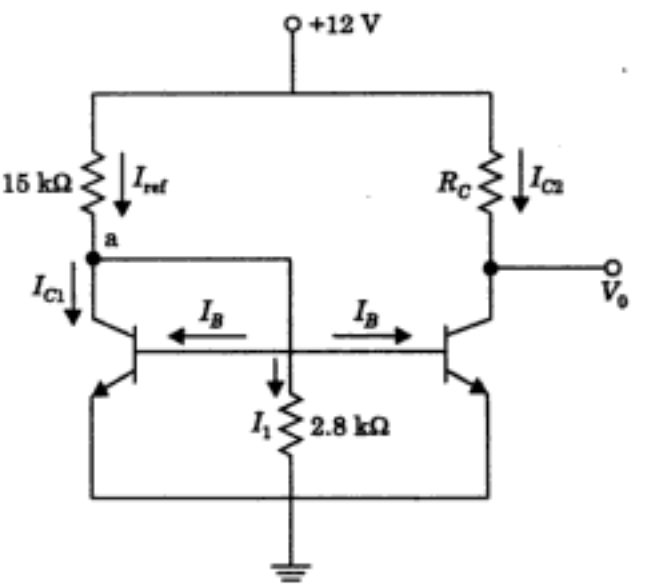


Fig. 5.31 Circuit for Example 5.17.

Solution (i) $$I_{ref} = \frac{12 - 0.7}{15} = 0.75 \text{ mA}$$

and $$I_1 = \frac{0.7}{2.8} = 0.25 \text{ mA}$$

At node a,

$$I_{ref} = I_{C1} + 2I_B + I_1$$

$$= I_{C1}\left(1 + \frac{2}{\beta}\right) + I_1$$

$\therefore$ $$0.75 = I_{C1}\left(1 + \frac{2}{\beta}\right) + 0.25$$

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Solving for I_{C1} gives

$$I_{C1} = 0.495 \text{ mA}$$
$$\cong 0.5 \text{ mA}$$

and $I_{C2} = I_{C1} = 0.5 \text{ mA}$ (due to mirror effect)

(ii) From the outer loop,

$$12 = I_{C2}R_C + V_0$$

So $$R_C = \frac{12 - 6}{0.5} = 12 \text{ k}\Omega$$

EXAMPLE 5.18

Figure 5.32 shows a modified current mirror circuit. Determine the emitter current in transistor Q_3 if $\beta = 100$ and $V_{BE} = 0.75$ V.

Solution From Fig. 5.33 at node a,

$$I = I_{C1} + I_1$$
$$= I_{C1} + I_{B1} + I_1'$$

or $$I = I_{C1}\left(1 + \frac{1}{\beta}\right) + I_1'$$

$$= I_{C1} + I_1' \quad (\text{as } \beta >> 1)$$

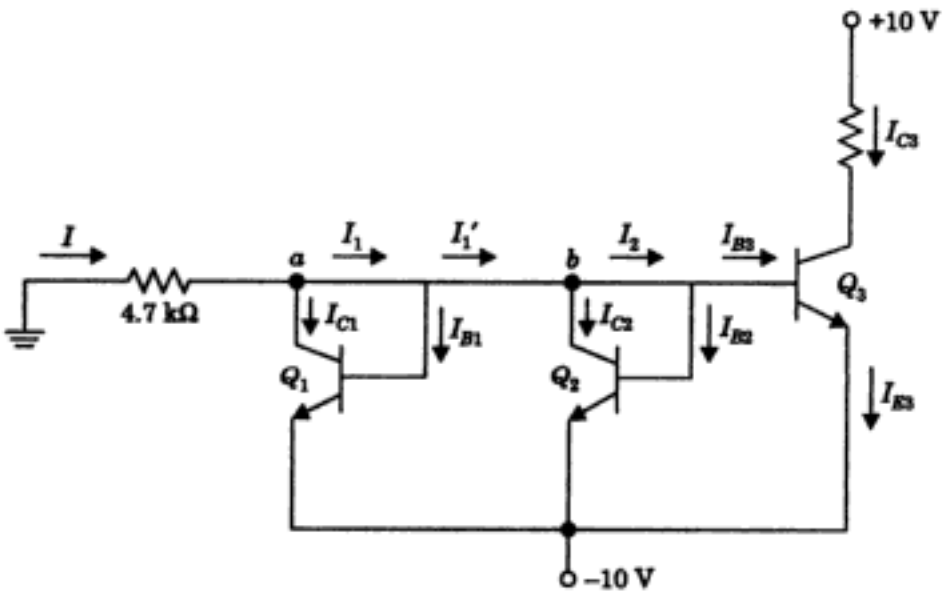


Fig. 5.32 Circuit of Example 5.18.

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Also at node b,

$$I_1' = I_{C2} + I_2$$
$$= I_{C2} + I_{B2} + I_{B3}$$
$$= I_{C2}\left(1 + \frac{1}{\beta}\right) + I_{B3}$$
$$= I_{C2} + I_{B3}$$

Putting the value of I_1', we get

$$I = I_{C1} + I_{C2} + I_{B3}$$
$$= 2I_C + I_{B3} \quad [\text{as } I_{C1} = I_{C2} = I_C]$$
$$= I_C\left(2 + \frac{1}{\beta}\right) = 2I_C$$

The current I is given by

$$I = \frac{10 - 0.75}{4.7} = \frac{9.25}{4.7} = 1.97 \text{ mA}$$

The collector current of Q_3 is equal to the collector current of Q_1 and Q_2 due to mirror action. Therefore, the emitter current is given as

$$I_{E3} = I_{C3} = I_C = \frac{I}{2} = 0.98 \text{ mA}$$

SUMMARY

- A transistor when used as an amplifier must be biased in the active region of operation to ensure distortion free output waveform.
- The operating point usually shifts with the change in temperature as transistor parameters I_{CO}, V_{BE} and β are all functions of temperature.
- A fixed bias circuit makes the base current constant whereas I_C and V_{CE} vary. Therefore, it does not provide a stable operating point against temperature variation or change of device.
- The emitter resistance R_E in the self bias circuit provides the negative feedback action and thus stabilizes the Q-point.
- A coupling capacitor is used to block dc signals. Its value should be sufficiently high so that it is short circuited at all the frequencies of interest.
- For stable operating point in a self bias circuit,

$$V_{BB} >> V_{BE}$$
$$(1 + \beta)R_E >> R_B$$

where V_{BB} and R_B are the Thevenin's equivalent voltage and equivalent resistance.

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- The sensitivity of a circuit to variation in parameters I_{CO}, V_{BE} and β is measured in terms of stability factors. The three stability factors are defined as:

$$S(I_{CO}) = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\beta = \text{constant}}$$

$$S(V_{BE}) = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\beta = \text{constant}}$$

and

$$S(\beta) = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},V_{BE} = \text{constant}}$$

- The minimum possible value of stability factor is 1.
- The expression for the various stability factors for the self bias circuit are:

$$S(I_{CO}) = (1+\beta)\frac{1 + R_B/R_E}{1 + \beta + R_B/R_E}$$

$$S(V_{BE}) = \frac{-\beta/R_E}{1 + \beta + R_B/R_E}$$

$$S(\beta) = \frac{I_{C1}(1 + R_B/R_E)}{\beta_1(1 + \beta_2 + R_B/R_E)}$$

- The total change in the collector current due to the variations in I_{CO}, V_{BE} and β over a specified temperature range is given by

$$\Delta I_C = S(I_{CO})\,\Delta I_{CO} + S(V_{BE})\,\Delta V_{BE} + S(\beta)\,\Delta\beta$$

- A current mirror is used for biasing IC circuits as it uses smaller values of resistors compared to discrete-biasing circuits.
- The output current in a current mirror is equal to reference current for large β and varies by about 3% for $50 \le \beta \le 200$.
- A Widlar current sources can provide low values of currents and high output resistance compared to basic current mirror.
- A current repeater can source current into more than one load.
- A Wilson current mirror is better than Widlar current source as (i) difference $(I_0 - I_{ref})$ is extremely small even for the modest values of β (ii) output resistance is higher than Widler current source.

REVIEW QUESTIONS

5.1 Name the ratings that limit the range of operation of a transistor.

5.2 What type of output waveform is obtained for a sinusoidal input to a CE amplifier when no dc bias is applied to emitter base junction.

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5.3 Name the region in which a transistor is biased when used as (i) amplifier (ii) a switch.

5.4 Why ac signal source is connected to the amplifier through a coupling capacitor? Give its suitable value.

5.5 Explain the limitation of a fixed bias circuit.

5.6 Explain the difference in dc and ac load lines. Is dc load larger or smaller than the ac load?

5.7 List the causes of variation of collector current in an amplifier.

5.8 Explain qualitatively why a self bias circuit is an improvement over the fixed bias circuit.

5.9 Explain how the Q-point is obtained graphically.

5.10 Define the three stability factors.

5.11 Stability factor of a circuit should be large or small?

5.12 Can stability factor be less than 1?

5.13 Give the temperature range over which manufacturers usually provide the data for a transistor.

5.14 Why the bias circuits used for discrete component amplifiers is not suitable for integrated circuits?

5.15 Sketch the basic current mirror and explain how it works as a constant current source.

5.16 Explain the limitations of the basic current mirror. Discuss a circuit that will overcome these.

5.17 Explain the advantages of a Wilson current mirror over a Widlar current source.

NUMERICAL PROBLEMS

P5.1 For a fixed bias circuit some information is provided in Fig. P-1. Determine: (a) I_C, (b) V_{CC}, (c) β, (d) R_B.

(Ans: 3.98 mA, 15.96 V, 199, 763 kΩ)

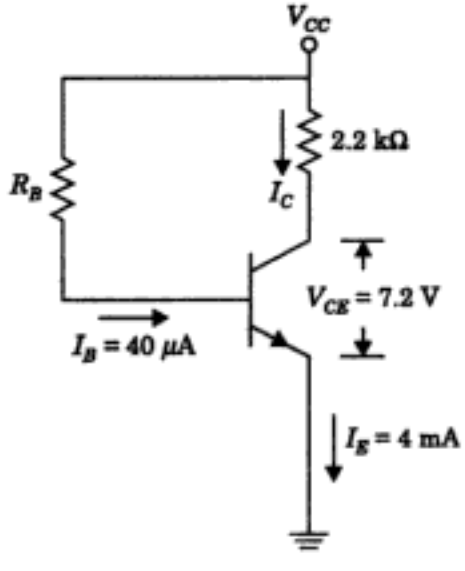


Fig. P-1

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P5.2 In an emitter stabilized bias circuit, value of some of the voltages and currents are shown in Fig. P-2. Determine: (a) β, (b) V_{CC}, (c) R_B.

(Ans: 153.3, 17.6 V, 740 kΩ)

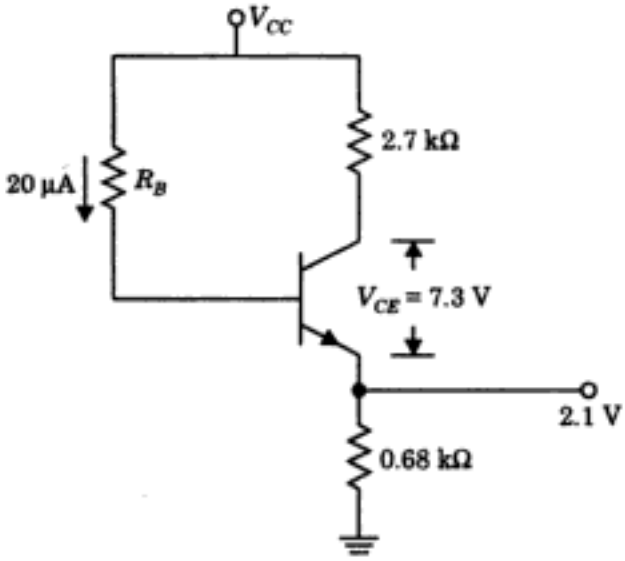


Fig. P-2

P5.3 For the three self-bias circuits shown in Fig. P-3, compute all the unknown quantities in the figures.

(Ans: for (a) part only: I_{CQ} = 1.6 mA, I_B = 0.02 mA, V_C = 9.76 V, V_E = 1.1 V, V_{CEQ} = 8.66 V)

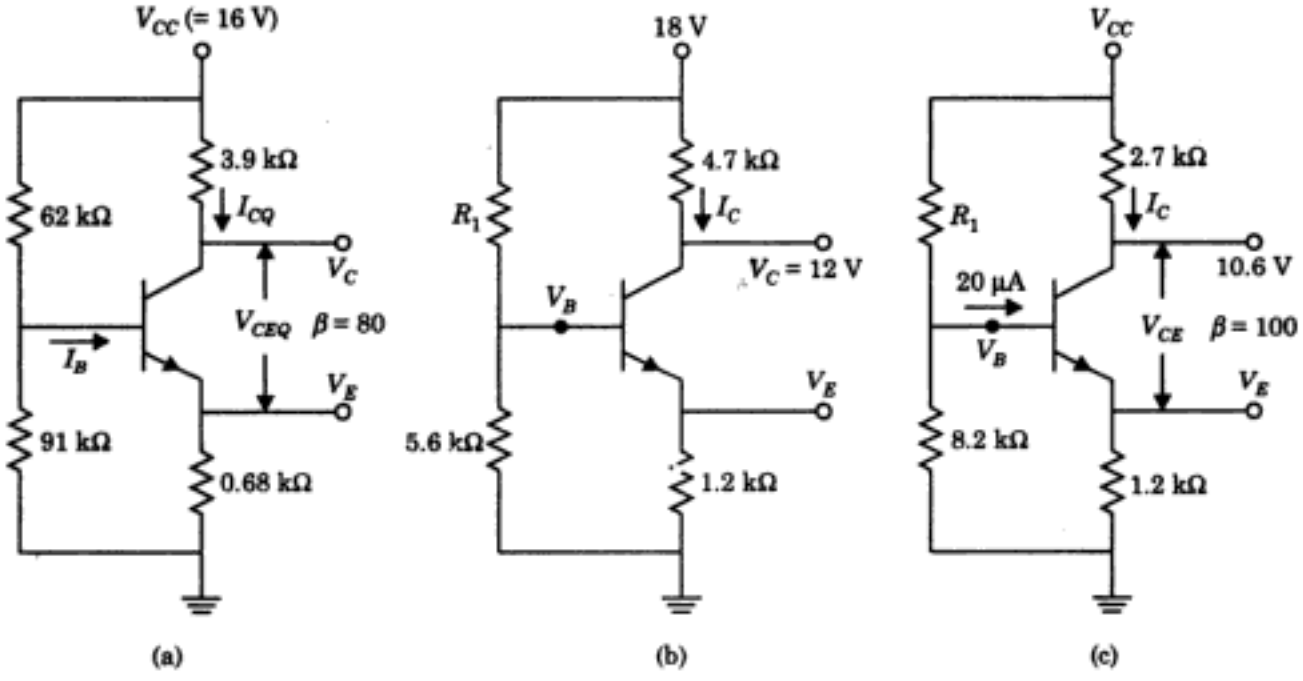


Fig. P-3

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P5.4 For the collector to base bias circuit shown in Fig. P-4 determine (a) V_C, (b) $S(I_{CO})$. Assume $\beta = 120$.

(Ans: 9.952 V, 53)

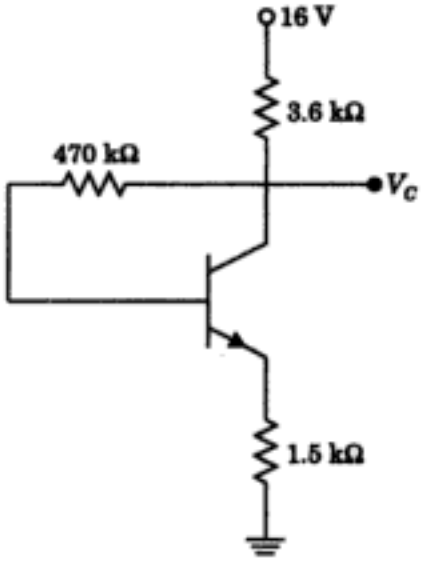


Fig. P-4

P5.5 Derive an expression for the stability factor $S(I_{CO})$ for the circuit shown in Fig. P-5.

$$\left(\textbf{Ans}: S = \frac{(1+\beta)[R_2(R_C + R_1) + R_E(R_1 + R_2 + R_3]}{R_1R_2 + (1+\beta)[R_1R_C + R_E(R_1 + R_2 + R_C)]}\right)$$

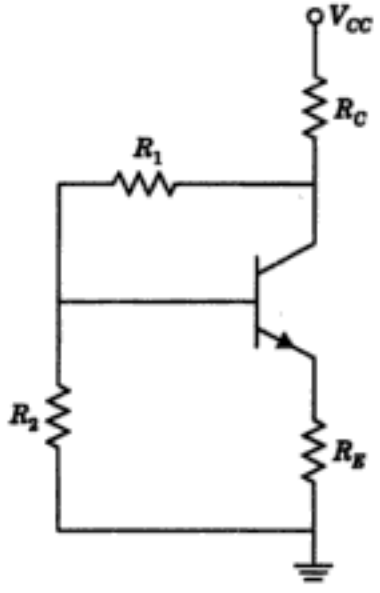


Fig. P-5

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P5.6 A transformer coupled amplifier stage is shown in Fig. P-6. Given: $V_{CEQ} = 4$ V, $\beta = 50$ and $V_{BE} = 0.7$ V. Determine (a) R_E, (b) $S(I_{CO})$.

(Ans: $R_E = 2.74$ kΩ, $S = 1$**)**

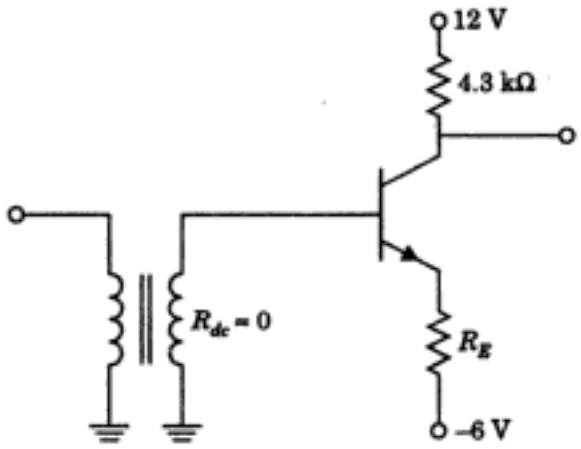


Fig. P-6

P5.7 In a self biased circuit, the Q-point is established at $V_{CE} = 12$ V and $I_C = 1.5$ mA. Determine R_E, R_1 and R_2 so that $S(I_{CO}) = 3$. Assume: $\beta = 50$, $V_{BE} = 0.7$ V, $V_{CC} = 22.5$ V.

(Ans: $R_1 = 22.8$ kΩ, $R_2 = 3.4$ kΩ, $R_E = 1.4$ kΩ**)**

P5.8 For a self-bias circuit, $R_E = 1$ kΩ, $R_B = R_1 \| R_2 = 7.75$ kΩ. The collector current I_C is 1.5 mA at 25°C. Determine the value of I_C at –65°C and 175°C.

(Ans: 1.12 mA, 2.18 mA**)**

P5.9 Design a self bias circuit for the case $V_{CC} = 9$ V to provide $1/3(V_{CC})$ across each of R_E and R_C, $I_E = 0.5$ mA and the current through the voltage divider $0.2I_E$. Assume β has very large value.

(Ans: $R_C = R_E = 6$ kΩ; $R_1 = 53$ kΩ, $R_2 = 37$ kΩ**)**

P5.10 In a self bias circuit, let $R_C = 5.6$ kΩ, $R_E = 1$ kΩ, $R_1 = 90$ kΩ, $R_2 = 10$ kΩ and $I_C = 1.5$ mA at 25°C. Using Table 5.1, find I_C at –65°C and 175°C.

(Ans: 1.104 mA, 2.22 mA**)**

P5.11 For the current mirror shown in Fig. P-11, determine R so that $I_0 = 100$ μA.

(Ans: 137.5 kΩ**)**

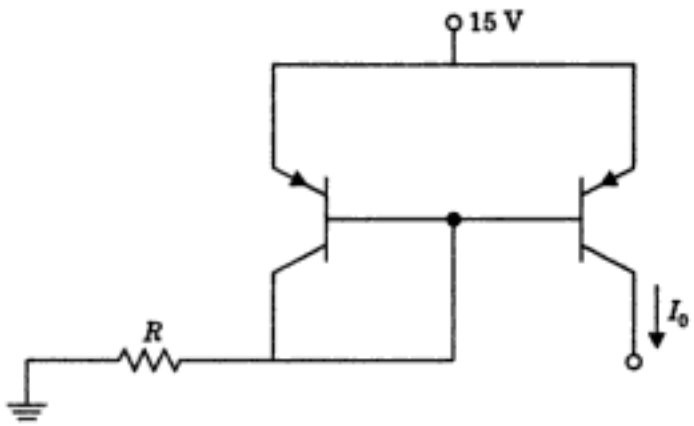


Fig. P-11

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P5.12 In the circuit of Fig. P-12, $I_R = 50\ \mu A$. What is the ratio R_1/R_2 needed for $I_0 = 100\ \mu A$.

(Ans: $R_1/R_2 \simeq 2$)

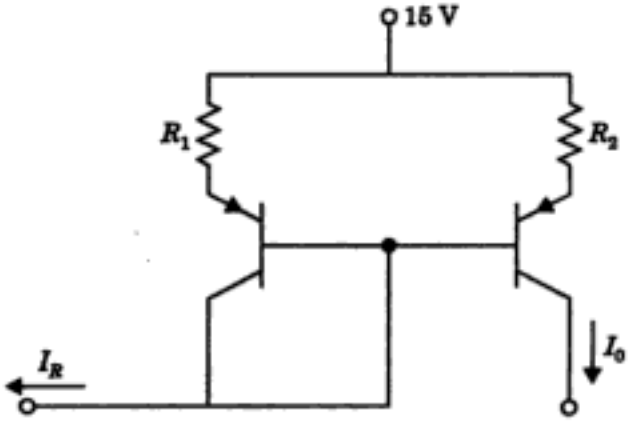


Fig. P-12

P5.13 A modified current mirror is shown in Fig. P-13. Calculate (a) the current through the collector resistor R_C, (b) the collector current through each transistor. Assume: $V_{BE} = 0.7$ V and $\beta = 100$.

(Ans: 7.5 mA, 2.5 mA)

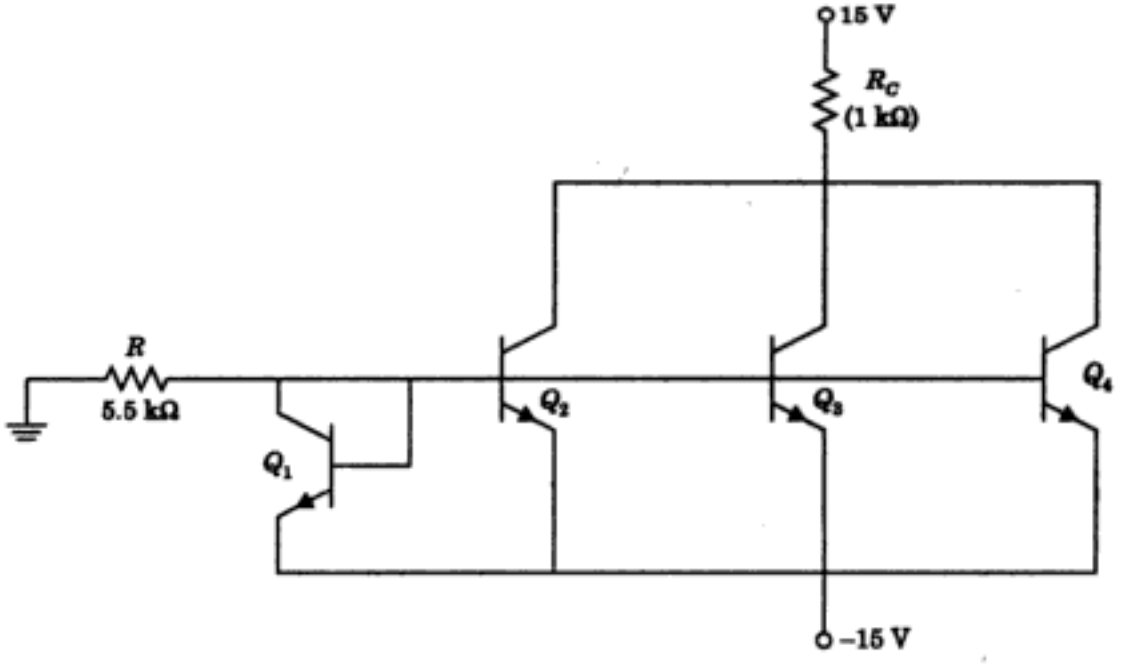


Fig. P-13

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CHAPTER 6

BJT Amplifiers

6.1 INTRODUCTION

BJT (Bipolar Junction Transistor) and FET (Field Effect Transistor) are the two most important semiconductor devices used for the amplification and switching applications. As an example, speech signals are amplified in a public address system where signal from the microphone is amplified by a cascaded amplifier stages and fed to speaker. Similarly, amplifiers are needed in radios, record players, TV etc. The switching applications of the transistor are in digital circuits, computers and memories etc. In Chapters 4 and 5, the volt-ampere characteristics of a BJT, need for dc biasing and various biasing circuits were discussed. In this chapter, we discuss the use of a BJT as an amplifier in different configurations such as CE, CB and CC configurations and study their comparative performance.

A transistor operates linearly for small input signals, so a small signal model of the transistor has been developed in the active region of operation. There are three different models used for the small signal ac analysis of transistor amplifiers: h-parameter model, hybrid-π model and r_e (or T) model. The use of these models for performing ac analysis of amplifier circuits has been illustrated by a number of solved examples. Graphical analysis though cumbersome and rarely used, but it gives an insight into the working of the circuit, is also discussed.

All the transistor amplifier circuits are examined at audio frequencies where the internal capacitances of the transistor and the coupling and by-pass capacitors can be neglected. The analysis of the transistor amplifier at very low and very high frequencies is discussed later in the Chapter 9.

6.2 SMALL SIGNAL MODELS OF A BJT

There are three small signal models of a BJT in use:

(i) h-parameter model, (ii) hybrid-π model and (iii) r_e-model.

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The h-parameter model is used extensively for transistor circuit ac analysis as h-parameters are usually specified by the manufacturers in the data sheets. However, it has the limitation that the h-parameters are specified by the manufacturer only at a typical operating point, whereas the circuit to be analyzed may be operating at a different operating point. Thus, the use of h-parameter model as an equivalent circuit of transistor does not provide exact analysis. On the other hand, the parameters of hybrid-π model or r_e-model can be determined at the given dc operating conditions and, therefore, are not limited by a single set of operating specifications provided by the manufacturer. Thus, the use of hybrid-π or r_e-model for ac analysis of transistor circuits provides more accurate analysis.

All the three models are used extensively in literature and industry. We have, therefore, examined all the three small signal models of the BJT in this chapter.

Notation

Since the BJT (and also the diode) circuits require both dc and ac currents and voltages in analysis, it will be appropriate to follow a universally used notation given as:

I_B or V_B: denotes dc part of base current and base voltage (Also implies I_{BQ} and V_{BQ}, i.e., the quiescent values)

i_b or v_b: denotes ac part of base current and base voltage

I_b or V_b: denotes the rms values of base current and base voltage

i_B or v_B: denotes (ac + dc) values collectively, i.e.,

$$i_B = I_B + i_b$$

and

$$v_B = V_B + v_b$$

We use similar notations for quantities referring to emitter and collector.

6.2.1 The Hybrid h-parameter Model

The h-parameter model for a transistor is obtained by first describing the hybrid-h model for a general two-port system. Any two-port active device such as a transistor or transformer can be specified by input and output voltages and currents as shown in Fig. 6.1.

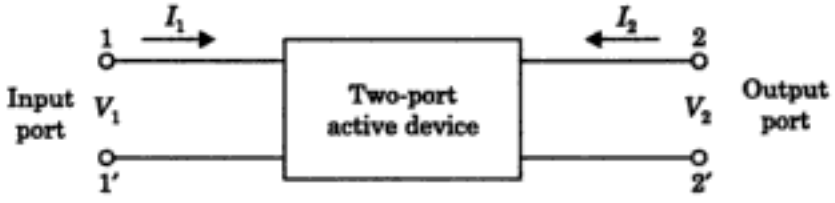


Fig. 6.1 Two-port system.

In Fig. 6.1, V_1, I_1, V_2 and I_2 are the rms (or effective) values of the ac voltages and currents. As we are doing ac analysis of the transistor, all the voltages and currents are ac signals only and can be represented either as v_1, i_1, v_2 and i_2 or by their rms values V_1, I_1, V_2 and I_2. Depending upon the device, two of these four quantities are selected as independent variables. For example, if the two-port device is a transformer then the input and output voltages (V_1 and V_2) are chosen as independent variables because this ratio is a constant and equal to the transformer turns ratio. For a transistor, input current I_1 and output voltage V_2 are usually chosen as independent variables. We may write, in general:

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$$V_1 = h_{11}I_1 + h_{12}V_2 \tag{6.1}$$

$$I_2 = h_{21}I_1 + h_{22}V_2 \tag{6.2}$$

The four parameters, h_{11}, h_{12}, h_{21} and h_{22} in Eqns. (6.1) and (6.2) have different dimensions and that is the reason that these parameters are also called **hybrid (mixed) parameters** or in brief *h-parameters*. It will further be seen that two of these parameters, h_{11} and h_{21} are short circuit parameters and the remaining two, that is h_{12} and h_{22} are open circuit parameters.

If $V_2 = 0$ in Eq. (6.1) (i.e. output port is short circuited), solving for h_{11} gives

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2 = 0} \tag{6.3}$$

It is easily seen that the parameter h_{11} is an impedance parameter and has the units of ohms. Further, since h_{11} is the ratio of input voltage and input current with output shorted, h_{11} is called the **short circuit input impedance.** The subscript 11 in h_{11} indicates that this parameter is determined by measuring quantities at the input terminals.

If, I_1 is made equal to zero in Eq. (6.1) by opening the input terminals, we get

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1 = 0} \tag{6.4}$$

The parameter h_{12} has no dimensions as it is the ratio of two voltages only. The subscript 12 in h_{12} indicates that the parameter is a transfer quantity and relates input and output quantities. This parameter is called **open circuit reverse transfer voltage ratio** as it is the ratio of input voltage to output voltage.

Similarly, the parameters h_{21} and h_{22} are obtained from Eq. (6.2) and are defined as follows:

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2 = 0} \tag{6.5}$$

This parameter is also dimensionless (like h_{12}) and is referred to as **short circuit forward current gain.** The fourth parameter, h_{22} is given by

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1 = 0} \tag{6.6}$$

The parameter h_{22} has the units of conductance and is called **output conductance** with input open circuited.

There is an alternative notation for the subscripts used with h which is more convenient and practical and is recommended by the IEEE standards:

h_{11} = Input resistance h_i

h_{12} = Reverse transfer voltage ratio h_r

h_{21} = Forward transfer current gain h_f

h_{22} = Output conductance h_o

The terminal Eqs. (6.1) and (6.2) of the two-port device can be rewritten using the suggested practical notation as:

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$$V_1 = h_i I_1 + h_r V_2 \tag{6.7}$$

$$I_2 = h_f I_1 + h_o V_2 \tag{6.8}$$

An ac equivalent circuit for the basic two-port device characterized by Eqs. (6.7) and (6.8) is shown in Fig. 6.2.

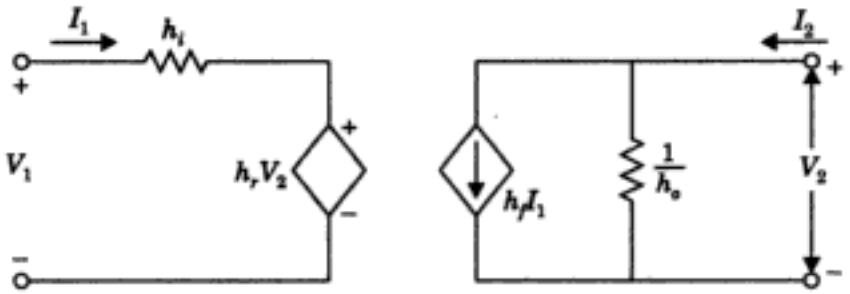


Fig. 6.2 ac equivalent circuit or *h*-model for a two-port device.

The device of our interest here is a transistor which can be used in three different configurations, i.e., *CE*, *CC* and *CB*. In order to identify the mode of operation of transistor, another subscript *e*, *c* or *b* is added in each of the *h*-parameters for *CE*, *CC* and *CB*, respectively.

Thus, the hybrid *h*-model of a transistor in *CE* configuration can be obtained by first writing the terminal equations using the graphical symbol shown in Fig. 6.3(a) as:

$$V_{be} = h_{ie} I_b + h_{re} V_{ce} \tag{6.9}$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce} \tag{6.10}$$

All the voltages and currents in these equations are the rms values of the ac signals as per the notation used.

The *h*-parameter model drawn using Eqns. (6.9) and (6.10) is shown in Fig. 6.3(b).

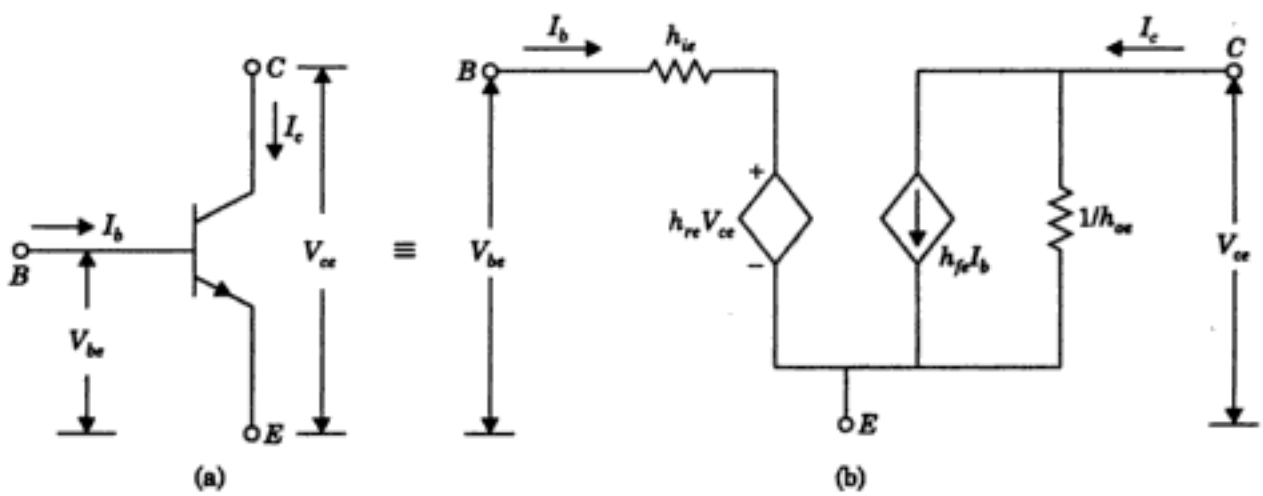


Fig. 6.3 *CE* configuration (a) graphic symbol, (b) *h*-parameter model.

In order to obtain hybrid *h*-model for any configuration, first draw the graphic symbol, indicate input and output voltages and currents, and write down the terminal equations. So, the terminal equations for a *CB* connected transistor [by using input quantities V_{eb}, I_e and the output quantities V_{cb} and I_c, as shown in graphic symbol Fig. 6.4(*a*)] can be written as:

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$$V_{eb} = h_{ib}I_e + h_{rb}V_{cb} \quad (6.11a)$$

$$I_2 = -I_c = h_{fb}I_e + h_{ob}V_{cb} \quad (6.11b)$$

The corresponding h-model is also shown in Fig. 6.4(b). Note that the output current I_2 in this case is equal to $-I_c$ (since I_2 has been assumed entering into the output port in the general analysis).

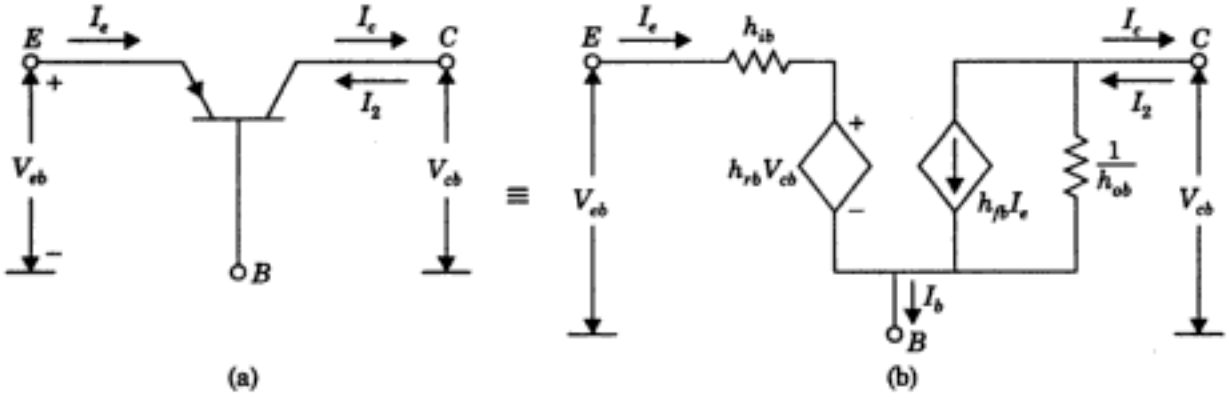


Fig. 6.4 *CB* configuration (a) graphic symbol (b) h-parameter model.

Similarly, we can draw the h-model for a *CC* transistor from its graphic symbol shown in the Fig. 6.5, using the terminal equations given as

$$V_{bc} = h_{ic}I_b + h_{rc}V_{ec} \quad (6.12a)$$

$$I_2 = -I_e = h_{fc}I_b + h_{oc}V_{ec} \quad (6.12b)$$

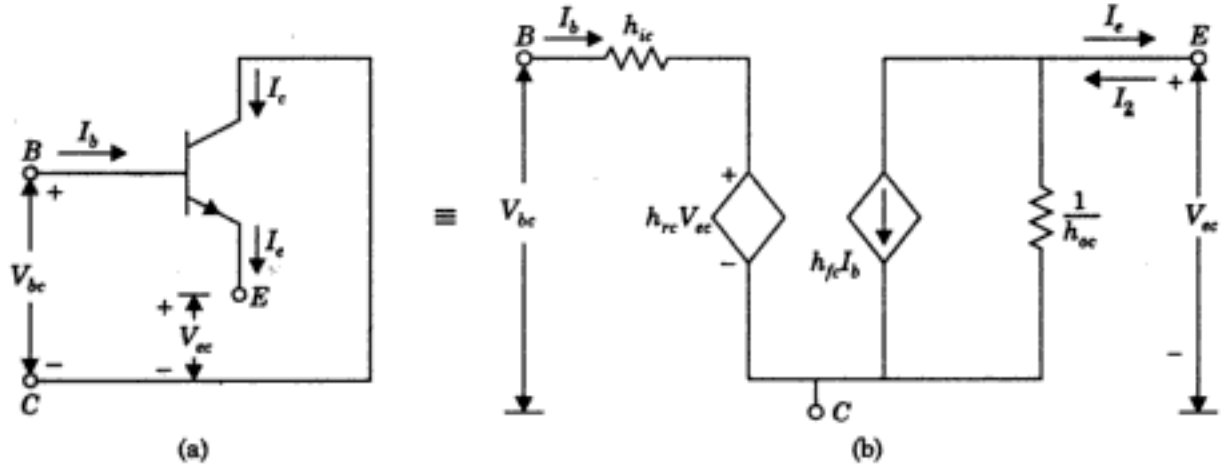


Fig. 6.5 *CC* configuration (a) graphic symbol (b) hybrid h-model.

It is possible to calculate h-parameters for a given Q-point from the output and input characteristics of transistor by using the definitions of the parameters. Thus the parameters h_{ie} and h_{re} can be determined from the input characteristics and the parameters h_{fe} and h_{oe} are obtained from the output collector characteristics of a transistor in CE configuration.

The calculation of parameters h_{fe} and h_{oe} from the output characteristics is shown in Fig. 6.6(a). We want to determine the h parameters at the quiescent point of operation. The definitions of h_{fe} and h_{oe} are given by

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$$h_{fe} = \frac{\partial i_C}{\partial i_B} = \frac{\Delta i_C}{\Delta i_B}\bigg|_{V_{CE}=\text{constant}} \tag{6.13}$$

and

$$h_{oe} = \frac{\partial i_C}{\partial v_{CE}} = \frac{\Delta i_C}{\Delta v_{CE}}\bigg|_{I_B=\text{constant}} \tag{6.14}$$

where the various voltages and currents represent the total values, that is, dc component plus ac component. Thus, $i_C = i_c + I_{CQ}$ and so on.

The symbol Δ in Eqns. (6.13) and (6.14) refers to a small change of the quantity around the Q-point. So, in Fig. 6.6(a)

$$h_{fe} = \frac{i_{C2} - i_{C1}}{i_{B2} - i_{B1}}\bigg|_{V_{CE}=V_{CEQ}} \tag{6.15}$$

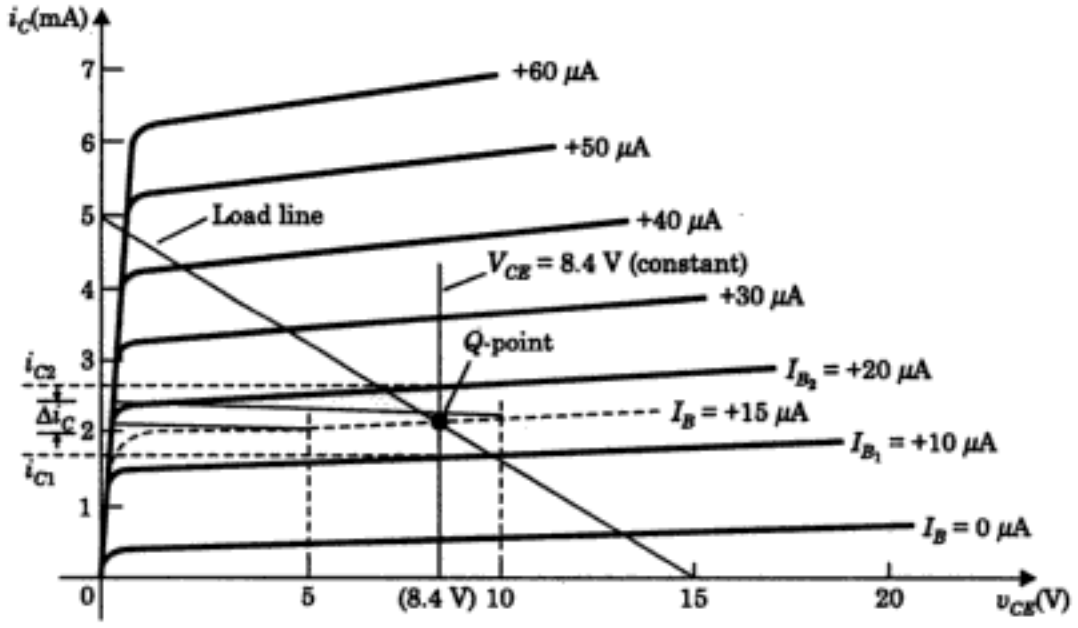


Fig. 6.6(a) Calculation of h_{fe} and h_{oe} from *CE* output characteristics.

Thus, at the Q-point (8.4 V, 15 μA) shown in Fig. 6.6(a), the value of h_{fe} is:

$$h_{fe} = \frac{\Delta i_C}{\Delta i_B}\bigg|_{V_{CE}} = \frac{2.7 - 1.7}{20 - 10}\bigg|_{V_{CE}=8.4\text{ V}} = 100$$

and

$$h_{oe} = \frac{\Delta i_C}{\Delta v_{CE}}\bigg|_{I_B} = \frac{2.4 - 2.1}{10 - 5}\bigg|_{I_B=15\ \mu\text{A}} = 60\ \mu\text{A/V}$$

To determine the parameters h_{ie} and h_{re}, the Q-point is first located on the input characteristics as shown in Fig. 6.6(b). The parameter h_{ie} is calculated by finding the change in base current i_B for a small change in V_{BE} as:

$$h_{ie} = \frac{\partial v_{BE}}{\partial i_B} = \frac{\Delta v_{BE}}{\Delta i_B}\bigg|_{V_{CE}=V_{CEQ}} \tag{6.16}$$

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$$= \left.\frac{v_{BE2} - v_{BE1}}{i_{B2} - i_{B1}}\right|_{V_{CE} = V_{CEQ}} \tag{6.17}$$

Thus, on the input characteristics shown in Fig. 6.6(b), for $V_{CE} = 8.4$V, plotted by interpolation, if not available at the desired value of V_{CE}

$$h_{ie} = \left.\frac{\Delta v_{BE}}{\Delta i_B}\right|_{V_{CE}} = \left.\frac{(730 - 715)\,\text{mV}}{(20 - 10)\,\mu\text{A}}\right|_{V_{CE} = 8.4\,\text{V}} = 1.5\ \text{k}\Omega$$

The value of h_{re} can similarly be computed using its definition. For higher accuracy, the changes about the Q-point should be made as small as possible.

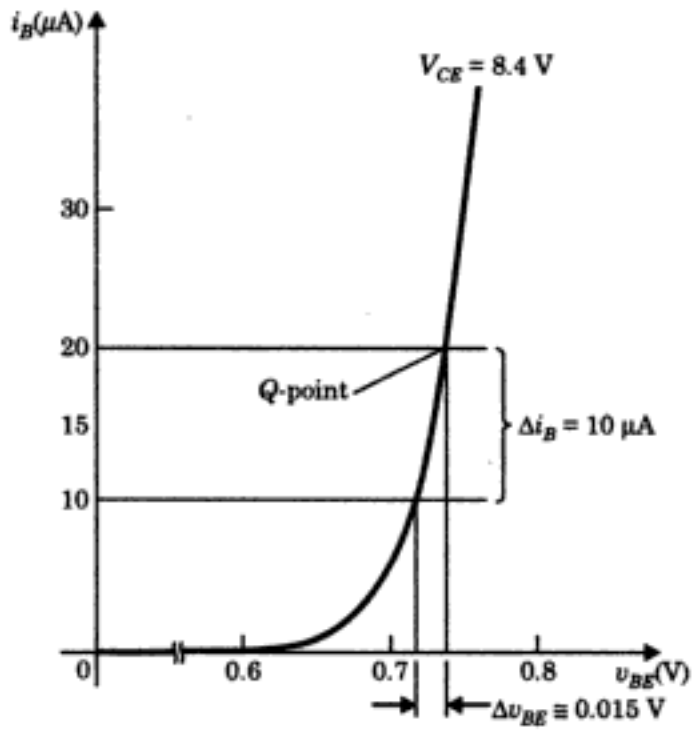


Fig. 6.6(b) Computing h_{ie} and h_{re} from the input characteristics.

There are two important facts which need to be mentioned about the h-parameters. Firstly, that the values of h-parameters depend upon the Q-point and secondly, h-parameters vary with temperature. Most of the transistor specification sheets provide curves giving the variation of h-parameters with the collector current and junction temperature.

It may further be emphasized that the h-parameter model of the transistor as its ac equivalent circuit is valid only for small input signals. The ac input signal should be small enough so that the variation of voltages/currents about the Q-point are sufficiently small. Then only the transistor parameters can be assumed to be constant over the signal excursion.

The use of h-parameters model as ac equivalent circuit of transistor has many advantages. The h-parameters are:

1. real numbers at audio frequencies (as all the internal capacitances of a transistor are sufficiently low and can be neglected at low frequencies)

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2. easy to measure experimentally
3. can be computed from transistor static characteristics.

The manufacturers usually specify *h*-parameters in data sheets and this is one reason that *h*-parameter model is extensively used for circuit analysis and design. Table 6.1 gives the values of *h*-parameters of a typical transistor in *CE*, *CC* and *CB* configurations.

Table 6.1 Typical *h*-parameter values for a transistor (at I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kHz)

Parameter	*CE*	*CC*	*CB*
$h_{11} = h_i$	1100 Ω	1100 Ω	21.6 Ω
$h_{12} = h_r$	2.5×10^{-4}	~1	2.9×10^{-4}
$h_{21} = h_f$	50	–51	–0.98
$h_{22} = h_o$	24 μA/V	25 μA/V	0.49 μA/V
$1/h_o$	40 K	40 K	2.04 M

Some of the transistor manufacturers specify all the four *CE*-*h*-parameters only, whereas others specify mixed parameters h_{fe}, h_{ib}, h_{ob} and h_{rb}. Given any four *h*-parameters, it is possible to compute the other parameters by the conversion formulas given in Table 6.2. These formulas can be easily verified by using the definition of the parameters and Kirchoff's laws. The exact conversion formulas are quite complicated and for all practical purposes, it is sufficient to use only the approximate conversion formulas of Table 6.2.

Table 6.2 Approximate Conversion Formulas for *h*-Parameters

1	*CE* to *CC*	$h_{ic} = h_{ie}$; $h_{rc} = 1$ $h_{fc} = -(1 + h_{fe})$; $h_{oc} = h_{oe}$
2	*CE* to *CB*	$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$ †; $h_{rb} = \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$ $h_{fb} = -\frac{h_{fe}}{1+h_{fe}}$; $h_{ob} = \frac{h_{oe}}{1+h_{fe}}$

EXAMPLE 6.1

Prove the *CE* to *CC* *h*-parameters conversion formulae given in Table 6.2.

Solution: In order to derive the conversion formulae, the *CE* *h*-parameter model is shown again in Fig. 6.7(a) to simplify the analysis. Now, by using the definitions of the *CC* *h*-parameters from Fig. 6.7(b) perform the computation as shown.

†The *CE* parameters in terms of the *CB* parameters are obtained by interchanging the subscripts *b* and *e*.

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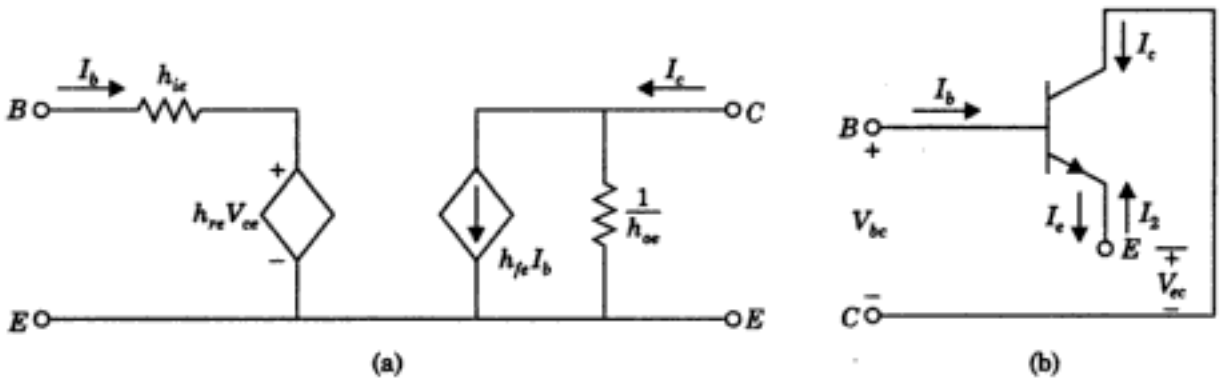


Fig. 6.7 (a) *CE* h-parameter model, (b) A transistor in *CC* configuration.

By definition, from Fig. 6.7(b),

$$h_{ic} = \left.\frac{V_{bc}}{I_b}\right|_{V_{ec}=0}$$

If we short the output terminals C and E in Fig. 6.7(a) so as to make $V_{ec} = 0$, it is easily seen that the collector terminal C is at the same potential as E. Further, with $V_{ce} = 0$, $h_{re}V_{ce}$ is also zero. So, we may write that

$$h_{ic} = h_{ie}$$

Similarly,

$$h_{fc} = \left.\frac{-I_e}{I_b}\right|_{V_{ec}=0} \qquad (I_2 = -I_e \text{ for } CC \text{ mode})$$

$$= -\left.\frac{(I_c + I_b)}{I_b}\right|_{V_{ec}=0}$$

From Fig. 6.7(a), for $V_{ce} = 0$, $I_c = h_{fe}I_b$.

Therefore,

$$h_{fc} = -\left.\frac{(h_{fe}I_b + I_b)}{I_b}\right|_{V_{ec}=0}$$

$$= -(1 + h_{fe})$$

Now,

$$h_{rc} = \left.\frac{V_{bc}}{V_{ec}}\right|_{I_b=0} \qquad \text{(for CC mode)}$$

$$= \left.\frac{(V_{be} + V_{ec})}{V_{ec}}\right|_{I_b=0} = \left.\left(1 + \frac{V_{be}}{V_{ec}}\right)\right|_{I_b=0}$$

or

$$h_{rc} = \left.\left(1 - \frac{V_{be}}{V_{ce}}\right)\right|_{I_b=0} \qquad (V_{ec} = -V_{ce})$$

$$= 1 - h_{re} \simeq 1 \qquad \text{(using definition of } h_{re})$$

The value of h_{re} is usually very small (2.5×10^{-4}) and hence can be neglected.

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Finally, $$h_{oc} = \frac{I_2}{V_{ec}}\bigg|_{I_b=0} = -\frac{I_e}{V_{ec}}\bigg|_{I_b=0}$$

$$= -\frac{(I_c + I_b)}{V_{ec}}\bigg|_{I_b=0} = -\frac{I_c}{V_{ec}}\bigg|_{I_b=0} = \frac{I_c}{V_{ce}}\bigg|_{I_b=0} \qquad (V_{ec} - V_{ce})$$

which is equal to h_{oe}.

So $$h_{oc} = h_{oe}$$

Thus, we can summarize:

$$h_{ic} = h_{ie}\ ; \quad h_{rc} = 1 - h_{re} \simeq 1$$

$$h_{fc} = -(1 + h_{fe}); \quad h_{oc} = h_{oe}$$

Hence proved.

6.2.2 Hybrid-π Model

The hybrid-π model is a very widely used model developed for a BJT in *CE* configuration and is shown in Fig. 6.8. The parameters g_m and r_π in this model depend upon the value of dc quiescent current I_{CQ} and hence provide more accurate analysis of the transistor. The model is applicable to both pnp and npn transistors without change of polarities.

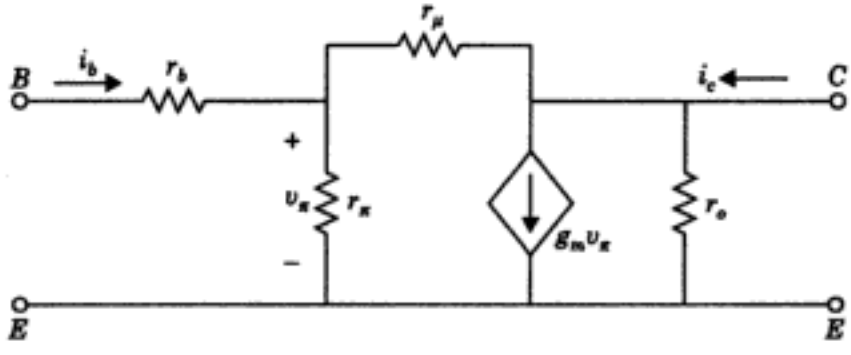


Fig. 6.8 Hybrid-π model of a transistor in *CE* configuration, at low frequencies.

In this model, transistor is represented as a voltage controlled current source. The significance of the various elements in this model is:

r_b = is called the base spreading resistance and is the ohmic resistance of the base region. Base region of the transistor is very thin compared to the emitter and collector regions and its resistance lies between 40 to 400 Ω. The ohmic resistance of the emitter/collector is usually of the order of 10 Ω and can be neglected in comparison to that of base region.

r_π = represents the incremental resistance of the emitter-base diode which is forward-biased in the active region of operation. (The incremental resistance for forward biased diode was denoted by r_d).

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r_μ = accounts for the feedback from output to input due to base width modulation or early effect. The value of r_μ is usually very high (several mega ohms) and will be neglected in the analysis henceforth.

r_o = is the output resistance and is also due to early effect. Its value is given by $r_o = V_A/I_{CQ}$ where V_A is the early voltage and I_{CQ} is the collector dc quiescent current. Typical values of r_o are tens of kilohms to hundreds of kilohms.

$g_m v_\pi$ = any small signal voltage v_π at the emitter junction results in a signal collector current $g_m v_\pi$ when collector is shorted to emitter (for ac conditions). BJT is represented as a voltage controlled current source, where controlled current is $g_m v_\pi$, the controlling voltage is v_π and g_m represents the transconductance of the transistor.

An alternative hybrid-π model can be developed by expressing the controlled current source ($g_m v_\pi$) in terms of the input base current i_b. In Fig. 6.8, it can be seen that

$$v_\pi = i_b r_\pi \tag{6.18}$$

For $v_{ce} = 0$, that is under short circuit conditions at the output,

$$i_c = g_m v_\pi \quad \text{(as } r_0 \text{ is shorted)} \tag{6.19}$$
$$= g_m r_\pi i_b$$

or
$$\frac{i_c}{i_b} = g_m r_\pi \tag{6.20}$$

Here, a new parameter β_0 is introduced as:

$$\beta_o = \frac{\Delta i_C}{\Delta i_B}_{V_{CE} = \text{constant} = V_{CEQ}} \tag{6.21}$$

$$= \frac{i_c}{i_b}_{v_{ce} = 0^*} \tag{6.22}$$

Thus, $\beta_0 = r_\pi g_m$

and $i_c = \beta_0 i_b$

The parameter β_0 is called the **ac common emitter forward short circuit current gain** and is the same as h_{fe} in the *CE* h-parameter model. The alternate hybrid-π model is shown in Fig. 6.9. In this model, transistor is represented as a current controlled current source, with the controlling current being i_b, and the controlled current $\beta_0 i_b$. The feed back resistance r_μ is usually very high and is neglected in general. The use of this model simplifies the analysis as we shall see later.

*It may be mentioned here that there is no physical short circuit between the output terminals. It only means that there are no incremental changes and V_{CE} is constant.

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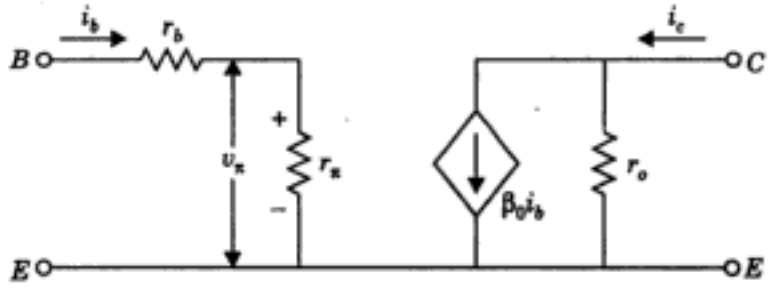


Fig. 6.9 An alternate hybrid-π model which represents BJT as a current controlled current source.

Transconductance g_m: The parameter g_m, gives the incremental change in collector current i_C about the operating point produced by incremental charge in the base emitter voltage v_{BE}. Thus, g_m can be expressed as,

$$g_m = \left.\frac{\Delta i_C}{\Delta V_{BE}}\right|_{v_{ce}=0} = \frac{i_c}{v_{be}} \tag{6.23}$$

Consider an ac signal v_{be} applied at the input of an npn transistor biased for active region of operation as shown in Fig. 6.10.

The total instantaneous base-emitter voltage v_{BE} is:

$$v_{BE} = V_{BE} + v_{be}$$

The collector current is given by

$$i_C = I_s e^{v_{BE}/V_T}$$

$$= I_s e^{(V_{BE}/V_T)} e^{v_{be}/V_T} \tag{6.24}$$

Here dc collector current I_{CQ} is:

$$I_{CQ} = I_C = I_s e^{V_{BE}/V_T} \tag{6.25}$$

So Eqn. (6.24) can be written as:

$$i_C = I_{CQ} e^{v_{be}/V_T} \tag{6.26}$$

For $v_{be} << V_T$, we may approximate Eq. (6.26) as:

$$i_C \simeq I_{CQ}\left(1 + \frac{v_{be}}{V_T}\right) \tag{6.27}$$

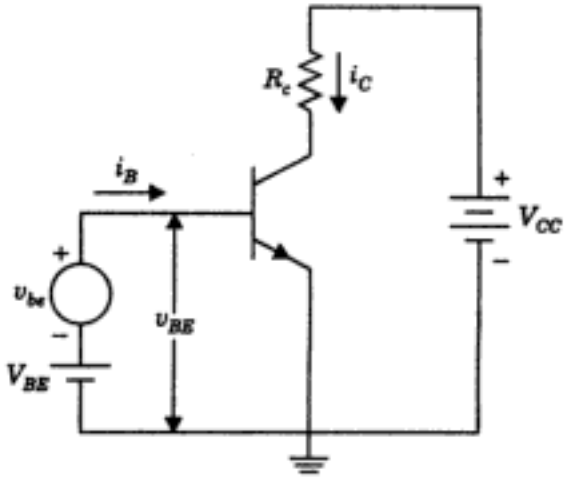


Fig. 6.10 An npn transists amplifier for computation of g_m, transconductance.

where we have retained only the first two terms of the exponential expansion. This approximation is valid only for v_{be} less than about 10 mV and is referred to as small signal approximation. Thus, Eq. (6.27) can be rewritten as:

$$i_C = I_{CQ} + \frac{I_{CQ}}{V_T} v_{be} \tag{6.28}$$

The collector current has two components, the dc bias current I_{CQ} and the signal component i_c, where

$$i_c = \frac{I_{CQ}}{V_T} v_{be} \tag{6.29}$$

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Using Eqn. (6.23), the value of the **transconductance** is given by

$$g_m = \frac{I_{CQ}}{V_T} \tag{6.30}$$

At room temperature (T = 293 K), $V_T = T/11{,}600 = 25$ mV,

$$g_m = \frac{I_{CQ}\,(\text{mA})}{25} \tag{6.31}$$

EXAMPLE 6.2

A BJT is operating at a base current of 7.6 μA and a β_0 of 104. Find the values of r_π and g_m.

Solution: Given I_{BQ} = 7.6 μA

Therefore, $I_{CQ} = \beta_0 I_{BQ}$

$= 104 \times 7.6 = 790.4$ μA

and $g_m = \dfrac{I_{CQ}}{V_T}$

So $g_m = \dfrac{790.4}{25} = 31.6$ mA/V $\quad (V_T = 25$ mV]

Also $r_\pi = \dfrac{\beta_0}{g_m} = \dfrac{104}{31.6} = 3.28$ kΩ

6.2.3 r_e-Model (T-Model)

Although h-parameter model or hybrid-π model can be used to carry out small signal analysis of all types of transistor circuits, there are situations in which r_e-model is found to be more convenient for the analysis. Figure 6.11 shows the two versions of r_e-model used. The model of Fig. 6.11(a) represents the BJT as a voltage controlled current source given by $g_m V_{be}$ with the control voltage v_{be}. The resistance r_e in the model represents the ac incremental (dynamic) resistance of the emitter base diode which is forward biased and depends upon the dc emitter current I_{EQ} and is given by

$$r_e = \frac{V_T}{I_{EQ}}\ * \tag{6.32}$$

*Note that for the case of diodes we have found that (see Eq. 2.22)

$$r_d = \frac{\eta V_T}{I_{DQ}}$$

For the case of BJTs we always assume $\eta = 1$, and here the diode current I_{DQ} (at quiescent point) is replaced by I_E and r_d renamed as r_e giving us

$$r_e = \frac{V_T}{I_E}$$

Clearly, r_e depends on the voltage V_T (and, therefore, on temperature T) and the quiescent current I_{EQ} (since I_E implies DC part of the net emitter current that is the quiescent value of the total emitter current).

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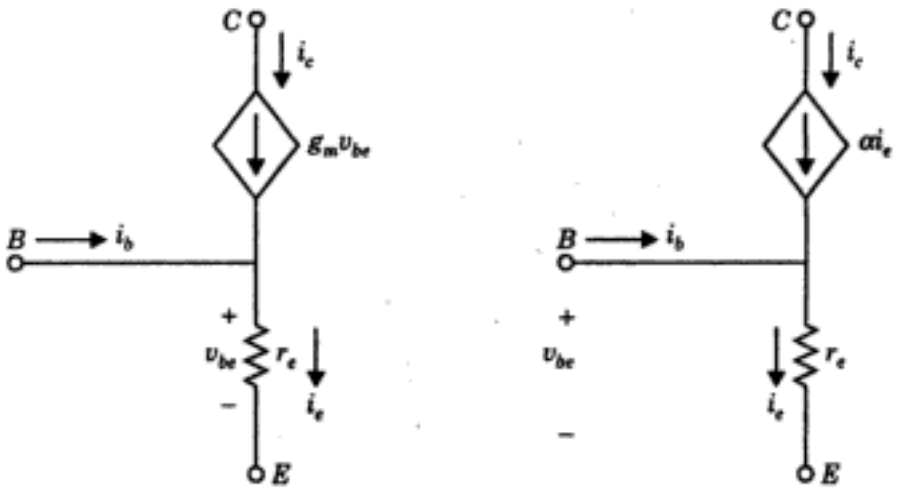


Fig. 6.11(a) Two versions of r_e-model (a) voltage controlled current source representation, (b) current controlled current source representation.

and
$$g_m = \frac{I_{CQ}}{V_T} \tag{6.33}$$

Another version of the r_c model can be obtained if $g_m v_{be}$ is expressed in terms of the emitter current as

$$g_m v_{be} = g_m (r_e i_e) = \left(\frac{I_{CQ}}{V_T}\right)\left(\frac{V_T}{I_{EQ}}\right) i_e$$

$$= \frac{I_{CQ}}{I_{EQ}} i_e = \alpha i_e \tag{6.34}$$

The alternative r_e-model is shown in Fig. 6.11(b) where transistor is represented as a current controlled current sources. There is one more popular r_e-model for a transistor in *CE* configuration and is shown in Fig. 6.11(c). The derivation of the model is obtained as follows:

In Fig. 6.11(a), the current i_e is given by

$$i_e = i_b + i_c$$

$$i_e = i_b + \beta_o i_b \qquad (\text{using } i_c = \beta_o i_b)$$

$$= (1 + \beta_o) i_b$$

$$\simeq \beta_o i_b \qquad (\text{for } \beta_o >> 1) \tag{6.35}$$

Further,
$$v_{be} = i_e r_e = \beta_o i_b r_e \tag{6.36}$$

Therefore, the input resistance R_i is:

$$R_i = \frac{v_{be}}{i_b} = \frac{\beta_o i_b r_e}{i_b}$$

$$= \beta_o r_e \tag{6.37}$$

Using the fact that the input impedance is $\beta_o r_e$, and that the collector current is $\beta_o i_b$, equivalent model for the transistor in *CE* configuration may be shown as in Fig. 6.11(c).

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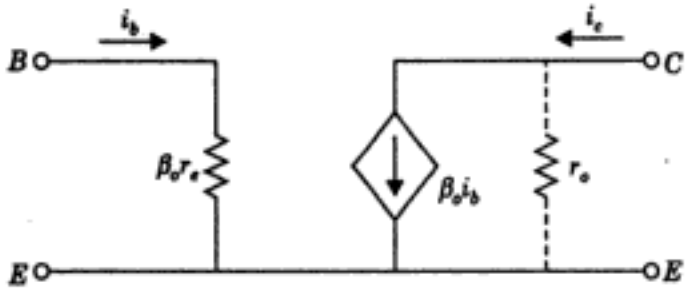


Fig. 6.11(c) Another popular version of r_e-model.

In the various versions of r_e-model, the output resistance r_o has not been included. If the value of r_o is available, then it can be included in the analysis as shown by dotted r_o in Fig. 6.11(c). It can further be seen that r_e-model given in Fig. 6.11(c) is similar to the hybrid-π model of Fig. 6.9. As

$$\beta_o r_e = \frac{\beta_o V_T}{I_{EQ}} = \frac{\beta_o V_T}{I_{CQ}} = \frac{\beta_o}{g_m} = r_\pi$$

The value of r_b in hybrid-π model is usually very small compared to r_π and is neglected. Thus both these models are same basically.

High Frequency Model of BJT

The various models discussed earlier for a BJT are suitable at the audio range of frequencies where the internal capacitance of a BJT can be neglected. It is assumed that transistor action is instantaneous and the output appears as soon as the input signal is applied. However, transistors exhibit charge storage phenomenon that limits the speed and frequency of operation. We have earlier seen in the study of *pn* junctions that two types of capacitances that is diffusion capacitance (C_D) and transition capacitance (C_T) are associated with it. These capacitances must be included in the BJT model at high frequencies. Figure 6.12 shows the hybrid-π model of a BJT valid for high frequencies. The capacitance C_π is due to the forward-biased emitter-base junction ($\therefore$ diffusion capacitance) and is of the order of 3–10 pFs. The capacitance C_μ represents the transition capacitance due to the reversed-biased collector-base junction and is usually smaller than C_π (<1 pF).

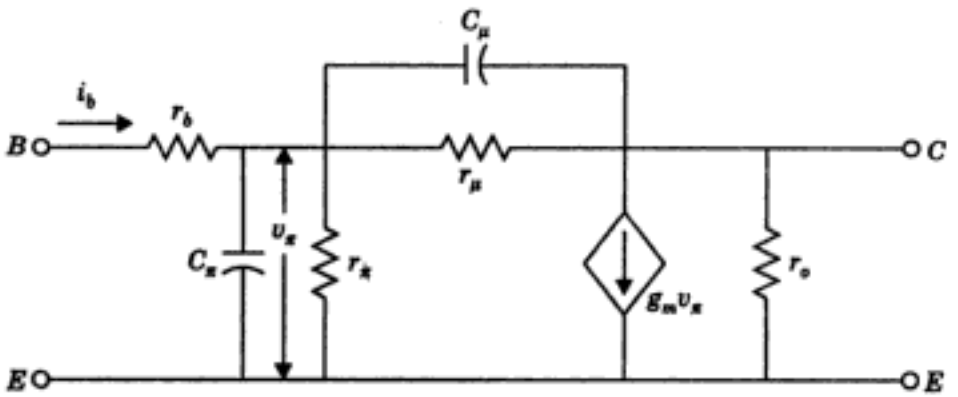


Fig. 6.12 High frequency model of a BJT.

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6.3 GRAPHICAL ANALYSIS OF A *CE* AMPLIFIER

The ac analysis of a transistor amplifier can be done by using any of the small signal models discussed in Section 6.2. However, it is illustrative to study the operation of a simple transistor amplifier circuit graphically. Although the graphical method is seldom used for analysis and design being lengthy and cumbersome, yet it gives a lot of insight into the operation of a transistor as an amplifier.

Consider a simple *CE* amplifier stage shown in Fig. 6.13(a). First consider the case when input signal $v_i = 0$. The desired base current is established by the base supply voltage V_{BB} and the resistance R_B. The dc base current (for $v_i = 0$) is obtained graphically from the input characteristics of a BJT drawn between v_{BE} and i_B as shown in Fig. 6.13(b). The intersection of the load line having a slope of $-1/R_B$ with the input characteristics gives the dc base current I_{BQ} (i.e., the quiescent base current).

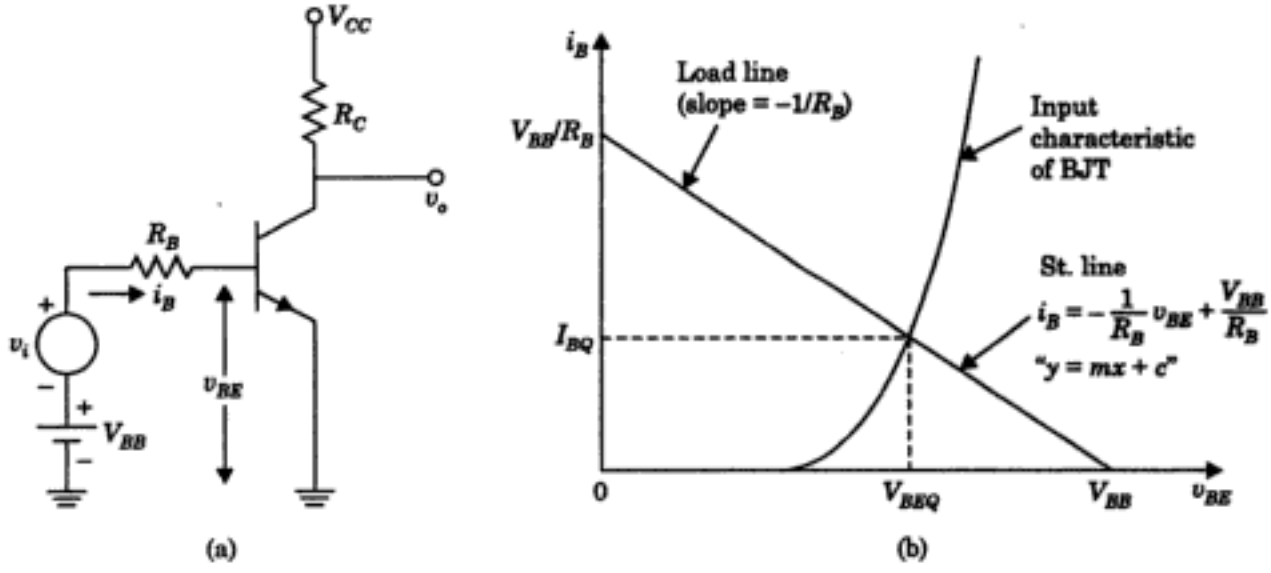


Fig. 6.13 (a) *CE* amplifier, (b) Finding the quiescent base current (I_{BQ}) graphically.

Having determined the value of base current I_{BQ}, the Q-point is now located on i_C–v_{CE} characteristics of the BJT as shown in Fig. 6.14. For the given load R_C, the load line is drawn from the collector circuit equation

$$v_{CE} = V_{CC} - i_C R_C$$

or

$$i_C = \frac{V_{CC}}{R_C} - \frac{1}{R_C} v_{CE} \tag{6.38}$$

which represents a straight line of slope $-1/R_C$. The Q-point is at the intersection of the load line with the i_C–v_{CE} curve corresponding to the base current I_{BQ}.

The co-ordinates of the Q-point gives the dc collector current I_{CQ} and collector to emitter voltage V_{CEQ}. For proper amplifier operation, Q-point should be in the active region and should be located in the centre so as to obtain maximum signal swing when input signal v_i is applied to the base of the amplifier.

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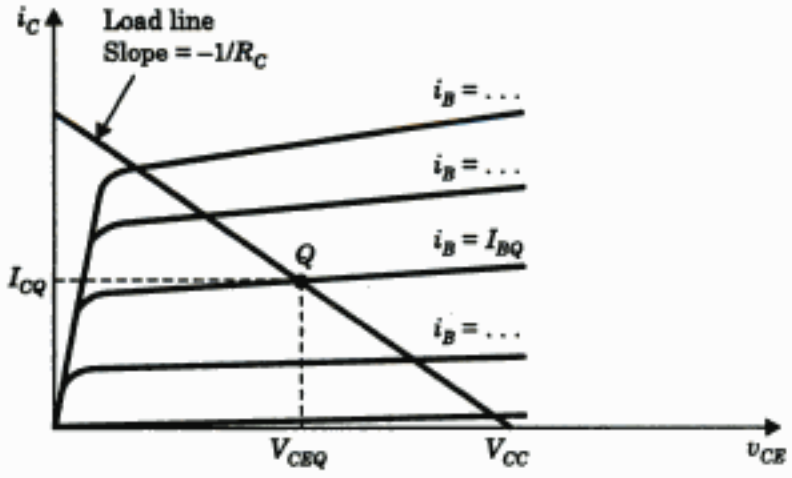


Fig. 6.14 Finding the Q-point (i.e., I_{CQ} and V_{CEQ}) graphically.

Now consider the case when ac signal v_i is applied. The sinusoidal signal v_i is thus superimposed on the dc voltage V_{BB} as shown in the input characteristics of Fig. 6.15(a). Corresponding to each value of $V_{BB} + v_i(t)$, one can draw a straight line with a slope $-1/R_B$. As an example, in Fig. 6.15(a) straight lines corresponding to $v_i = 0$, $v_i = V_{max}$ and $v_i = V_{min}$ have been shown. Now, if the amplitude of v_i is sufficiently small then the Q-point moves over an almost linear portion of the i_B–v_{BE} curve resulting in sinusoidal signals i_b and v_{be} as shown in figure. It basically means that for small signals, a sinusoidal input signal v_i produces a sinusoidal base current i_b, and no distortion is produced.

Now, coming to i_C–v_{CE} characteristics of Fig. 6.15(b), the Q-point will move along the load line of slope $-1/R_C$ as base current changes from i_{B2} to i_{B1}. Taking the projections as shown in Fig. 6.15(b), signal components i_c and v_{ce} are obtained. It may be noted that v_{ce} waveform is 180° shifted (lagging) from the input signal v_i. A small value of input signal v_i will produce large value of v_{ce} and the ratio. v_{ce}/v_i provides the gain of the amplifier. As can be seen, graphical analysis is quite cumbersome and its use is not practical for analysis and design of circuits. However, it gives a good insight of operation of a BJT and explain the need of having small input signal v_i.

6.4 ANALYSIS OF TRANSISTOR AMPLIFIER CIRCUITS USING SMALL SIGNAL EQUIVALENT CIRCUITS

A BJT can be used as an amplifier in three different configurations, i.e. *CE*, *CC* and *CB*. Whatever may be the type of amplifier, in general, there are four quantities of interest in any amplifier: A_I, R_i, A_V and R_o, that is, current gain, input impedance, voltage gain and output impedance, respectively. It has been emphasized earlier that a transistor is biased in the active region using various biasing techniques so as to get a distortion free output signal. We are, however, interested in finding only the ac values of gains and impedances. Therefore, an ac equivalent circuit is obtained by replacing all the dc voltage supplies by short circuits. The dc levels are important for determining the Q-point and once the Q-point has been determined, the dc levels can simply be ignored. In addition, all the coupling capacitors and by-pass capacitors are usually chosen high and, therefore, have very low reactance at the signal frequency of interest. The coupling and by-pass capacitors can, therefore, be assumed to be short circuit.

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So
$$I_o = -(h_{fe}I_b + h_{oe}R_C I_o) \tag{6.42}$$

Solving for A_I, gives
$$A_I = \frac{I_o}{I_b} = -\frac{h_{fe}}{1 + h_{oe}R_C} \tag{6.43}$$

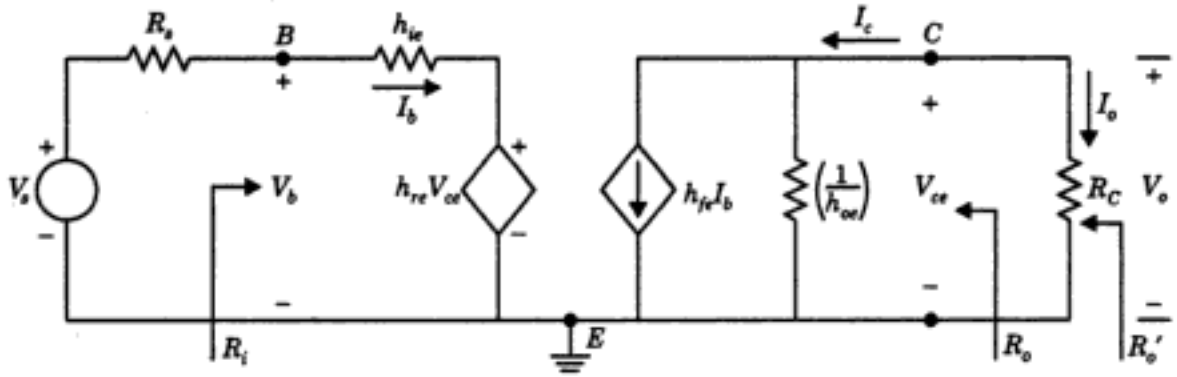


Fig. 6.17 AC equivalent circuit of the *CE* amplifier of Fig. 6.16.

Input resistance R_i

The resistance seen looking into the input terminals or the base gives the input resistance of the amplifer, that is,
$$R_i = \frac{V_b}{I_b} \tag{6.44}$$

From the input circuit in Fig. 6.17,
$$V_b = h_{ie}I_b + h_{re}V_{ce} \tag{6.45}$$

Also
$$V_{ce} = I_o R_C = A_i I_b R_C \tag{6.46}$$

Putting the value of V_{ce} from Eq. (6.46) in Eq. (6.45) we obtain
$$V_b = h_{ie}I_b + h_{re}A_I I_b R_C$$

So
$$R_i = \frac{V_b}{I_b} = h_{ie} + h_{re}A_I R_C \tag{6.47}$$

Voltage gains, A_V and A_{V_s}

The voltage gain of an amplifier can be defined with or without source resistance R_s taken into account. Thus,
$$A_V = \frac{V_o}{V_b} \quad \text{(also called } \textbf{transducer voltage gain}\text{)} \tag{6.48}$$

and
$$A_{V_s} = \frac{V_o}{V_s} \quad \left(\begin{array}{l}\text{also } \textbf{called overall voltage gain} \text{ or the} \\ \text{voltage gain taking source resistance}\end{array}\right) \tag{6.49}$$

In Fig. 6.17,
$$V_o = I_o R_C$$

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and $$V_b = I_b R_i$$

Therefore, $$A_V = \frac{V_o}{V_b} = \frac{I_o R_C}{I_b R_i} = A_I \frac{R_C}{R_i} \quad (6.50)$$

The overall voltage gain A_{V_s} is given by

$$A_{V_s} = \frac{V_o}{V_s} = \frac{V_o}{V_b} \cdot \frac{V_b}{V_s} \quad (6.51)$$

The ratio V_b/V_s is obtained from the equivalent input circuit of the amplifier shown in Fig. 6.18.

Using voltage divider rule in Fig. 6.18, we get

$$\frac{V_b}{V_s} = \frac{R_i}{R_s + R_i} \quad (6.52)$$

Thus, $$A_{V_s} = A_V \frac{R_i}{R_s + R_C} \quad (6.53)$$

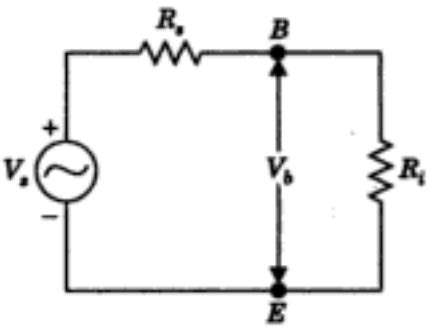


Fig. 6.18 Equivalent input circuit for computing V_b/V_s.

The overall voltage gain A_{V_s} is of more importance and is usually much less than A_V on account of appreciable voltage drop of input signal across the source resistance R_s. For example, if $R_s = R_i$ then

$$A_{V_s} = 0.5 A_V$$

It can be seen that half of the input signal voltage is lost as voltage drop across the source resistance R_s.

Current gain A_{I_s}

If the input signal is a current source I_s with resistance R_s which is the Norton's equivalent of the voltage source as shown in Fig. 6.19 then the overall current gain A_{I_s} is given by

$$A_{I_s} = \frac{I_o}{I_s}$$

$$= \frac{I_o}{I_b} \cdot \frac{I_b}{I_s} \quad (6.54)$$

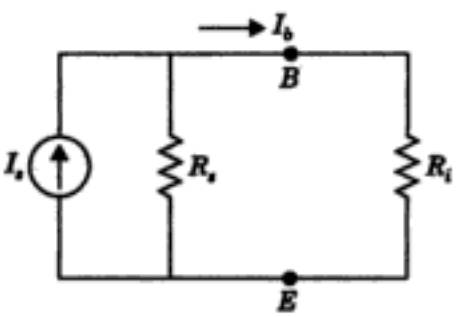


Fig. 6.19 Norton's equivalent of voltage source.

Using the current divider rule in Fig. 6.19,

$$\frac{I_b}{I_s} = \frac{R_s}{R_s + R_i} \quad (6.55)$$

Hence, $$A_{I_s} = A_I \frac{R_s}{R_s + R_i} \quad (6.56)$$

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Output resistances R_o and R_o'

The resistances R_o and R_o' are the resistances seen at the output terminals of an amplifer without and with load R_C taken into account, respectively. The output resistance $R_o = 1/Y_o$ is determined by setting the input signal $V_s = 0$ (but taking R_s into account) and load resistance $R_C = \infty$ in Fig. 6.17. The resulting circuit shown in Fig. 6.20 is now driven by an external voltage source V_2, and current I_2 drawn by the circuit is determined so as to compute output resistance R_o.

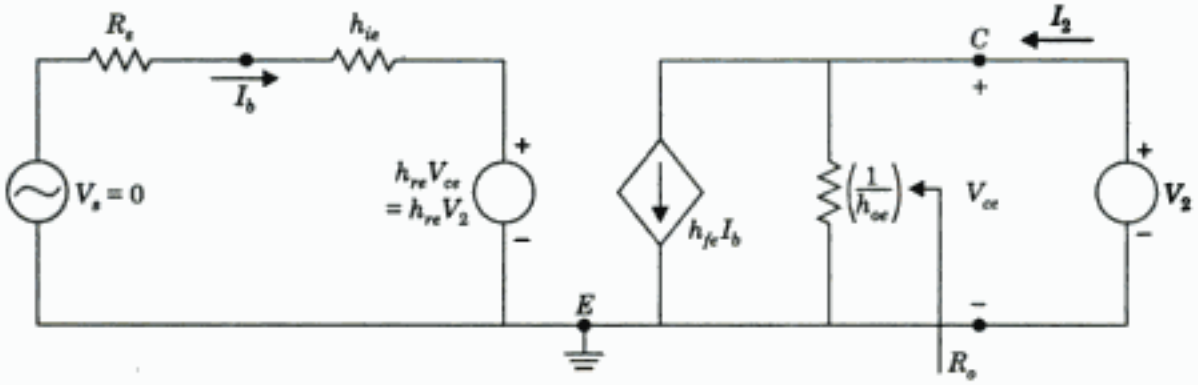


Fig. 6.20 Equivalent circuit for computing R_o.

In Fig. 6.20 with $V_s = 0$, KVL for the input loop gives

$$R_s I_b + h_{ie} I_b + h_{re} V_2 = 0 \qquad \text{(Since } V_{ce} = V_2\text{)}$$

Simplifying

$$I_b = \frac{-h_{re} V_2}{R_s + h_{ie}} \tag{6.57}$$

From the output circuit, we may write

$$I_2 = h_{fe} I_b + h_{oe} V_2 \tag{6.58}$$

Putting the value of I_b from Eq. (6.57) to Eq. (6.58), we get

$$I_2 = \frac{-h_{fe} h_{re} V_2}{R_s + h_{ie}} + h_{oe} V_2 \tag{6.59}$$

Solving for $Y_o = I_2/V_2$, we obtain

$$Y_o = h_{oe} - \frac{h_{fe} h_{re}}{R_s + h_{ie}} \tag{6.60}$$

In this derivation, we have not taken load resistance R_C into account. If R_C is included then the output resistance R_o' is given as:

$$R_o' = R_C \| R_o \tag{6.61}$$

All the formulas derived for a *CE* amplifier are summarized in Table 6.3.

Table 6.3 Important Formulae for a *CE*-amplifier

$A_I = -\dfrac{h_{fe}}{1 + h_{oe}R_C}$	$A_{Vs} = \dfrac{A_V R_i}{R_i + R_s} = \dfrac{A_I R_C}{R_i + R_s}$
$R_i = h_{ie} + h_{re}A_I R_C$	$A_{Is} = \dfrac{A_i R_s}{R_i + R_s}$
$A_V = \dfrac{A_I R_C}{R_i}$	$Y_o = \dfrac{1}{R_o} = h_{oe} - \dfrac{h_{fe}h_{re}}{h_{ie} + R_s}$

The analysis above has been done for a *CE* amplifier. In a similar manner, one can perform the analysis for a *CC* or *CB* amplifier by using the *h*-model valid for the configuration. It can be seen that all the formulae given in Table 6.3 are valid for a *CC* or *CB* amplifier only if we change the subscript *e* to *c* for CC and *e* to *b* for CB, respectively for all the *h*-parameters used.

Output impedance using short circuit current/open circuit voltage method. For some of the complicated circuits, it is found more convenient to determine R_o and R_o' by an alternate method called the **short circuit current and open circuit voltage method.**

Any two-terminal network can be represented by its Thevenin's equivalent circuit shown in Fig. 6.21(a) where V_{oc} represents the open circuit voltage at the output terminals, and R_o is the output resistance seen at the terminals 1 and 2. The network can also be represented by the Norton's equivalent circuit shown in Fig. 6.21(b) where a short circuit current source I_{sc} is in parallel with the output resistance R_o. The output resistance can be given by

Since $$I_{sc} = \frac{V_{oc}}{R_o}$$

Therefore, $$R_o = \frac{V_{oc}}{I_{sc}} \qquad (6.62)$$

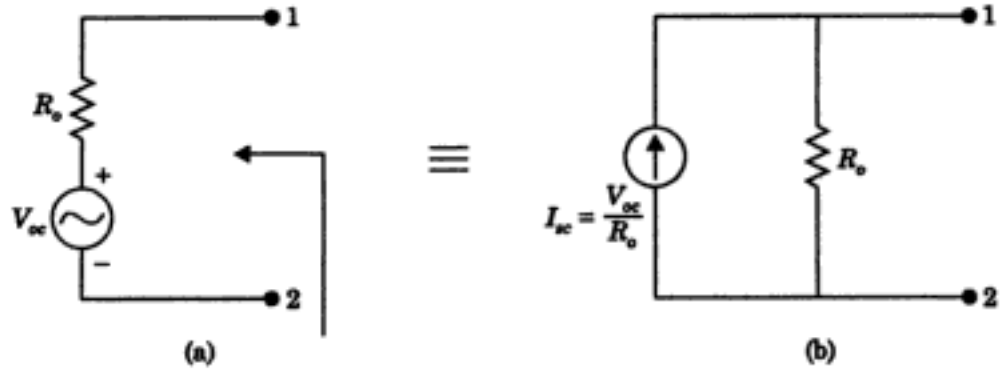


Fig. 6.21 (a) Thevenin's equivalent circuit (b) Norton's equivalent circuit.

We now show the use of this method for finding the output resistances R_o and R_o' for a *CE* amplifier. Note that in this method of analysis, we will not set $V_s = 0$.

In the ac equivalent circuit of *CE* amplifier shown in Fig. 6.17, if the output is short circuited by making $V_o = 0$ then output circuit reduces to as shown in Fig. 6.21(c).

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The short circuit current now is

$$I_{sc} = -h_{fe} I_b \tag{6.63}$$

and from the input loop in Fig. 6.17, we get

$$I_b = \frac{V_s}{R_s + h_{ie}} \quad (h_{re} V_{ce} = h_{re} V_o = 0) \tag{6.64}$$

Substituting the value of I_b from Eq. 6.64 into Eq. 6.63, we get

$$I_{sc} = \frac{-h_{fe} V_s}{R_s + h_{ie}} \tag{6.65}$$

Under open circuit conditions at the output, i.e. for $R_C = \infty$

$$V_{oc} = -h_{fe} I_b \times \frac{1}{h_{oe}} \tag{6.66}$$

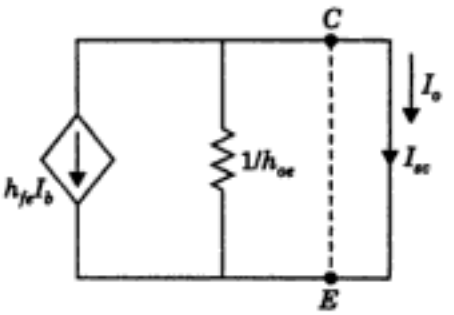


Fig. 6.21(c) Output circuit when $V_o = 0$ (short circuit case)

From the input loop,

$$V_s = I_b(R_s + h_{ie}) + h_{re} V_{oc} \tag{6.67}$$

Putting the value of I_b from Eq. (6.66) to Eq. (6.67), we get

$$V_s = -\frac{h_{oe} V_{oc}}{h_{fe}} (R_s + h_{ie}) + h_{re} V_{oc} \tag{6.68}$$

$$= V_{oc} \left[-\frac{h_{oe}}{h_{fe}} (R_s + h_{re}) + h_{re} \right]$$

$$\therefore \quad \frac{1}{V_{oc}} = \frac{1}{V_s} \left[-\frac{h_{oe}}{h_{fe}} (R_s + h_{ie}) + h_{re} \right] \tag{6.68a}$$

From Eq. (6.65) and Eq. (6.68a), we get

$$Y_o = \frac{I_{sc}}{V_{oc}} = h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}} \tag{6.69}$$

which is same as Eq. (6.60).

EXAMPLE 6.3

The h-parameters of a transistor used in CE amplifier are given as: $h_{ie} = 1$ kΩ; $h_{fe} = 100$, $h_{re} = 2 \times 10^{-4}$ and $h_{oe} = 20$ μA/V. If $R_C = 5$ kΩ and $R_s = 1$ kΩ, determine A_I, R_I, A_V, A_{Vs}, R_o and R_o'.

Solution: Using exact formulae from Table 6.3,

$$A_I = \frac{-h_{fe}}{1 + h_{oe} R_C}$$

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$$= \frac{-100}{1 + 20 \times 10^{-6} \times 5 \times 10^{3}} = \frac{100}{1 + .1} = -90.9$$

$$R_i = h_{ie} + h_{re} A_I R_C$$

$$= 1 - 20 \times 10^{-6} \times 90.9 \times 5$$

$$= 1 - .0909 = 0.909 \text{ k}\Omega$$

(Note that R_i will always be less than h_{ie} for the basic CE amplifier)

$$A_V = \frac{A_I R_C}{R_i}$$

$$= -\frac{90.9 \times 5}{.909} = -500$$

The negative sign in voltage gain indicates that there is 180° phase shift between input and output voltage waveforms.

$$A_{Vs} = \frac{A_V R_i}{R_i + R_s}$$

$$= -\frac{500 \times .909}{1.909} = -238.08$$

$$A_{Is} = A_I \frac{R_s}{R_s + R_i}$$

$$= -90.9 \frac{1}{1.909} = -47.6$$

$$Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s}$$

$$= 20 \times 10^{-6} - \frac{100 \times 2 \times 10^{-4}}{(1 + 1)}$$

$$= 20 \times 10^{-6} - 10^{-2} \simeq 20 \times 10^{-6}$$ (Note that $Y_o \simeq h_{oe}$)

Therefore, $$R_o = \frac{1}{Y_o} = \frac{1}{20 \times 10^{-6}} = 50 \text{ k}\Omega$$

and $$R_o' = R_o \| R_C = 50 \text{ k} \| 5 \text{ k} = 4.54 \text{ k}\Omega$$

EXAMPLE 6.4

The transistor in the amplifier shown in Fig. 6.22(a) has the following parameters:

$$h_{ie} = 2 \text{ k}\Omega;\ h_{fe} = 50;\ h_{re} = 2 \times 10^{-4} \text{ and } h_{oe} = 20 \times 10^{-6} \text{ A/V}$$

determine: $A_I' = \frac{I_o}{I_s}$, $A_{Vs} = \frac{V_o}{V_s}$, $R_{i,\text{eff}}$, R_o and R_o'.

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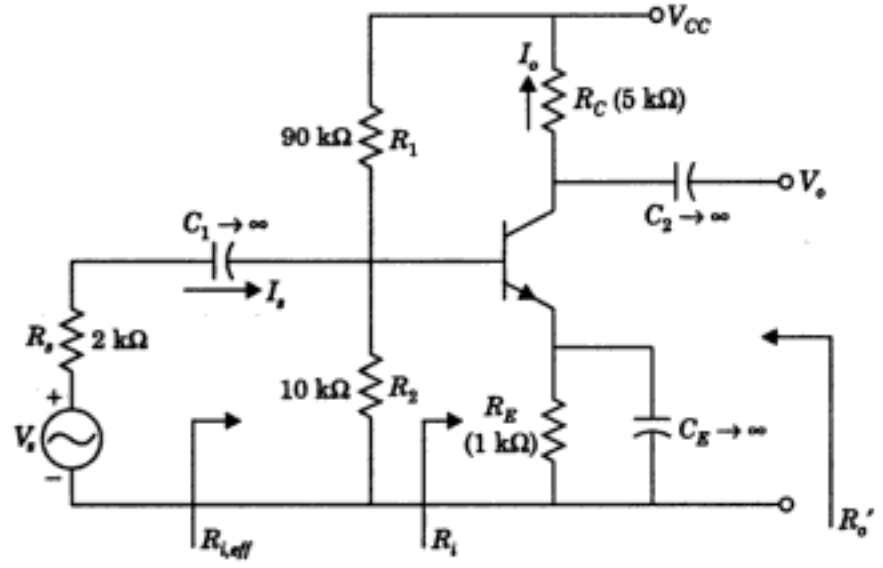


Fig. 6.22(a) Circuit for Example 6.4.

Solution: The ac equivalent circuit is shown in Fig. 6.22(b). It may be noted that all the capacitors C_1, C_2 and C_E are large and, therefore, act as short circuits in the ac equivalent circuit.

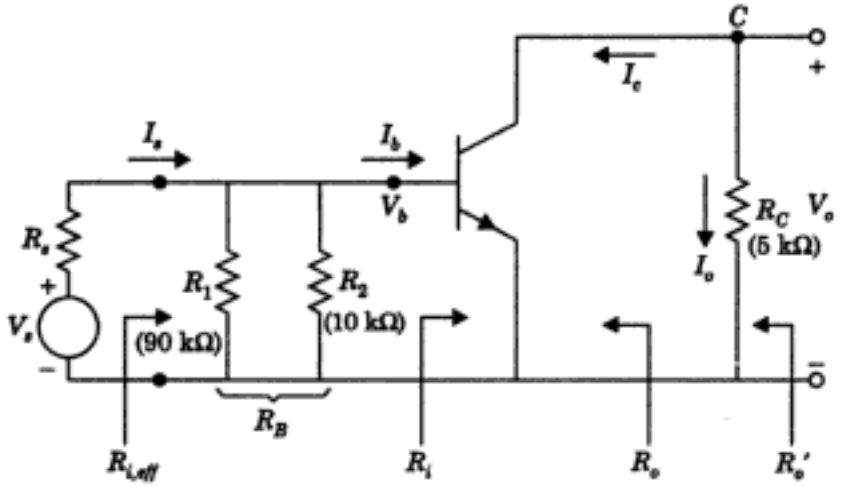


Fig. 6.22(b) ac equivalent circuit for the circuit of Example 6.4.

The only difference in this circuit from that of basic *CE* amplifier is the presence of biasing resistors R_1, R_2. One can, therefore make use of all the results derived earlier and given in Table 6.3. Thus, it is not necessary to replace the transistor by its *h*-model. In Fig. 6.22(b),

$$R_B = R_1 \,||\, R_2$$

$$= 90 \text{ k}\Omega \,||\, 10 \text{ k}\Omega = 9 \text{ k}\Omega$$

Current gain,

$$A_I = \frac{I_o}{I_b} = -\frac{h_{fe}}{1 + h_{oe} R_C}$$

$$= -\frac{50}{1 + 20 \times 10^{-6} \times 5 \times 10^3} = -\frac{50}{1.1}$$

$$= -45.45$$

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It may be noted that A_I in Table 6.3 gives current gain from collector to base only.

Input impedance $R_i = h_{ie} + h_{re}A_I R_C$

$$= 2 + 2 \times 10^{-4} \times (-45.45) \times 5$$
$$= 2 - 0.04545$$
$$= 1.954 \text{ k}\Omega$$

Overall input impedance $R_{i,\text{eff}}$ is obtained as:

$$R_{i,\text{eff}} = R_B \| R_i$$
$$= 9 \text{ k}\Omega \| 1.954 \text{ k}\Omega$$
$$= 1.6 \text{ k}\Omega$$

Overall circuit gain $$A_I' = \frac{I_o}{I_s} = \frac{I_o}{I_b} \times \frac{I_b}{I_s} = A_I \times \frac{I_b}{I_s}$$

Since $$\frac{I_b}{I_s} = \frac{R_B}{R_B + R_i}$$

$$= \frac{9}{9 + 1.954}$$

$$= 0.82$$

Thus, $$A_I' = -45.45 \times 0.82 = -37.26$$

Voltage gain $$A_{Vs} = \frac{V_o}{V_s} = \frac{V_o}{V_b} \times \frac{V_b}{V_s} = A_I \frac{R_C}{R_i} \times \frac{R_{i,\text{eff}}}{R_s + R_{i,\text{eff}}}$$

$$= \frac{-45.45 \times 5}{1.954} \times \frac{1.6}{2 + 1.6}$$

$$= -51.68$$

In order to compute R_o, we must first find the effective source resistance by setting $V_s = 0$.

It can be seen that,

$$R_{s,\text{eff}} = R_s \| R_1 \| R_2$$
$$= 2 \text{ k}\Omega \| 9 \text{ k}\Omega = 1.636 \text{ k}\Omega$$

Therefore, $$Y_o = \frac{1}{R_o} = h_{oe} - \frac{h_{fe}h_{re}}{R_{s,\text{eff}} + h_{ie}}$$

$$= 20 \times 10^{-6} - \frac{50 \times 2 \times 10^{-4}}{1.636 + 2}$$

$$= 20 \times 10^{-6} - 0.27 \times 10^{-2}$$

$$\cong 20 \times 10^{-6}$$

So, $$R_o = 50 \text{ k}\Omega$$

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and $$R_o' = R_o || R_C$$
$$= 50\ \text{k}\Omega || 5\ \text{k}\Omega = 4.54\ \text{k}\Omega$$

Thus:

$$A_I' = -37.26; \quad R_{i,\text{eff}} = 1.6\ \text{k}\Omega; \quad A_{V_s} = -51.68$$
$$R_o = 50\ \text{k}\Omega; \quad R_o' = 4.54\ \text{k}\Omega$$
Ans.

Analysis of common collector amplifier (Emitter follower): The circuit of a *CC* transistor (or grounded collector) amplifier is shown in Fig. 6.23. Here, the collector is connected directly to the supply V_{CC} and (not through R_C, as was in the *CE* configuration). Thus, the collector is at ground potential in ac model. This circuit is also known as **emitter follower** because its voltage gain is close to unity. Thus, any input signal voltage applied at the base appears across the load at emitter without any change in amplitude or phase. The emitter follows the variations taking place at base and hence the name emitter follower. It will further be shown that this circuit has high current gain, high input resistance (hundreds of kilohms) and low output resistance (tens of ohms). Because of these, an emitter follower finds application in connecting a signal source of high impedance to a load of low impedance, that is, it acts as a buffer stage.

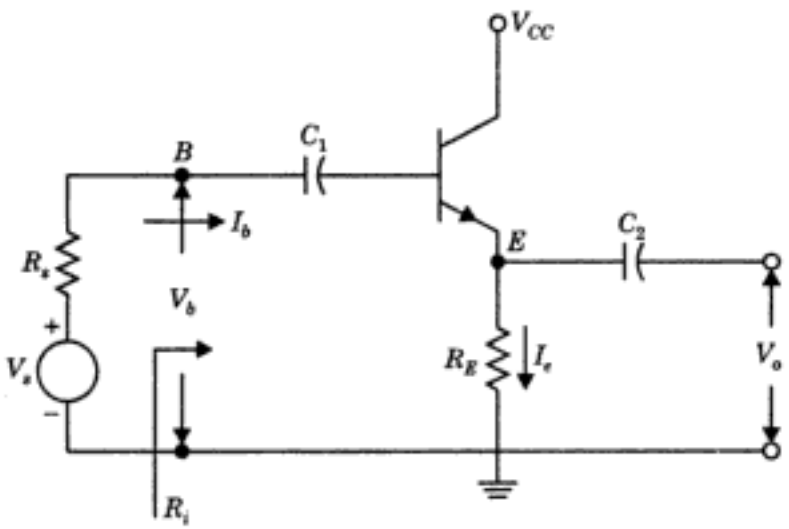


Fig. 6.23 A *CC* amplifier (emitter follower).

The various formulae for A_I, A_V, R_i and R_o for a *CC* amplifier are easily obtained from the formulae derived for a *CE* amplifier (Table 6.3) simply by changing the suffix *e* to *c*. Further, the *h*-parameters in *CE* configuration are usually available, therefore, using conversion formulae from Table 6.2 for converting *CE* parameters to *CC* parameters, we may write,

$$A_I = \frac{I_e}{I_b} = \frac{-h_{fc}}{1 + h_{oc}R_E} = \frac{(1 + h_{fe})}{1 + h_{oe}R_E} \quad \text{[Here load is } R_E\text{, so } R_C = R_E\text{]} \tag{6.70}$$

$$R_i = \frac{V_b}{I_b} = h_{ic} + h_{rc}A_I R_E = h_{ie} + A_I R_E \quad [h_{rc} = 1] \tag{6.71}$$

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$$A_V = \frac{V_o}{V_b} = \frac{A_I R_E}{R_i} \tag{6.72}$$

$$= \frac{R_i - h_{ie}}{R_i} = 1 - \frac{h_{ie}}{R_i} \qquad \text{[using Eq. 6.71]}$$

and
$$Y_o = h_{oc} - \frac{h_{fc}h_{rc}}{h_{ic} + R_s} = h_{oe} + \frac{(1 + h_{fe})}{h_{ie} + R_s} \tag{6.73}$$

Using the same values of the transistor parameters as used in Example 6.2, and with R_E = 5 kΩ and R_s = 1 kΩ, the results are found to be as:

$$A_I = 91.8; \qquad A_V = 0.998; \qquad A_{V_s} = 0.995$$

$$R_i = 460 \text{ kΩ}; \qquad R_o = 19.79 \text{ Ω}$$

Thus, it is verified that an emitter follower has voltage gain close to unity, high current gain and very high input resistance and low output resistance. Note that the voltage gain of almost unity and low output resistance imply that the source V_s with resistance R_s has been replaced by a new source $V_s' = A_V V_s \approx V_s$ and a low output resistance of nearly R_s/h_{fe} (low). So we have obtained a better output voltage source. (low resistance causes low loading effect). Hence a *CC* amplifier is also called a **buffer** or a **voltage follower**.

6.4.2 Simplified *h*-parameter Model

From the values of four *h*-parameters given in Table 6.1 for *CE* configuration it can be seen that the values of parameters h_{re} *and* h_{oe} *are small enough and can be neglected in the model.* Thus, for all the practical purposes, only two of the four parameters, that is, h_{ie} and h_{fe} are sufficient to perform approximate analysis of the transistor circuits at low frequencies. The simplified model for CE transistor is shown in Fig. 6.24 and is used for load resistances small enough to satisfy the condition $h_{oe}R_C < 0.1$. The errors are found to be less than 10% in the calculations for A_I, A_V, R_i and R_o. Thus, for h_{oe} = 25 μA/V, for the values of load $R_C \leq 4$ kΩ, $h_{oe}R_C$ will be less than or equal to 0.1. However, for R_C much greater than 4 kΩ, this condition will not be satisfied and approximate model cannot be used.

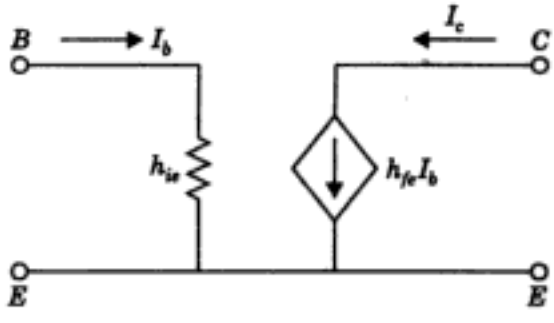


Fig. 6.24 Approximate *h*-parameter model for a *CE* transistor.

In most of the practical situations, it is sufficient to obtain approximate values of A_I, R_i, A_V, R_o in place of carrying out the lengthy exact calculations and obtain a physical feel of the transistor circuit. This is illustrated by analyzing a *CE* amplifier by using approximate *h*-parameter model.

Analysis of a CE amplifier: The ac equivalent circuit of a *CE* amplifier using approximate *h*-parameter model is shown in Fig. 6.25.

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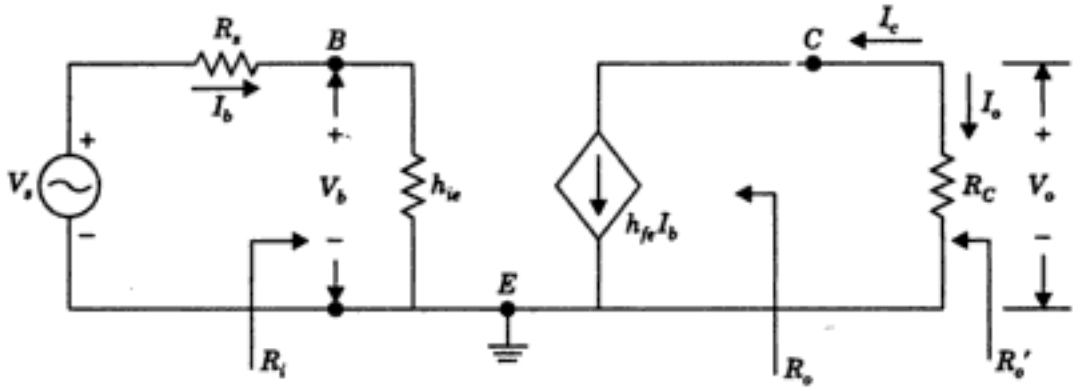


Fig. 6.25 ac equivalent circuit of *CE* amplifier using approximate *h*-parameter model.

Current gain A_I

Since $$A_I = \frac{I_o}{I_b}$$

In Fig. 6.25,

$$I_o = -h_{fe} I_b$$

Therefore, $$A_I = \frac{I_o}{I_b} = -h_{fe} \tag{6.74}$$

Input resistance R_i

It is seen clearly that

$$R_i = h_{ie} \tag{6.75}$$

Voltage gain A_V

$$A_V = \frac{V_o}{V_b} = \frac{I_o R_C}{I_b R_i} = A_I \frac{R_C}{R_i}$$

Putting values of A_I and R_i, we get

$$A_V = -\frac{h_{fe} R_C}{h_{ie}} \tag{6.76}$$

Output resistance R_o

By inspection, we find

$$R_o = \infty \tag{6.77a}$$

and $$R_o' = R_C \tag{6.77b}$$

Analysis of CE amplifier with emitter resistance: Figure 6.26(a) shows a *CE* amplifier with a resistance R_E in the emitter branch. This circuit has the important feature of providing stability to the voltage gain of the *CE* amplifier. As will be seen voltage gain of the amplifier becomes almost independent of the *h*-parameters and, therefore, does not vary with change of device or temperature variation.

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Using the approximate h-parameter model, ac equivalent circuit is shown in Fig. 6.26(b).

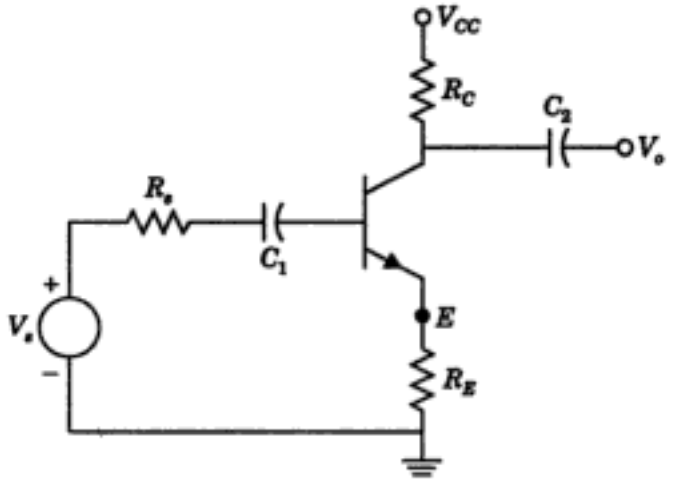


Fig. 6.26(a) *CE* amplifier with emitter resistance, R_E.

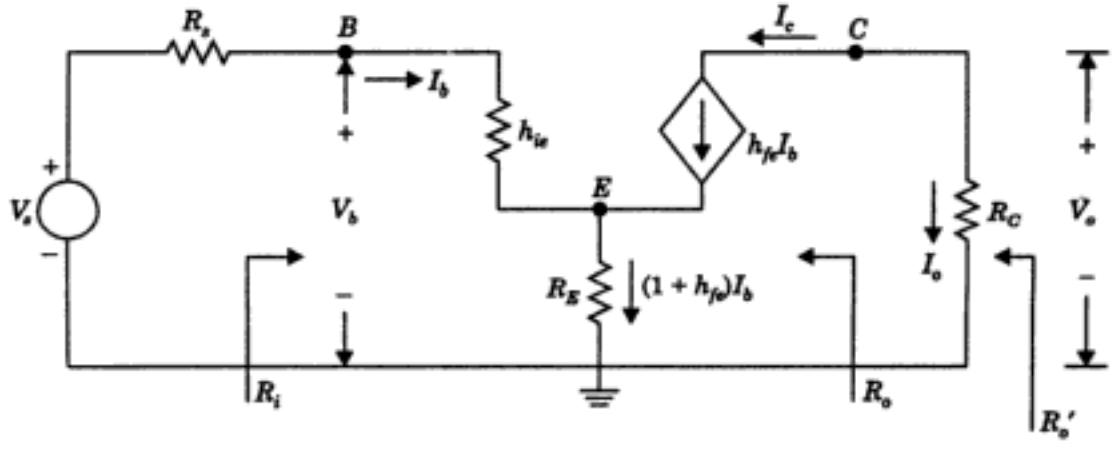


Fig. 6.26(b) ac equivalent circuit using approximate h-model.

Current gain A_I

In Fig. 6.26(b),

$$I_o = -h_{fe}I_b \tag{6.78}$$

$\therefore$

$$A_I = \frac{I_o}{I_b} = -h_{fe} \tag{6.79}$$

Input resistance R_i

From the input loop,

$$V_b = h_{ie}I_b + (1 + h_{fe})I_bR_E \tag{6.80}$$

Therefore,

$$R_i = \frac{V_b}{I_b} = h_{ie} + (1 + h_{fe})R_E \tag{6.81}$$

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The input resistance of a *CE* amplifier with a resistance R_E is seen to be increased by $(1 + h_{fe})R_E$.

Voltage gain A_V

$$A_V = \frac{A_I R_C}{R_i} = -\frac{h_{fe} R_C}{h_{ie} + (1 + h_{fe})R_E} \tag{6.82}$$

Usually, $(1 + h_{fe})R_E >> h_{ie}$ and for $h_{fe} >> 1$, therefore Eq. (6.82) yields:

$$A_V \cong -\frac{h_{fe} R_C}{h_{fe} R_E}$$

$$= -\frac{R_C}{R_E} \tag{6.83}$$

The voltage gain of this circuit can be seen to be independent of the device parameters and is completely stable. Thus, if a resistance is put in the emitter branch of a *CE* amplifier, the voltage gain is stabilized, although it gets reduced due to the "negative feedback" effect of R_E. (We shall study more about the negative feedback in the chapter on Feedback).

Output impedances R_o and R_o'

It can be easily seen from Fig. 6.26(b) that $R_o = \infty$ and $R_o' = R_o || R_C = R_C$.

EXAMPLE 6.5

Compute $A_I = I_o/I_s$, $A_{Vs} = V_o/V_s$, R_i and R_o' for the transistor amplifier shown in Fig. 6.27(a). The transistor parameters are: $h_{ie} = 4$ kΩ, $h_{fe} = 200$, $h_{re} = 0$, $h_{oe} = 0$.

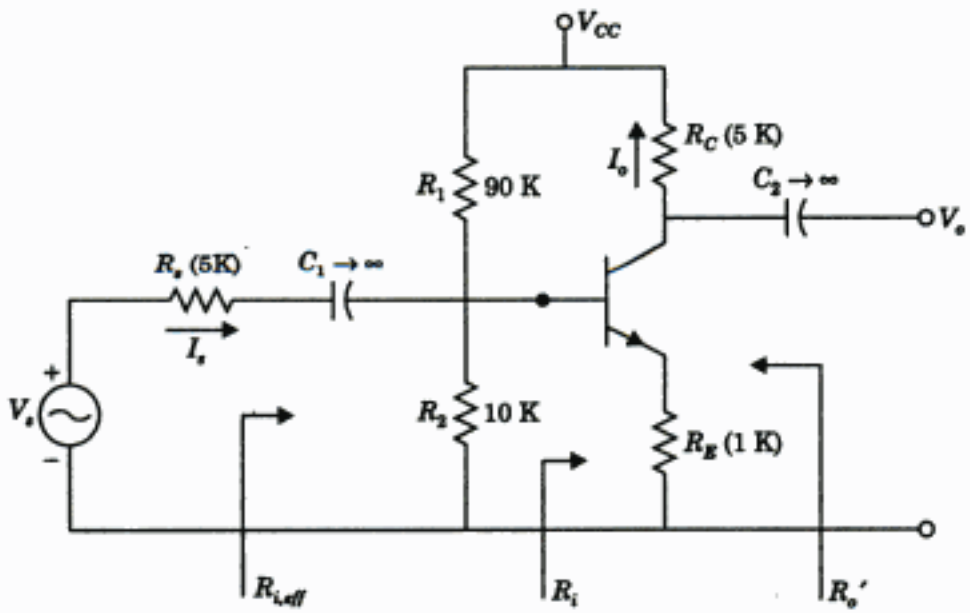


Fig. 6.27(a) Circuit diagram for Example 6.5.

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Solution: The ac equivalent circuit is obtained by short circuiting capacitors C_1, C_2 and V_{CC} and shown in Fig. 6.27(b). It can be seen that R_1 comes in parallel to R_2.

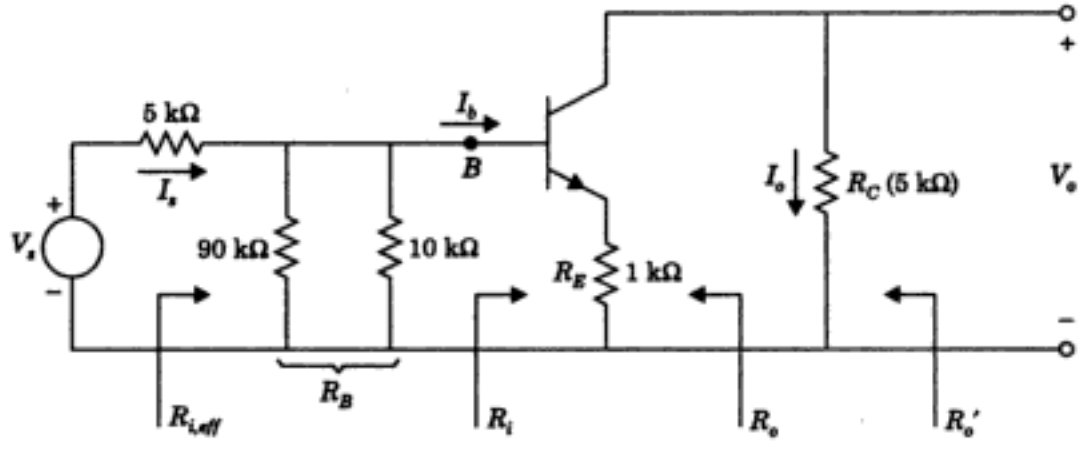


Fig. 6.27(b) ac equivalent circuit for Example 6.5.

We can use approximate analysis as h_{re} and h_{oe} both are given zero. All the results that were derived for a *CE* amplifier with emitter resistance, R_E can be used.

Thus,

$$A_I' = \frac{I_o}{I_b} = -h_{fe}$$

$$= -200$$

$$R_i = h_{ie} + (1 + h_{fe})R_E \qquad \text{[Input resistance at base]}$$

$$= 4 + 201 \times 1$$

$$= 205\ \text{k}\Omega$$

$$R_{i,\text{eff}} = R_B \| R_i \qquad [R_B = 90\ \text{k}\Omega \| 10\ \text{k}\Omega = 9\ \text{k}\Omega]$$

$$= 9\ \text{k}\Omega \| 205\ \text{k}\Omega$$

$$= 8.62\ \text{k}\Omega$$

$$A_I = \frac{I_o}{I_s} = \frac{I_o}{I_b} \times \frac{I_b}{I_s}$$

$$= (-h_{fe}) \frac{R_B}{R_B + R_i}$$

$$= (-200) \times \frac{9}{9 + 205}$$

$$= -8.41$$

$$A_{VS} = \frac{V_o}{V_s} = \frac{V_o}{V_b} \times \frac{V_b}{V_s} = A_I' \frac{R_C}{R_i} \times \frac{R_{i,\text{eff}}}{R_s + R_{i,\text{eff}}}$$

$$= -200 \times \frac{5}{205} \times \frac{8.62}{5 + 8.62}$$

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$$= -25.95$$

$$R_o = \infty$$

$$R_o' = R_o || R_C = 5 \text{ k}\Omega$$

Analysis of a CC amplifier (Emitter follower) using approximate h-model. The analysis of an emitter follower of Fig. 6.28(a) can also be done by replacing the transistor by its model valid for *CE* configurations. The ac equivalent circuit using approximate *h*-model is shown in Fig. 6.28(b).

Current gain

In Fig. 6.28(b),

$$I_o = (1 + h_{fe})I_b \tag{6.84}$$

Therefore, the current gain A_I is expressed as:

$$A_I = \frac{I_o}{I_b} = (1 + h_{fe}) \tag{6.85}$$

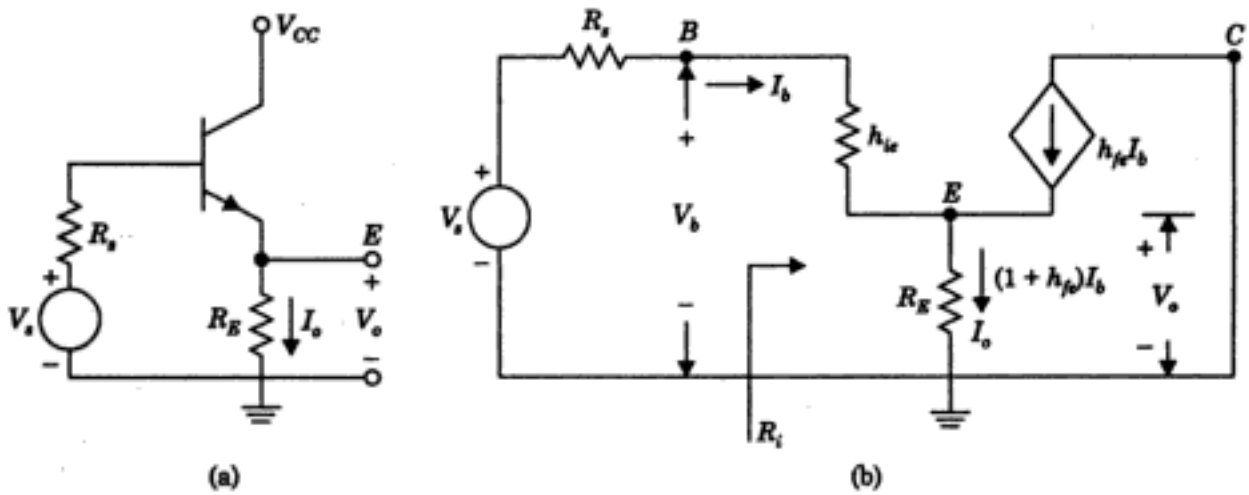


Fig. 6.28 (a) Emitter follower circuit, (b) AC equivalent circuit of an emitter follower using approximate *h*-model.

Input resistance R_i

From the input loop,

$$V_b = h_{ie}I_b + (1 + h_{fe})R_E I_b \tag{6.86}$$

Therefore, the input resistance R_i is:

$$R_i = \frac{V_b}{I_b} = h_{ie} + (1 + h_{fe})R_E \tag{6.87}$$

Voltage gain

Since $$V_o = (1 + h_{fe})I_b R_E \tag{6.88}$$

and $$V_b = h_{ie}I_b + (1 + h_{fe})I_b R_E \tag{6.89}$$

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The voltage gain A_V is:

$$A_V = \frac{V_o}{V_b} = \frac{(1+h_{fe})R_E}{h_{ie}+(1+h_{fe})R_E} \tag{6.90}$$

The denominator in Eq. (6.90) will always be greater than the numerator, therefore, the voltage gain is less then unity as expected.

Output resistances R_o and R_o'

Using the open circuit voltage, short circuit current method which is found to be more convenient, we find

Open circuit voltage $V_{oc} = V_s$ (Since $R_E = \infty$ and $I_b = 0$) (6.91)

Short circuit current $I_{sc} = (1 + h_{fe})I_b$ [for $R_E = 0$] (6.92)

and $V_s = (R_s + h_{ie})I_b$ (6.93)

Therefore, $$I_{sc} = \frac{(1+h_{fe})V_s}{R_s + h_{ie}} \tag{6.94}$$

and $$R_o = \frac{V_{oc}}{I_{Sc}} \tag{6.95}$$

$$= \frac{R_S + h_{ie}}{1+h_{fe}} \tag{6.96}$$

So $$R_o' = R_o \| R_E \tag{6.97}$$

For R_E = 5 kΩ and R_S = 1 kΩ and h_{ie} = 1 kΩ; h_{fe} = 100, the results are found:

A_I = 101; R_i = 506 kΩ

A_V = 0.998; R_o = 19.8 Ω

It can be seen by comparing these results with those obtained using exact analysis, the errors are within 10%.

CB amplifier analysis using approximate h-model: Figure 6.29(a) shows the circuit of a *CB* amplifier. The ac equivalent circuit using approximate *h*-parameter model for *CB* configuration is shown in Fig. 6.29(b).

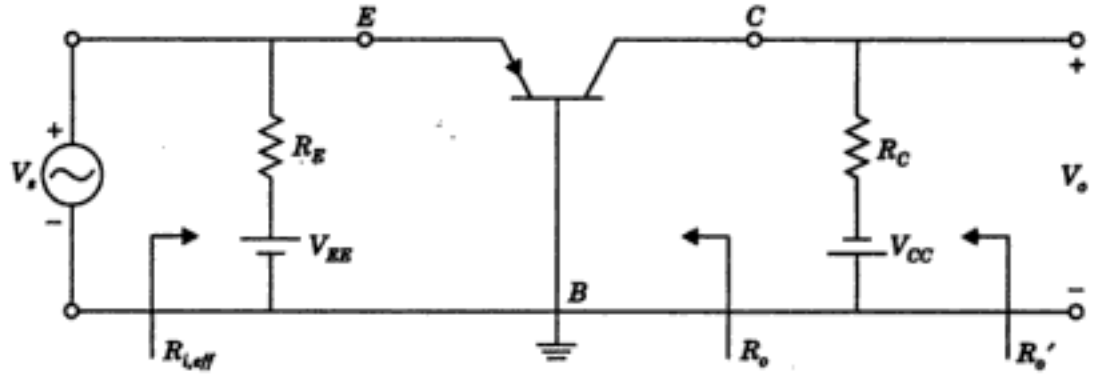


Fig. 6.29(a) A *CB* amplifier stage (pnp transistor).

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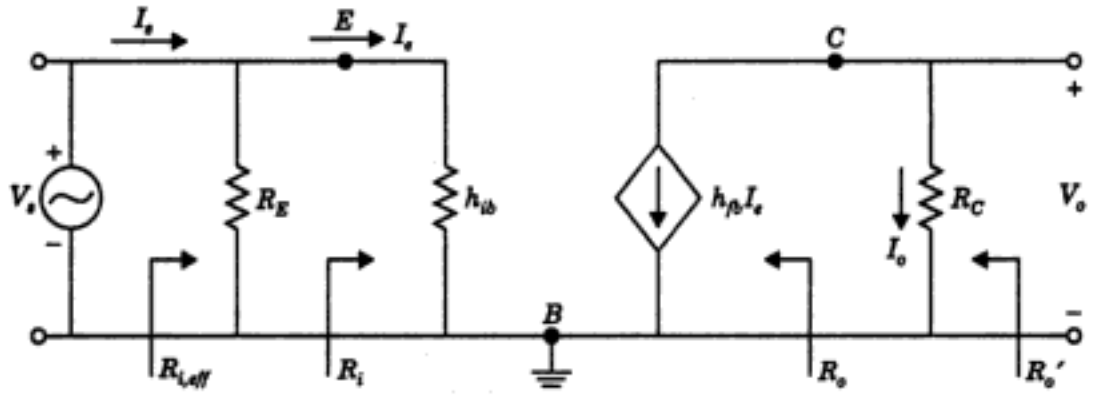


Fig. 6.29(b) ac equivalent circuit using *CB* *h*-model.

It is easily seen from Fig. 6.29(b).

Input impedance
$$R_i = h_{ib} \tag{6.98a}$$

and
$$R_{i,eff} = R_E \| h_{ib} \tag{6.99b}$$

Current gain A_I
$$I_o = -h_{fb} I_e \tag{6.100}$$

So
$$A_I = \frac{I_o}{I_e} = -h_{fb} \tag{6.101}$$

and
$$A_I' = \frac{I_o}{I_s} = \frac{A_I R_E}{R_E + R_i} \tag{6.102}$$

Voltage gain A_V
$$V_o = I_o R_C$$
$$= -(h_{fb} I_e) R_C \tag{6.103}$$

Since
$$I_e = \frac{V_s}{h_{ib}} \quad \text{[Voltage at node } E \text{ is } V_s\text{]} \tag{6.104}$$

So
$$V_o = -\frac{h_{fb} V_s}{h_{ib}} R_C \tag{6.105}$$

Thus,
$$A_V = \frac{V_o}{V_s} = -\frac{h_{fb}}{h_{ib}} R_C \tag{6.106}$$

Output resistances R_o and R_o' can be seen by inspection as:
$$R_o = \infty \tag{6.107}$$
$$R_o' = R_C$$

The above analysis gives the results in terms of *CB* parameters. If only *CE* parameters are available then conversion formulae from Table 6.2 can be used.

The analysis can also be performed by replacing the *CE* approximate *h*-model between E, B and C and deriving the results by writing KVL equations as shown in Fig. 6.30.

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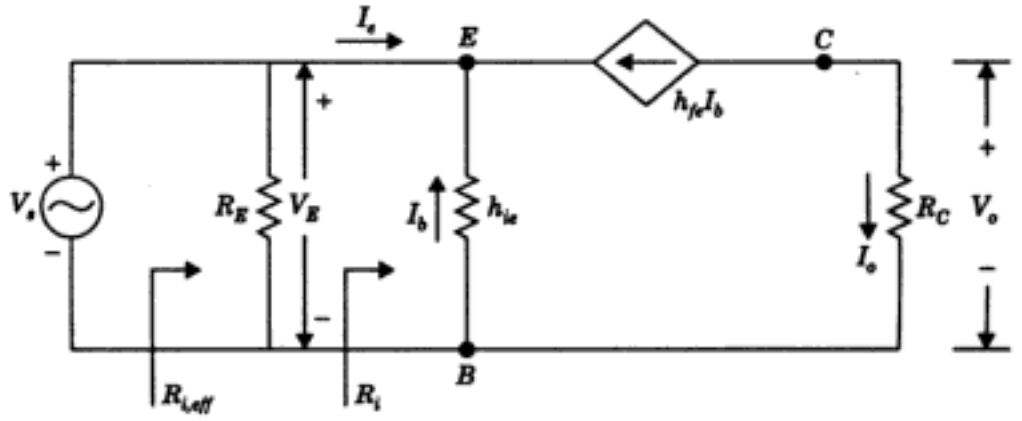


Fig. 6.30 ac equivalent circuit of a *CB* amplifier using *CE* *h*-model.

In Fig. 6.30,

$$I_e = -(1 + h_{fe})I_b \tag{6.108}$$

and voltage at emitter, V_E (V_E is also equal to V_s)

$$V_E = -I_b h_{ie} \tag{6.109}$$

Input resistance R_i is given as:

$$R_i = \frac{V_E}{I_e} = \frac{-h_{ie}I_b}{-(1+h_{fe})I_b} = \frac{h_{ie}}{1+h_{fe}} = h_{ib} \quad \left[\text{Using conversion formulae from Table 6.2}\right] \tag{6.110}$$

Current gain $$A_I = \frac{I_o}{I_e} = \frac{-h_{fe}I_b}{-(1+h_{fe})I_b} = \frac{h_{fe}}{1+h_{fe}} = -h_{fb} \tag{6.111}$$

Voltage gain $$A_V = \frac{V_o}{V_s}$$

Here, $$V_o = I_o R_C \tag{6.112}$$

and $$V_s = V_E = I_e R_i \tag{6.113}$$

Thus, $$A_V = \frac{I_o R_C}{I_e R_i} = \frac{A_I R_C}{R_i} \tag{6.114}$$

Putting the values of A_I and R_i from Eqns. (6.111) and (6.110), we get

$$A_V = -\frac{h_{fb}}{h_{ib}} R_C \tag{6.115}$$

By inspection, it can be seen

$$R_o = \infty \; ; \quad R_o' = R_C \tag{6.116}$$

The results derived here are exactly same to those derived using *CB* *h*-model.

Summary of Results

The various results derived for different amplifier configurations using approximate *h*-parameter model have been listed in the Table 6.4.

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Table 6.4 Summary of Important Results Using Approximate h-parameter Model

	CE	CE with R_E	CC	CB
A_I	$-h_{fe}$	$-h_{fe}$	$(1 + h_{fe})$	$-h_{fb} = \frac{h_{fe}}{1+h_{fe}}$
R_i	h_{ie}	$h_{ie} + (1 + h_{fe})R_E$	$h_{ie} + (1 + h_{fe})R_C$	$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$
A_V	$-\frac{h_{fe}R_c}{h_{ie}}$	$-\frac{h_{fe}R_C}{R_i}$	$1 - \frac{h_{ie}}{R_i}$	$\frac{-h_{fb}}{h_{ib}}R_C = h_{fe}\frac{R_C}{h_{ie}}$
R_o	∞	∞	$\frac{R_s + h_{ie}}{1+h_{fe}}$	∞
R_o'	R_C	R_C	$R_o \| R_C$	R_C

6.4.3 Analysis of Transistor Circuits Using Hybrid-π Model

Figure 6.31[(a) and (b)] shows the two versions of the hybrid-π model of a BJT at low frequencies already discussed in section 6.1.2. If h-parameters of a transistor are not available and only value of β_o is provided then we use hybrid-π model for analyzing an amplifier stage.

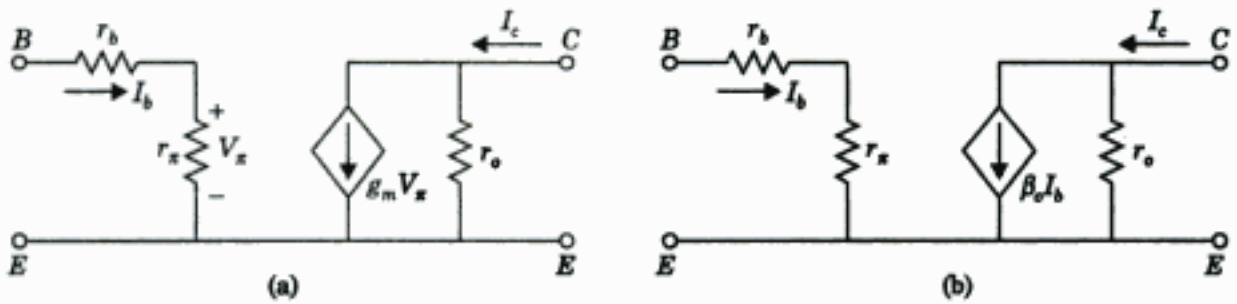


Fig. 6.31 Two versions of hybrid-π model.

It was also shown in section 6.1.2 that

Transconductance $$g_m = \left|\frac{I_{CQ}}{V_T}\right|$$

ac short circuit current gain at low frequency, $\beta_o = g_m r_\pi$

Output resistance $$r_o = \left|\frac{V_A}{I_{CQ}}\right|$$

where V_A is the early voltage and I_{CQ} is the quiescent collector current.

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It can be seen that, the parameters of hybrid-π model (g_m, r_π and r_o) depend upon the quiescent current, I_{CQ}, and this is the reason that this *model provides more accurate analysis* compared to h-parameter model. Thus, when performing analysis of transistor circuits using hybrid-π model, one must perform the dc analysis as well for complete solution. Before taking up some examples where both ac and dc analysis are performed, we first discuss the ac analysis by using hybrid-π model.

Common emitter (CE) amplifier (ac analysis): Figure 6.32(a) shows the basic configuration of a *CE* amplifier. For simplicity, biasing circuit has not been included in the analysis. The

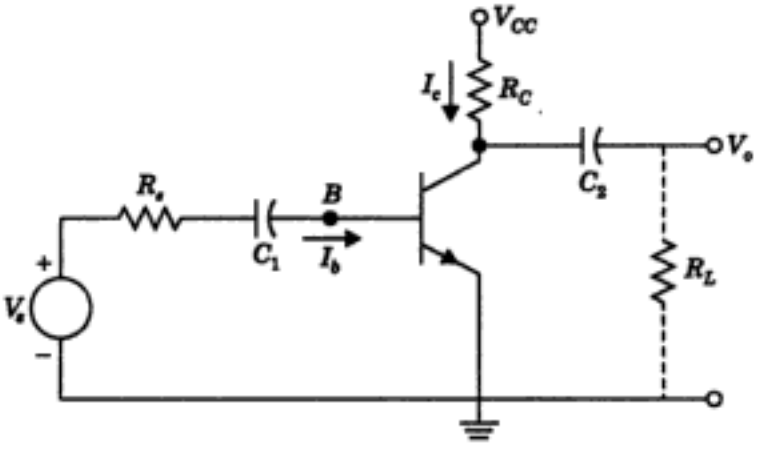


Fig. 6.32(a) A *CE*-amplifier.

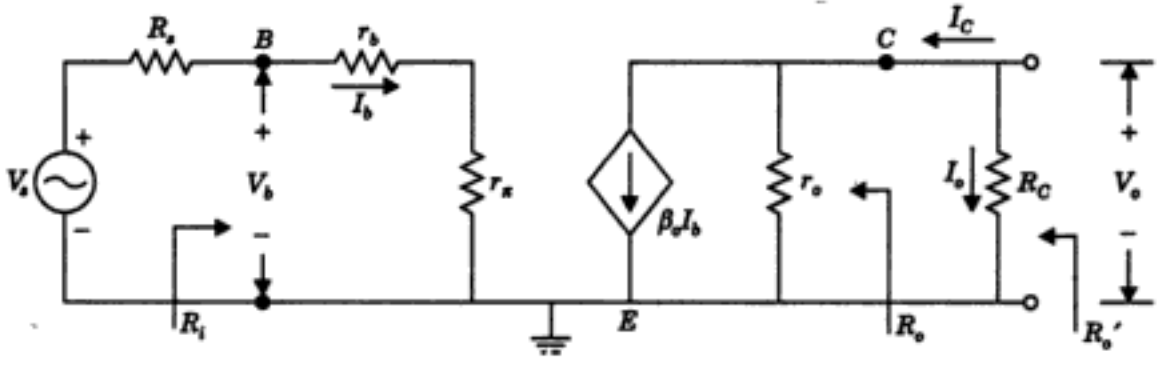


Fig. 6.32(b) ac equivalent circuit using hybrid-π model.

analysis of such a basic *CE* amplifier has already been done using h-parameter model in section 6.3.2. Now, we are doing the analysis using hybrid-π model. The ac equivalent circuit of the *CE* amplifier using hybrid-π model is shown in Fig. 6.32(b).

In practical amplifiers, the output is taken across the actual load resistance R_L [shown dotted lines in Fig. 6.32(a)], so as to couple only the ac output available across R_C. In the ac equivalent circuit shown in Fig. 6.32(b), the resistance R_C will simply be modified to $R_C' = R_C \| R_L$ and it will not make any change on the method of ac analysis. The various ac quantities, A_I, R_i, A_V, R_o and R_o' can be obtained from the ac equivalent circuit shown in Fig. 6.32(b).

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Current gain A_I

Using current divider relation in the output circuit of Fig. 6.32(b),

$$I_c = \frac{\beta_o I_b r_o}{r_o + R_C} \tag{6.117}$$

Thus,
$$A_I = \frac{I_o}{I_b} = -\frac{I_c}{I_b} = \frac{-\beta_o r_o}{r_o + R_C} \tag{6.118}$$

For $R_C << r_o$

$$A_I \cong -\beta_o \tag{6.119}$$

This is the expected result as β_o is the short circuit current gain of the transistor (for $R_C = 0$).

Input resistance R_i

It can be seen from Fig. 6.32(b), that

$$R_i = \frac{V_b}{I_b} = r_b + r_\pi \tag{6.120}$$

The value of r_b is usually small as compared to r_π and can be neglected. Thus,

$$R_i = r_\pi \tag{6.121}$$

Overall voltage gain A_{Vs}

From the output loop, we may write

$$V_o = -\beta_o I_b \ (R_C || r_o) \tag{6.122}$$

and from the input loop,

$$V_s = I_b(r_b + r_\pi + R_s) \tag{6.123}$$

Therefore,
$$A_{Vs} = \frac{V_o}{V_s}$$

$$= -\frac{\beta_o (R_C || r_o)}{(r_b + r_\pi + R_s)} \tag{6.124}$$

For discrete circuits, $r_o >> R_C$ usually, therefore, Eq. (6.124) reduces to

$$A_{Vs} \cong -\frac{\beta_o R_C}{r_b + r_\pi + R_s} \tag{6.125}$$

In all the IC amplifiers, one is interested in maximum possible gain that can be achieved from the *CE* amplifier. It can be seen from Eqn. (6.125) that the gain of a *CE* amplifier can be increased by increasing R_C. However, when $R_C >> r_o$ then $R_C || r_o \cong r_o$ and gain of the amplifier becomes independent of R_C. Now, the maximum gain that can be achieved from a *CE* amplifier is given by

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$$A_{Vs,\max} = \frac{-\beta_o r_o}{r_o + r_\pi + R_s} \tag{6.126}$$

Usually, $r_\pi >> (r_b + R_s)$

Thus, $$A_{Vs,\max} = \frac{-\beta_o r_o}{r_\pi}$$

$$= -g_m r_o \quad (\text{as } \beta_o = r_\pi g_m) \tag{6.127}$$

Since $$r_o = \frac{|V_A|}{|I_{CQ}|}$$

and $$g_m = \frac{|I_{CQ}|}{V_T}$$

So, $$A_{Vs,\max} = \frac{-V_A}{V_T} \tag{6.128}$$

As an example, in IC amplifiers, with $V_A = 100$ V and $V_T = 25$ mV, Eq. (6.128) yields a maximum voltage gain of 4000.

Output resistance R_o

The output resistance R_o is found by setting $V_s = 0$ in Fig. 6.32(b). If $V_s = 0$, I_b will be zero, and therefore,

$$R_o = r_o \tag{6.129a}$$

and $$R_o' = r_o \| R_C \tag{6.129b}$$

Usually, $r_o >> R_C$, so $R_o' = R_C$

The various results derived for the *CE* amplifier have been summarized in the first columns of Table 6.5. The results using approximate model with $r_o \to \infty$ and $r_b = 0$ are also listed in the second column of Table 6.5.

Table 6.5 *CE* Amplifier Stage Results

Quantity	*Exact formulae*	*Approximate* ($r_b = 0$, $r_o = \infty$)
A_i	$-\frac{\beta_o r_o}{r_o + R_C}$	$-\beta_o$ ($r_o = \infty$)
R_i	$r_b + r_\pi$	r_π ($r_b = 0$)
A_{Vs}	$-\frac{\beta_o (r_o \| R_C)}{R_s + r_b + r_\pi}$	$\frac{-\beta_o R_C}{R_s + r_\pi}$ ($r_b = 0, r_o = \infty$)
R_o	r_o	∞
R_o'	$r_o \| R_C$	R_C ($r_o = \infty$)

EXAMPLE 6.6

Find A_I, R_i, A_{V_s} for the *CE* amplifier shown in Fig. 6.33. Assume $\beta_o = \beta_F^* = 100$, $r_b = 0$, $r_o = \infty$.

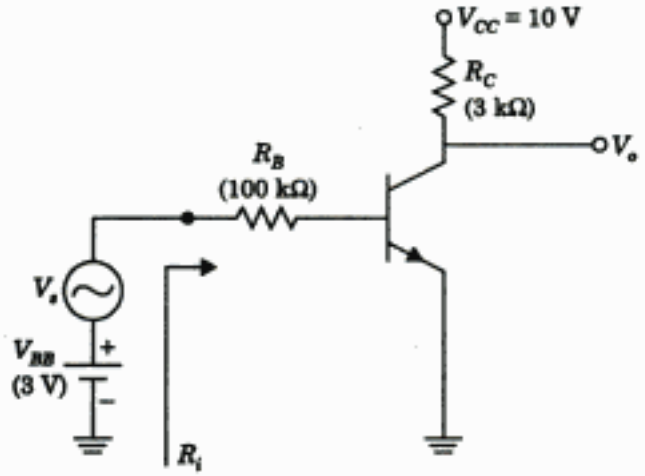


Fig. 6.33 Circuit for Example 6.6.

Solution: In order to determine the small signal parameters g_m and r_π, we first carry out the dc analysis to find the dc quiescent current I_{CQ}. The dc equivalent circuit is obtained by making $V_s = 0$ and is shown in Fig. 6.34(a).

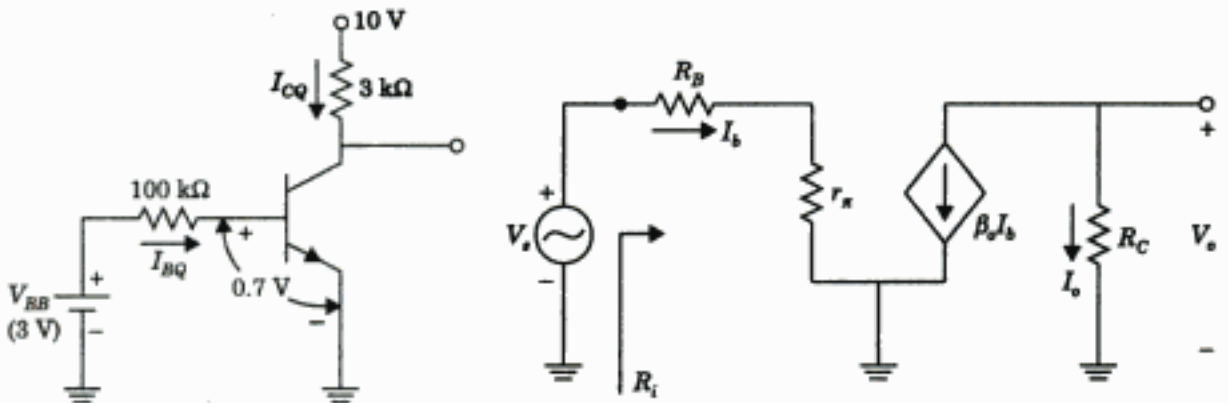


Fig. 6.34 (a) dc equivalent circuit, (b) ac equivalent circuit using approximate hybrid-π model.

DC analysis

Since emitter base junction is forward biased, assume that the transistor is operating in the active mode of operation. In Fig. 6.34(a),

$$I_{BQ} = \frac{V_{BB} - V_{BE,\text{active}}}{R_B}$$

$$= \frac{3 - 0.7}{100} \qquad \text{(assuming } V_{BE,\text{active}} = 0.7 \text{ V)}$$

$$= 0.023 \text{ mA}$$

*For all practical purposes, dc beta (β_F) is assumed equal to ac beta (β_o).

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Since $I_{CQ} = \beta_F I_{BQ}$

$= 100 \times 0.023 = 2.3$ mA

So $I_{CQ} = 2.3$ mA

Now, we can find the small signal parameters, g_m and r_π as:

$$g_m = \frac{I_{CQ}}{V_T}$$

$$= \frac{2.3}{25} = 92 \text{ mA/V}$$

and $$r_\pi = \frac{\beta_o}{g_m}$$

$$= \frac{100}{92} = 1.09 \text{ k}\Omega$$

AC analysis

The ac equivalent circuit using approximate hybrid-π model is shown in Fig. 6.34(b).

Current gain $$A_I = \frac{I_o}{I_b} = \frac{-\beta_o I_b}{I_b} = -\beta_o = -100$$

Input resistance $R_i = R_B + r_\pi$

$= 100 + 1.09 = 101.09$ kΩ

Voltage gain

Since $V_o = I_o R_C$

$= -\beta_o I_b R_C$

and $$I_b = \frac{V_s}{R_B + r_\pi}$$

Therefore, $$A_{V_s} = \frac{V_o}{V_s} = \frac{-\beta_o R_C}{R_B + r_\pi}$$

$$= \frac{100 \times 3}{100 + 1.09} = -2.96$$

The common collector amplifier or emitter follower: Figure 6.35(a) shows the circuit diagram of a basic common collector amplifier. It can be seen that under ac conditions, collector is at ground potential and is common between the input signal source applied at base terminal and output voltage taken from emitter, (that is precisely the reason this configuration is called the **common collector**). It will be shown that a *CC* amplifier provides voltage gain close to unity (but always < 1), high input impedance (hundreds of kohms), low output resistance (tens of ohms) and a high current gain. The most common application of a *CC* amplifier is as a buffer stage and is used to connect a high impedance signal source to a low impedance output load over a wide range of frequencies. When the signal source

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is applied as input of a *CC* [as shown in Fig. 6.35(a)], it gets transformed to a voltage source of low impedance. Figure 6.35(b) shows the ac equivalent circuit using the hybrid-π model. In this model, we have assumed $r_b = 0$ and as r_o is usually much greater than R_E therefore, r_o can be neglected in the analysis.

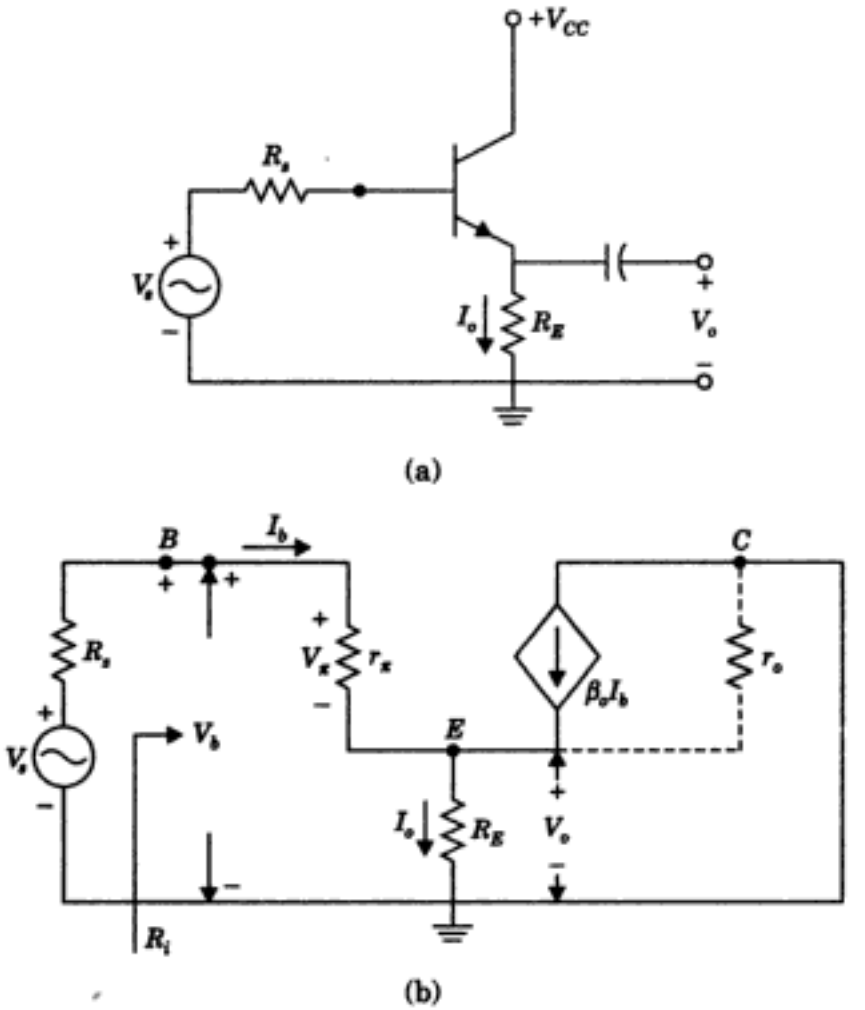


Fig. 6.35 (a) *CC* amplifier, (b) ac equivalent circuit using hybrid-π model.

Current gain A_I

In Fig. 6.35(b),

$$V_\pi = I_b r_\pi \tag{6.130}$$

and

$$I_o = (1 + \beta_o) I_b \tag{6.131}$$

Therefore,

$$A_I = \frac{I_o}{I_b} = (1 + \beta_o) \tag{6.132}$$

Input resistance R_i

Since

$$V_b = I_b r_\pi + (1 + \beta_o) I_b R_E \tag{6.133}$$

$$R_i = \frac{V_b}{I_b} = r_\pi + (1 + \beta_o) R_E \tag{6.134}$$

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The input resistance of a *CC* amplifier is much higher than that of a *CE* amplifier by a factor of $(1 + \beta_o)R_E$.

Voltage gain A_{V_s}

In Fig. 6.35(b),

$$V_o = (1 + \beta_o)I_b R_E \tag{6.135}$$

and

$$V_s = I_b[R_s + r_\pi + (1 + \beta_o)R_E] \tag{6.136}$$

Therefore,

$$A_{V_s} = \frac{V_o}{V_s} = \frac{(1+\beta_o)R_E}{R_s + r_\pi + (1+\beta_o)R_E} \tag{6.137}$$

In Eq. (6.137), denominator will always be greater than the numerator [by $(R_s + r_\pi)$] and thus the voltage gain of the emitter follower is always less than unity (only slightly).

Output resistance R_o

The output resistance, R_o can be obtained by setting $V_s = 0$, $R_E = \infty$ and applying a test voltage V_2 as shown in Fig. 6.36.

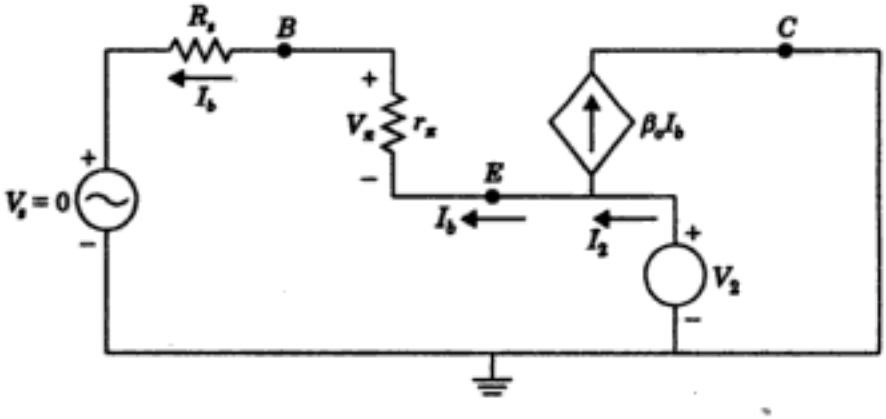


Fig. 6.36 Circuit for finding output resistance R_o.

We may write

$$V_2 = I_b(R_s + r_\pi) \tag{6.138}$$

$$I_2 = (1 + \beta_o)I_b \tag{6.139}$$

Therefore,

$$R_o = \frac{V_2}{I_2} = \frac{R_s + r_\pi}{1 + \beta_o} \tag{6.140}$$

It may be noted from Eq. (6.140) that the output resistance R_o is a function of the source resistance R_s. Further, since $\beta_o >> 1$ (order of 200), the output resistance R_o is usually very small and is of the order of few ohms only. Now, the output resistance, R_o' taking load resistance into account is obtained as

$$R_o' = R_o \| R_E$$

The results derived here have been listed in the first column of Table 6.6 and the results using exact model are listed in the second column of Table 6.6.

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Table 6.6 *CC* Amplifier Stage Results

Quantity	*Approximate*	*Exact* $[R_E' = R_E \| r_o]$
A_I	$+(1+\beta_o)$	$\frac{+(1+\beta_o)r_o}{r_o+R_E}$
R_i	$r_\pi + (1+\beta_o)R_E$	$r_b + r_\pi + R_E'(1+\beta)$
A_{Vs}	$\frac{(1+\beta_o)R_E}{R_s+R_i}$	$\frac{(1+\beta_o)R_E'}{R_s+R_i}$
R_o	$\frac{R_s+r_\pi}{1+\beta_o}$	$r_o \| \frac{R_s+r_b+r_\pi}{1+\beta_o}$
R_o'	$R_o \| R_E$	$R_E \| R_o$

EXAMPLE 6.7

A common collector amplifier stage uses a transistor biased at $I_C = 2$ mA and driven from a 5 kΩ source. It is given for the transistor that $\beta_o = 125$ and $V_A = \infty$.

(a) What value of the load resistance R_E is needed to make $R_i \geq 500$ kΩ.

(b) Using the value of R_E found in part (a), determine A_V, R_o, R_o'.

Solution:

(a) First we evaluate the transistor parameters g_m and r_π.

$$g_m = \frac{I_{CQ}}{V_T} = \frac{2.0}{25} = 80 \text{ m℧}$$

$$r_\pi = \frac{\beta_o}{g_m} = \frac{125}{80} = 1.56 \text{ kΩ}$$

From Eq. (6.134),

$$R_i = r_\pi + (1+\beta_o)R_E$$

So

$$1.56 \text{ kΩ} + (1+125)R_E \geq 500 \text{ kΩ}$$

Thus,

$$R_E \geq 3.96 \text{ kΩ}$$

(b) From Eq. (6.137) (also see Table 6.6),

$$A_V = \frac{(1+\beta_o)R_E}{R_s+R_i}$$

$$= \frac{(1+125)3.96}{5+500} = 0.988$$

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$$R_o = \frac{R_s + r_\pi}{1 + \beta_o}$$

$$= \frac{5 + 1.56}{1 + 125} = 52\ \Omega$$

$$R_o' = R_o \,||\, R_E$$

$$= 52\ \Omega \,||\, 3.96\ \text{k}\Omega = 51\ \Omega.$$

Common base (CB) amplifier: Figure 6.37(a) shows a *CB* amplifier using a pnp transistor. A pnp transistor has been used here only for simplicity. A *CB* amplifier is characterized

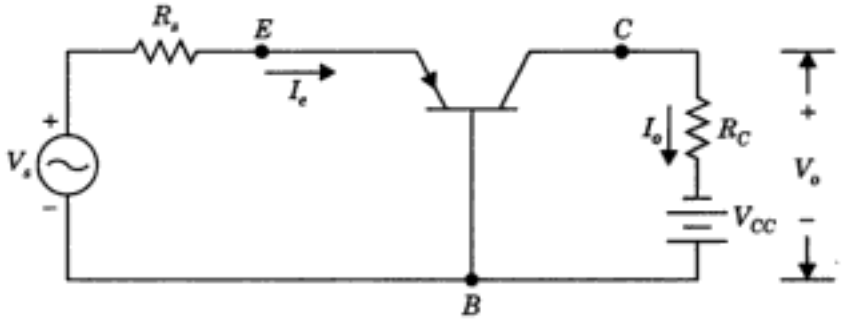


Fig. 6.37(a) A common base amplifier stage (pnp transistor).

by current gain A_I less than unity, voltage gain, A_V high; input impedance R_i is the lowest and output impedance R_o is the highest of the three configurations. This circuit is used to match a very low impedance source to drive a high impedance load or as a constant current source. The ac equivalent circuit obtained by replacing the transistor by its approximate hybrid-π model is shown in Fig. 6.37(b) for analysis. Note that the polarity of voltage drop V_π and direction of current source $g_m V_\pi$ in Fig. 6.37(b) remains same as in the original hybrid-π model.

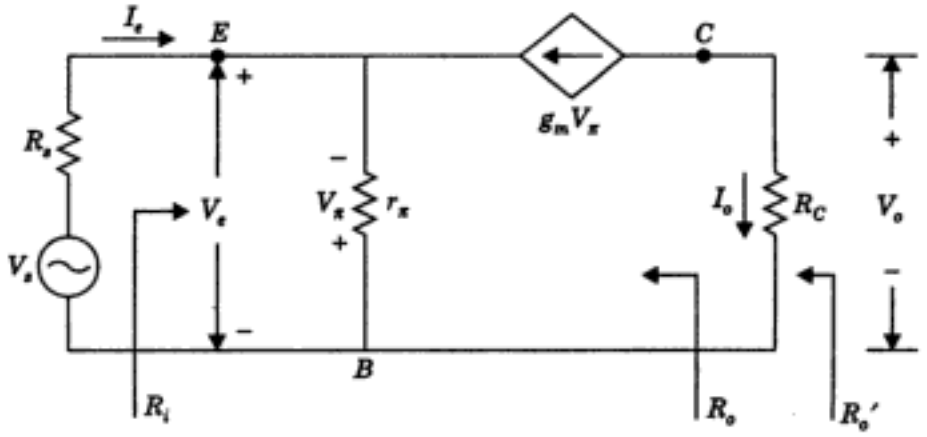


Fig. 6.37(b) ac equivalent circuit of *CB* amplifier stage.

Current gain

In Fig. 6.37(b),

$$I_o = -g_m V_\pi \tag{6.141}$$

and

$$V_\pi = -(I_e + g_m V_\pi) r_\pi \tag{6.142}$$

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Simplifying $V_\pi(1 + g_m r_\pi) = -I_e r_\pi$

$$V_\pi = \frac{-I_e r_\pi}{1 + \beta_o} \tag{6.143}$$

Putting the value of V_π in Eq. (6.141), we obtain

$$I_o = \frac{g_m r_\pi I_e}{1 + \beta_o} \tag{6.144}$$

Now, the current gain:

$$A_I = \frac{I_o}{I_e} = \frac{\beta_o}{1 + \beta_o} \qquad [\because\ g_m r_\pi = \beta_o] \tag{6.145}$$

$$\simeq 1 \tag{6.146}$$

Input resistance, $$R_i = \frac{V_e}{I_e} \tag{6.147}$$

But $$V_e = (I_e + g_m V_\pi) r_\pi$$

$$= (I_e - g_m V_e) r_\pi \qquad (V_e = -V_\pi) \tag{6.148}$$

$$V_e(1 + g_m r_\pi) = I_e r_\pi \tag{6.149}$$

$\therefore$ $$R_i = \frac{V_e}{I_e} = \frac{r_\pi}{1 + \beta_o} \simeq \frac{r_\pi}{\beta_o} \qquad (g_m r_\pi = \beta_o \text{ and } \beta_o >> 1) \tag{6.150}$$

$$= \frac{1}{g_m} \tag{6.160}$$

Voltage gains A_V and A_{V_s}

In Fig. 6.37(b),

$$A_V = \frac{V_o}{V_e} \tag{6.161}$$

$$V_o = I_o R_C \tag{6.162}$$

$$= -g_m V_\pi R_C$$

and $$V_\pi = -V_e$$

Therefore, $$V_o = g_m V_e R_C \tag{6.163}$$

$$A_V = \frac{V_o}{V_e} = g_m R_C \tag{6.164}$$

$$A_{V_s} = \frac{V_o}{V_s} = A_V \frac{V_e}{V_s}$$

$$= A_V \frac{R_i}{R_i + R_s} = g_m R_C \frac{1/g_m}{R_s + R_i} = \frac{R_C}{R_s + R_i} \simeq \frac{R_C}{R_s} \tag{6.165}$$

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Output resistances R_o and R_o'

In Fig. 6.37(b), if $V_s = 0$ then no current flows through r_π which means $V_\pi = 0$. Thus, the current source $g_m V_\pi = 0$, therefore,

$$R_o = \infty \tag{6.166a}$$

and

$$R_o' = R_C \tag{6.166b}$$

The results of a *CB* amplifier using approximate and exact analysis are shown in Table 6.7.

Table 6.7 *CB* Amplifier Stage Results

Quantity	*Approximate*	*Exact* $[R_L = R_C \| r_o]$
A_I	$\frac{\beta_o}{1+\beta_o} \approx 1$	$\frac{\beta_o}{\beta_o + R_C/R_L}$
R_i	$\frac{r_\pi}{1+\beta_o} \approx \frac{1}{g_m}$	$\frac{r_b + r_\pi}{(\beta R_L/R_C)+1}$
A_V	$A_I \frac{R_C}{R_s + R_C} = \frac{R_C}{R_s}$	$\frac{R_L}{R_s + R_i} \times \frac{\beta_o}{1+(\beta_o(R_L/R_C))}$
R_o	∞	$r_o\left[1 + \frac{\beta R_s}{R_s + r_b + r_\pi}\right]$
R_o'	R_C	$R_o \| R_C$

CE amplifier with R_E: The circuit of a *CE* amplifier with a resistance R_E in the emitter branch is shown in Fig. 6.38(a). The important feature of this circuit is that it provides *stability to the voltage gain* and makes its insensitive to the variations of β_o due to device change or temperature. The ac equivalent circuit using approximate hybrid-π model is shown in Fig. 6.38(b).

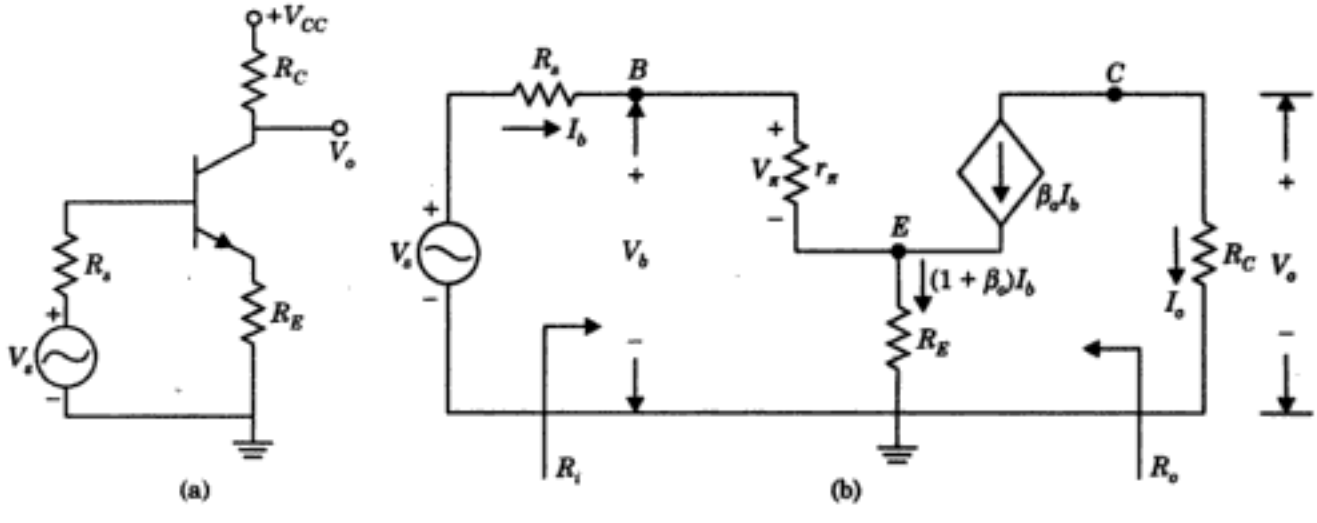


Fig. 6.38 (a) A *CE* amplifier with an emitter resistance, R_E, (b) ac equivalent circuit using approximate hybrid-π model ($r_b = 0$, $r_o = \infty$).

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Current gain

Since
$$I_o = -\beta_o I_b \tag{6.167}$$
$$A_I = \frac{I_o}{I_b} = -\beta_o \tag{6.168}$$

Input resistance R_i

In Fig. 6.38(b),
$$V_b = I_b r_\pi + (1 + \beta_o) I_b R_E \tag{6.169}$$
So
$$R_i = \frac{V_b}{I_b} = r_\pi + (1 + \beta_o) R_E \tag{6.170}$$

The input resistance R_i for this circuit is large as compared to a simple *CE* amplifier.

Voltage gain A_{V_s}

Since
$$V_o = I_o R_C = -\beta_o R_C I_b \tag{6.171}$$
and
$$V_s = I_b(R_s + r_\pi) + (1 + \beta_o) I_b R_E \tag{6.172}$$
Therefore,
$$A_{V_s} = \frac{V_o}{V_s} = \frac{-\beta_o R_C}{R_s + r_\pi + (1 + \beta_o) R_E} \tag{6.173}$$

For $R_E(1 + \beta_o) >> (R_s + r_\pi)$ and $\beta_o >> 1$, Eq. (6.173) reduces to
$$A_{V_s} \cong \frac{-R_C}{R_E} \tag{6.174}$$

Thus, the voltage gain of a *CE* amplifier with R_E is independent of transistor parameters and hence stabilized. However, the voltage of this circuit is less than that of a simple *CE* amplifier. The voltage gain has got reduced due to negative feedback effect of R_E which will be discussed in detail in a later chapter.

Output resistances R_o, R_o'

It can be seen in Fig. 6.38(b), that
$$R_o = \infty \tag{6.175a}$$
and
$$R_o' = R_C \tag{6.175b}$$

EXAMPLE 6.8

The transistor in the circuit shown in Fig. 6.38(a) is biased at $I_C = 0.2$ mA and has $\beta_o = 125$. For $R_s = 2$ kΩ, $R_E = 100$ Ω and $R_C = 5$ kΩ, determine R_i and A_{V_s}.

Solution: First we find the transistor parameters g_m and r_π:
$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.2}{25} = 8\,\text{mV}$$
$$r_\pi = \frac{\beta_o}{g_m} = \frac{125}{8} = 15.6\,\text{k}\Omega$$

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From Eq. (6.170), the input resistance is obtained as:

$$R_i = r_\pi + (1 + \beta_o)R_E$$
$$= 15.6 + (1 + 125)0.1 = 28.2\ \text{k}\Omega$$

A_{Vs}, from Eq. (6.173), is

$$A_{Vs} = \frac{-\beta_o R_C}{R_s + r_\pi + (1 + \beta_o)R_E}$$
$$= \frac{-125 \times 5}{2 + 15.6 + (1 + 125)0.1} = -20.7$$

EXAMPLE 6.9

For the circuit shown in Fig. 6.39 determine r_π, A_I, R_i, A_{Vs}, R_o and R_o'. Given $\beta_o = \beta_F = 200$.

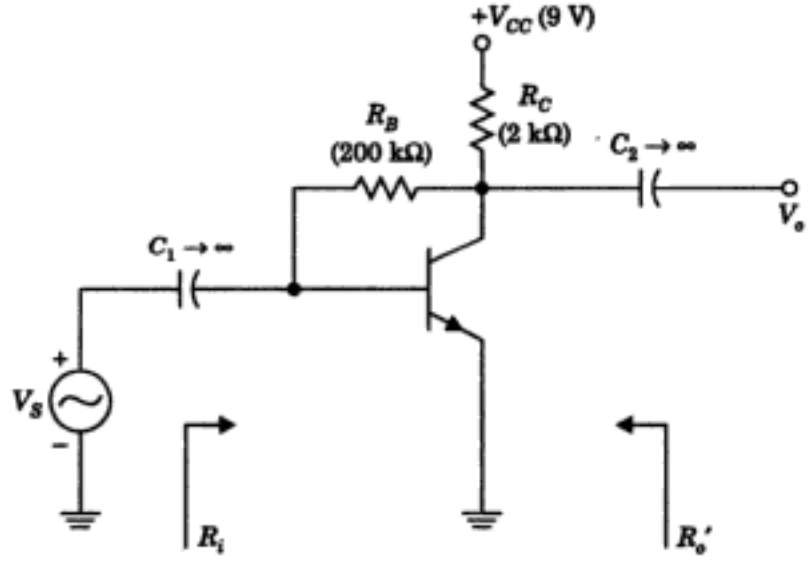


Fig. 6.39 Circuit for Example 6.9.

Solution: In order to calculate r_π, we first find g_m. For this, compute the value of the dc quiescent current, I_{CQ} from the dc equivalent circuit shown in Fig. 6.40(a). Writing KVL from collector to base loop,

$$V_{CC} = R_C(I_C + I_B) + R_B I_B + V_{BE}$$
$$= R_C(\beta_F + 1)I_B + R_B I_B + V_{BE}$$

Solving for I_B, gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta_F)R_C}$$
$$= \frac{9 - 0.7}{200 + (1 + 200)2} = 13.78\ \mu\text{A}$$
$$I_{CQ} = I_C = \beta_F I_B$$
$$= 200 \times 13.78 = 2.756\ \text{mA}$$

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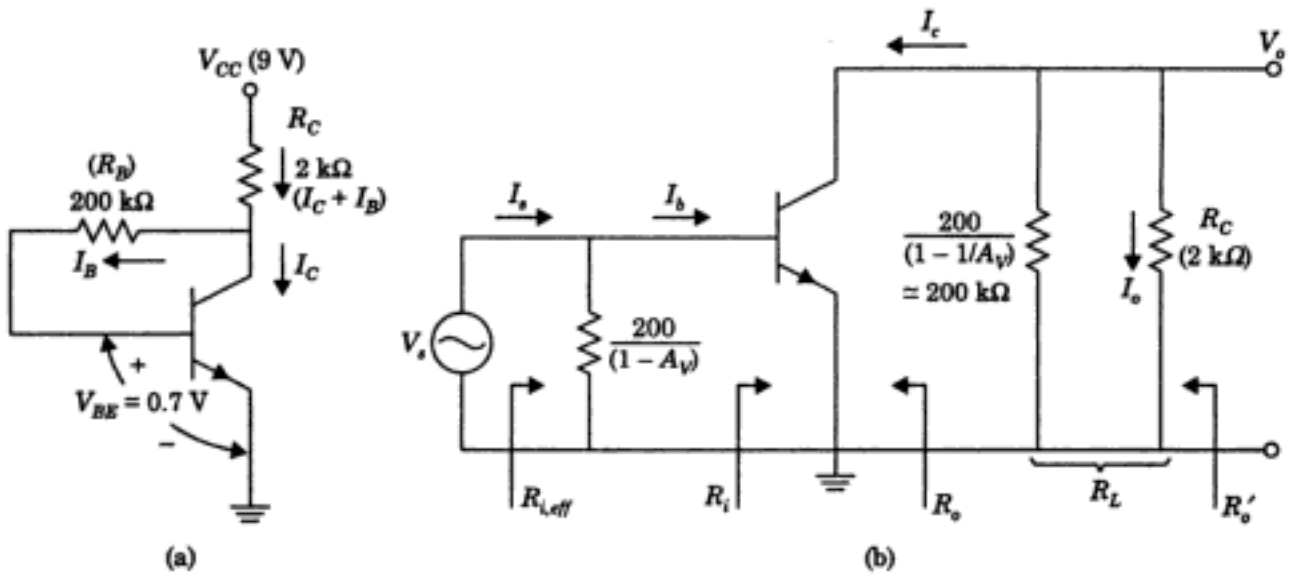


Fig. 6.40 (a) dc equivalent circuit, (b) ac equivalent circuit using Miller's theorem.

and

$$g_m = \frac{I_{CQ}}{V_T} = \frac{2.756}{25} = 0.11\ \Omega$$

Therefore,

$$r_\pi = \frac{\beta_o}{g_m}$$

$$= \frac{200}{0.11\ \Omega} = 1.81\ \text{k}\Omega$$

AC analysis

The ac analysis for finding A_I, A_V, R_i, R_o' for this circuit becomes fairly complicated if done by using the basic principles, i.e., replacing the transistor by its model and writing KCL, KVL equations, due to the presence of feedback resistor R_B. However, the analysis is simplified by using Miller's theorem (see Appendix A6.1 given at the end of the chapter). The ac equivalent circuit where feedback resistance, R_B is replaced by equivalent resistance using Miller's theorem is shown in Fig. 6.40(b). In Fig. 6.40(b),

$$A_V = \frac{V_o}{V_s}$$

To simplify the analysis, assume $A_V >> 1$ which will be usually valid for a *CE* amplifier so that

$$\frac{200}{1 - 1/A_V} = 200\ \text{k}\Omega$$

The effective load resistance now becomes

$$R_L = 200\ \text{k}\Omega \,||\, 2\ \text{k}\Omega$$

$$= 1.98\ \text{k}\Omega$$

Using hybrid-π model and approximate results given in Table 6.5 for a *CE* amplifier stage, we have

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$$A_I = \frac{I_o}{I_b} = \frac{-I_c}{I_b} = -\beta_o = -200$$

$$R_i = r_\pi = 1.81 \text{ k}\Omega$$

and

$$A_V = \frac{V_o}{V_s} = \frac{-\beta_o R_L}{r_\pi}$$

$$= \frac{-200 \times 1.98}{1.81} = -218.78$$

So, our assumption that $A_V >> 1$ is justified.

Since

$$\frac{200}{1 - A_V} = \frac{200}{219.78} = 0.91 \text{ k}\Omega$$

Therefore,

$$R_{i,\text{eff}} = R_i \| 0.91 \text{ k}\Omega$$

$$= \frac{1.81 \times 0.91}{2.72} = 0.6 \text{ k}\Omega$$

and

$$A_I' = \frac{I_o}{I_s} = \frac{V_o}{R_C} \times \frac{R_{i,\text{eff}}}{V_s} = \frac{A_V R_{i,\text{eff}}}{R_C}$$

$$= \frac{-218.78 \times 0.6}{2} = -65.61$$

Also

$$R_o = \infty$$

and

$$R_o' = R_L = 1.98 \text{ k}\Omega$$

6.4.4 Comparison of *CE*, *CC* and *CB* Amplifier Configurations

The analysis of different amplifier configurations has been done by using h-parameter model and hybrid-π model. Analysis can be carried out using any one of the models depending upon the available data. By now, we are also aware of the important features of the three basic amplifier configurations, i.e., *CE*, *CC* and *CB* and also know where to use these. Table 6.8 provides typical numerical values of A_I, R_i, A_V, R_o and R_o' calculated for the three basic BJT configurations for a transistor biased at $I_{CQ} = 2.5$ mA and $\beta_o = 100$, $R_s = 600\ \Omega$, $R_C = R_E = 1.5$ kΩ.

Table 6.8 Comparison of BJT Configurations

Quantity	*CE*		*CC*		*CB*	
$\lvert A_I \rvert$	High	100	High	101	Low	0.990
R_i	Medium	1.0 kΩ	High	153 kΩ	Low	9.90 Ω
$\lvert A_V \rvert$	High	93.8	Low	0.990	Low	2.44
R_o	High	∞	Low	15.8 Ω	High	∞
R_o'	—	1.50 kΩ	—	15.6 Ω	—	1.50 kΩ

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It can be seen from the expressions for A_I, R_i and A_V that all the three quantities are a function of load resistance, R_C (R_E), whereas R_o depends upon the source resistance R_s. It is instructive to study the variation of A_I, R_i, A_V, R_o and R_o' as a function of load resistance R_C (for A_I, R_i, A_V) and source resistance R_s (for R_o, R_o'). The various plots have been shown in Fig. 6.41 for each of the three configurations.

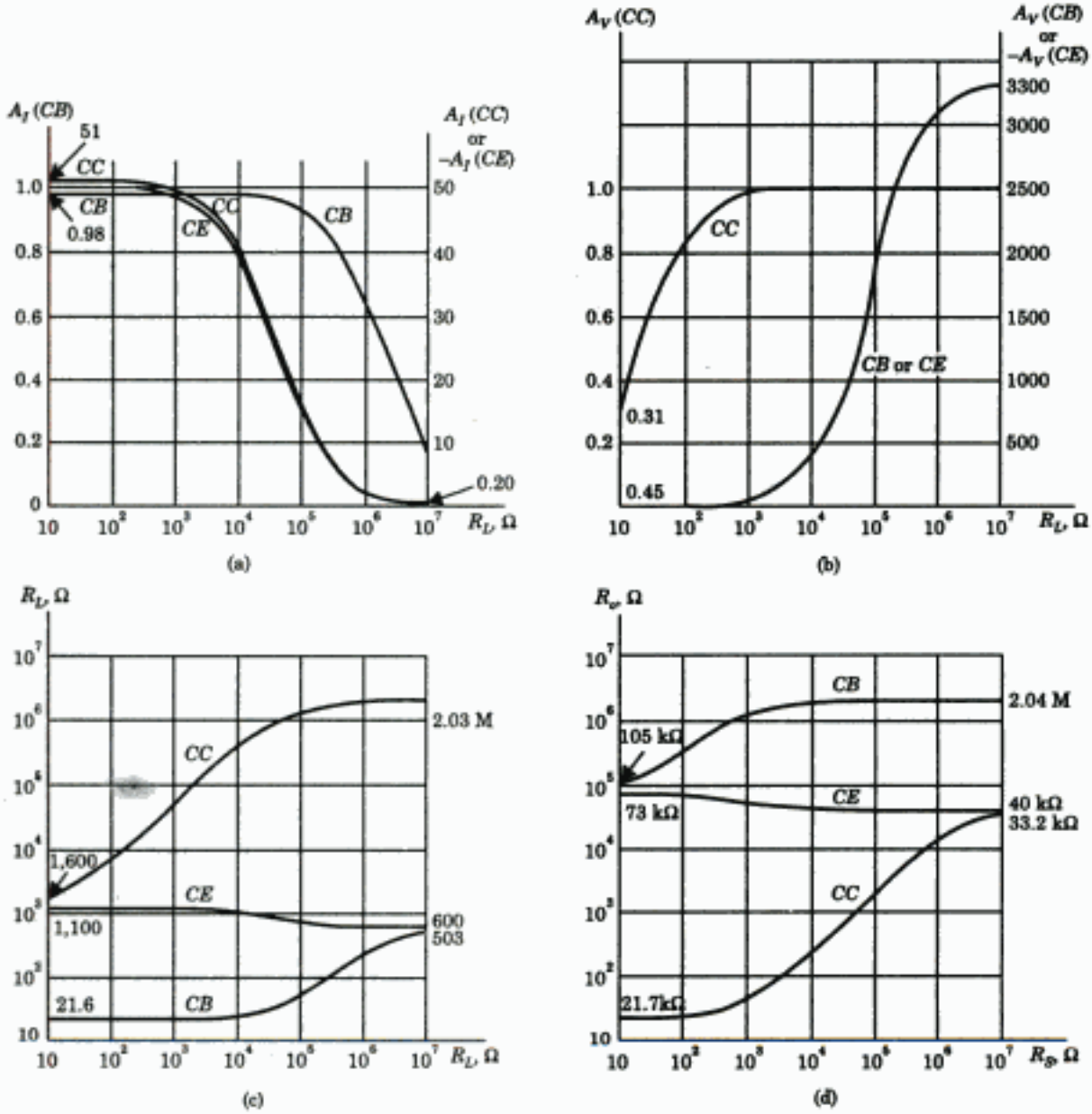


Fig. 6.41 (a) Current gain A_I (b) voltage gain A_V (c) input resistance R_i as a function of load resistance and (d) output resistance R_o as a function of the source resistance, R_s.

All these curves are shown for a typical transistor.

From the plots and the Table 6.8, we may summarize:

***CE* amplifier:** This is the only configuration that provides both voltage gain and the current gain. Therefore, it is the most versatile and useful configuration. Its input and output impedances R_i and R_o are moderate and lies between those for *CC* and *CB* configurations.

***CC* amplifier:** The current gain is high (more than *CE* stage), A_V is less than (but close to) unity, R_i is the highest and R_o is the lowest of the three configurations. Because of its high input resistance and low output resistance, the circuit is used as a buffer stage between a *CE* amplifier and a low resistance load. It is also used in impedance matching applications.

***CB* amplifier:** The current gain is less than unity. A_V is low, R_i is the lowest and R_o is highest of the three configurations. All the above properties are less desirable for signal amplification. Therefore, *CB* configuration is rarely used alone. However, in conjunction with *CE* as in a cascode configuration (CE-CB cascade), it improves or widens the frequency response of a *CE* amplifier and, therefore, is often used in video amplifiers (used in TV).

6.4.5 Transistor Amplifier Analysis Using r_e-model

As earlier discussed in Section 6.1, r_e-model is also sensitive to the dc operating point of the amplifier circuit and, therefore, provides accurate analysis. The use of r_e-model for solving various transistor circuits is now discussed.

CE-amplifier with fixed-bias

The circuit of a *CE* amplifier using fixed-bias is shown in Fig. 6.42(a) and its ac equivalent circuit using r_e-model is shown in Fig. 6.42(b).

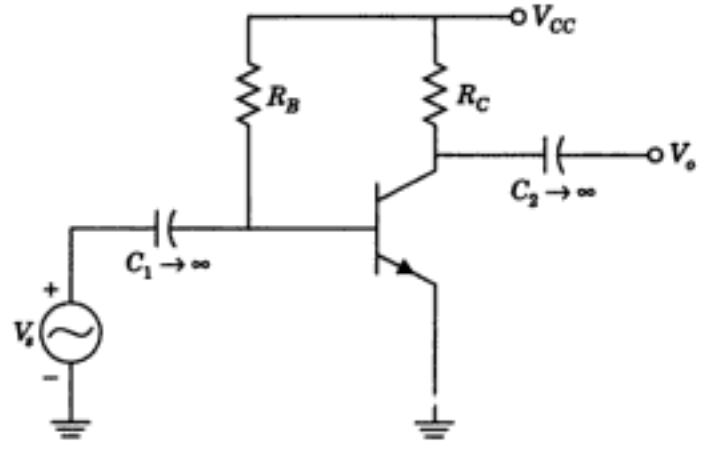


Fig. 6.42(a) A *CE* amplifier with fixed-bias circuit.

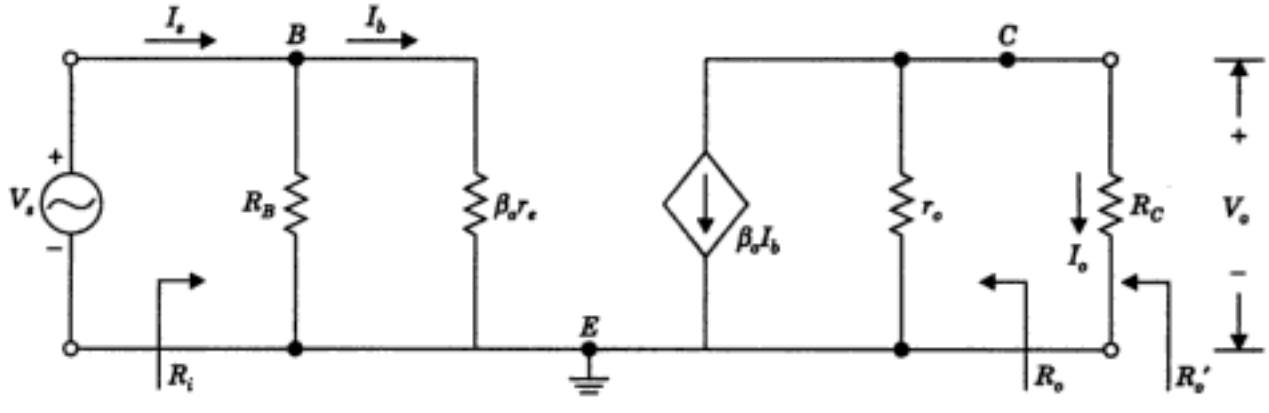


Fig. 6.42(b) ac equivalent circuit using r_e-model.

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Current gain A_I

$$A_I = \frac{I_o}{I_s}$$

$$= \frac{I_o}{I_b} \cdot \frac{I_b}{I_s} \tag{6.176}$$

Applying the current divider rule at the output circuit, we get

$$I_o = -\frac{r_o(\beta_o I_b)}{r_o + R_C} \tag{6.177}$$

So
$$\frac{I_o}{I_b} = -\frac{\beta_o r_o}{r_o + R_C} \tag{6.178}$$

and from the input circuit

$$\frac{I_b}{I_s} = \frac{R_B}{R_B + \beta_o r_e} \tag{6.179}$$

Thus,
$$A_I = \frac{I_o}{I_b} \times \frac{I_b}{I_s}$$

$$= \left(-\frac{r_o \beta_o}{r_o + R_C}\right)\left(\frac{R_B}{R_B + \beta_o r_e}\right)$$

$$= -\frac{\beta_o R_B r_o}{(r_o + R_C)(R_B + \beta_o r_e)} \tag{6.180}$$

Usually, $r_o >> 10R_C$ and $R_B \geq 10\beta_o r_e$

Therefore,
$$A_I \cong -\frac{\beta_o R_B r_o}{r_o R_B}$$

$$\cong -\beta_o \tag{6.181}$$

Input resistance R_i

From Fig. 6.42(b),

$$R_i = R_B \| \beta_o r_e \tag{6.182}$$

For $R_B > 10\beta_o r_e$ as is usually, $R_i \cong \beta_o R_e$

Voltage gain A_V

$$V_o = -\beta_o I_b \, (R_C \| r_o) \tag{6.183}$$

But
$$I_b = \frac{V_i}{\beta_o r_e} \tag{6.184}$$

So
$$V_o = -\beta_o \left(\frac{V_i}{\beta_o r_e}\right)(R_C \| r_o) \tag{6.185}$$

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Thus, $$A_V = \frac{V_o}{V_s} = -\frac{(R_C \| r_o)}{r_e} \tag{6.186}$$

If $$r_o \geq 10R_C$$

Then $$A_V = -\frac{R_C}{r_e} \tag{6.187}$$

Output resistance R_o

To obtain R_o in the circuit, set $V_s = 0$ in Fig. 6.42(b) which makes $I_s = I_b = 0$. This makes the current source, $\beta_o I_B = 0$ that is the current source becomes open and we can write

$$R_o = r_o \tag{6.188}$$

and $$R_o' = r_o \| R_C$$

$$\cong R_C \qquad [r_o \geq 10R_C]$$

Note: For most practical situations, the value of r_o is usually large ($r_o \geq 10R_C$) and therefore, can be neglected in the analysis. If r_o is included, analysis becomes quite complicated and there is very little deviation from the approximate results. In view of this, it is better to adopt a realistic approach and r_o is not included in the model as will be shown by the example that follows:

Unbypassed CE emitter-bias configuration: Figure 6.43(a) shows a self-biased *CE* amplifier with an unbypassed emitter resistor R_E. Its ac equivalent circuit using r_e model is given in Fig. 6.43(b).

Current gain A_I

Applying the current divider rule to the input circuit in Fig. 6.43(b) gives

$$\frac{I_b}{I_s} = \frac{R_B}{R_B + R_i} \quad \text{(where } R_B = R_1 \| R_2\text{)} \tag{6.189}$$

Also, from the output circuit,

$$I_o = -\beta_o I_b$$

So $$\frac{I_o}{I_b} = -\beta_o$$

Since $$A_I = \frac{I_o}{I_b} = \frac{I_o}{I_b} \times \frac{I_b}{I_s}$$

$$= -\beta_o \cdot \frac{R_B}{R_B + R_i} \tag{6.190}$$

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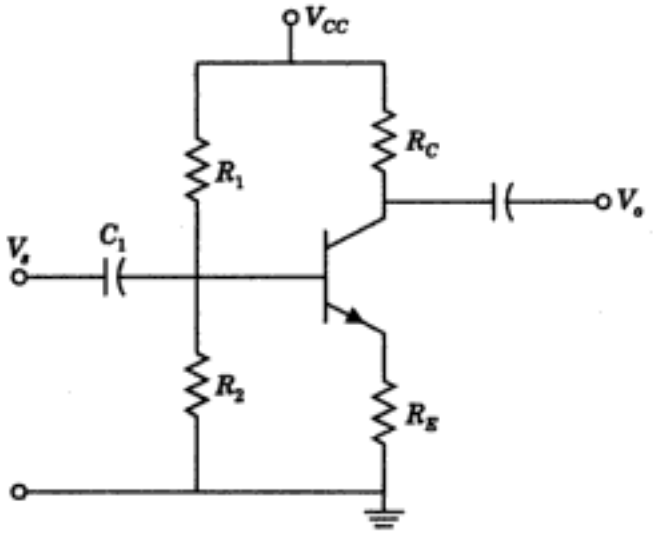


Fig. 6.43(a) *CE* emitter-bias configuration

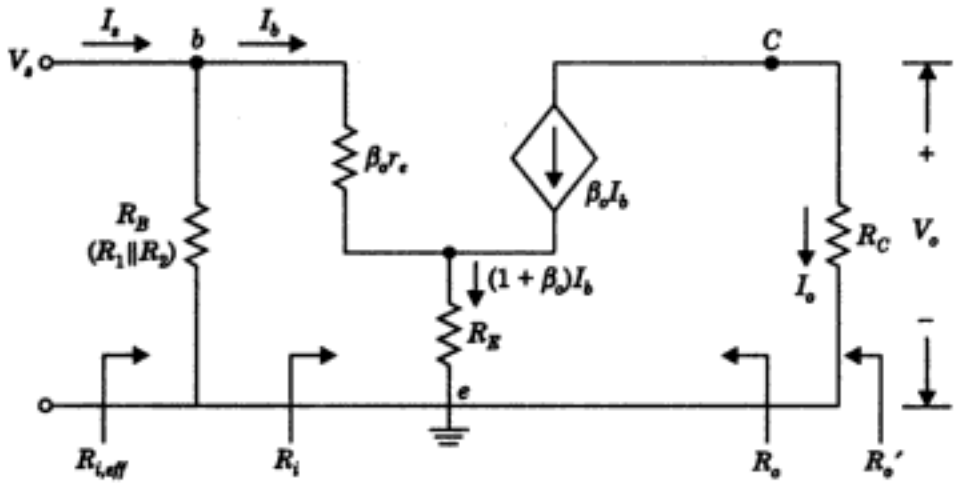


Fig. 6.43(b) AC equivalent circuit.

In Fig. 6.43(b),

$$R_i = \frac{V_s}{I_b}$$

Since
$$V_s = I_b\beta_o r_e + (1 + \beta_o)I_b R_E \tag{6.191}$$

So
$$R_i = \beta_o r_e + (1 + \beta_o)R_E \tag{6.192}$$

Thus,
$$A_I = -\beta_o \frac{R_B}{R_B + \beta_o r_e + (1+\beta_o)R_E}$$

$$\cong -\beta_o \frac{R_B}{R_B + \beta_o(r_e + R_E)} \quad \text{(Since } \beta >> 1\text{)} \tag{6.193}$$

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Input resistance $R_{i,eff}$

In Fig. 6.43(b),

$$R_{i,eff} = R_B \| R_i \tag{6.194}$$

Voltage gain A_V

$$V_o = -I_o R_C \tag{6.195}$$

and

$$V_s = I_b R_i \tag{6.196}$$

$$A_V = \frac{V_o}{V_s} = \frac{I_o R_C}{I_b R_i} = -\frac{\beta_o I_b R_C}{I_b R_i} \qquad (\because\ I_o = \beta_o I_b)$$

$$= -\frac{\beta_o R_C}{\beta_o r_e + (1+\beta_o) R_E}$$

$$\cong -\frac{R_C}{R_E} \qquad (\beta_o >> 1,\ \beta_o R_E >> \beta_o r_e) \tag{6.197}$$

Output resistance R_o

It is easily seen that

$$R_o = \infty \tag{6.198}$$

and

$$R_o' = R_C$$

Results if r_o is included

The results appearing below clearly reveal the additional complexity resulting from including r_o in the analysis.

$$R_i = \beta_o r_e + \left[\frac{(1+\beta_o) + R_C/r_o}{1 + (R_C + R_E)/r_o}\right] R_E \tag{6.199}$$

$$R_o = r_o + \frac{\beta_o (r_o + r_e)}{1 + \beta \dfrac{r_e}{R_E}} \tag{6.200}$$

$$A_V = \frac{-\dfrac{\beta_o R_C}{R_i}\left[1 + \dfrac{r_e}{r_o}\right] + \dfrac{R_C}{r_o}}{1 + \dfrac{R_C}{r_o}} \tag{6.201}$$

and

$$A_I = \frac{A_V R_i}{R_C} \tag{6.202}$$

Exact expression for A_I can be obtained by using the above equations.

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If we let $r_o \to \infty$ in the results given in Eq. (6.199) to Eq. (6.202) we obtain the results as derived earlier ignoring r_o.

EXAMPLE 6.10

For the circuit shown in Fig. 6.44, determine $R_{i,eff}$, R_o, A_V and A_I, for transistor data given as $\beta_o = \beta_F = 200$, $r_o = 50$ kΩ.

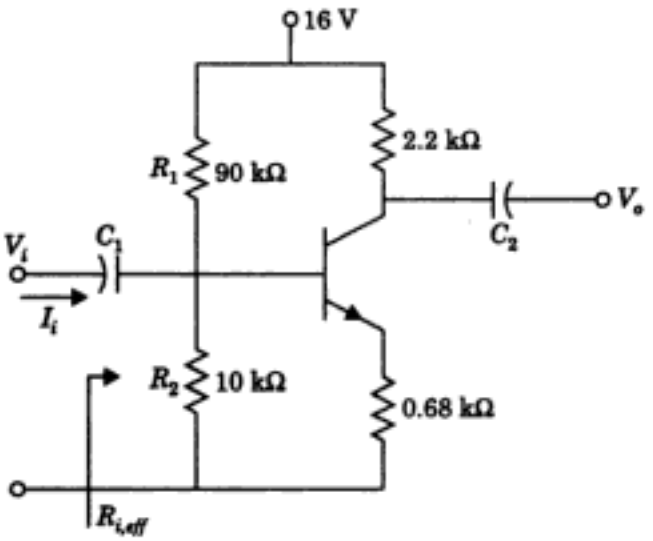


Fig. 6.44 Circuit for Example 6.10.

Solution: The question can be solved by using hybrid-π model. However, here we solve it using r_e-model. First perform the dc analysis to obtain r_e. Under dc conditions, capacitors C_1 and C_2 will be open circuited, as shown in the Thevenin's equivalent circuit of Fig. 6.45(a).

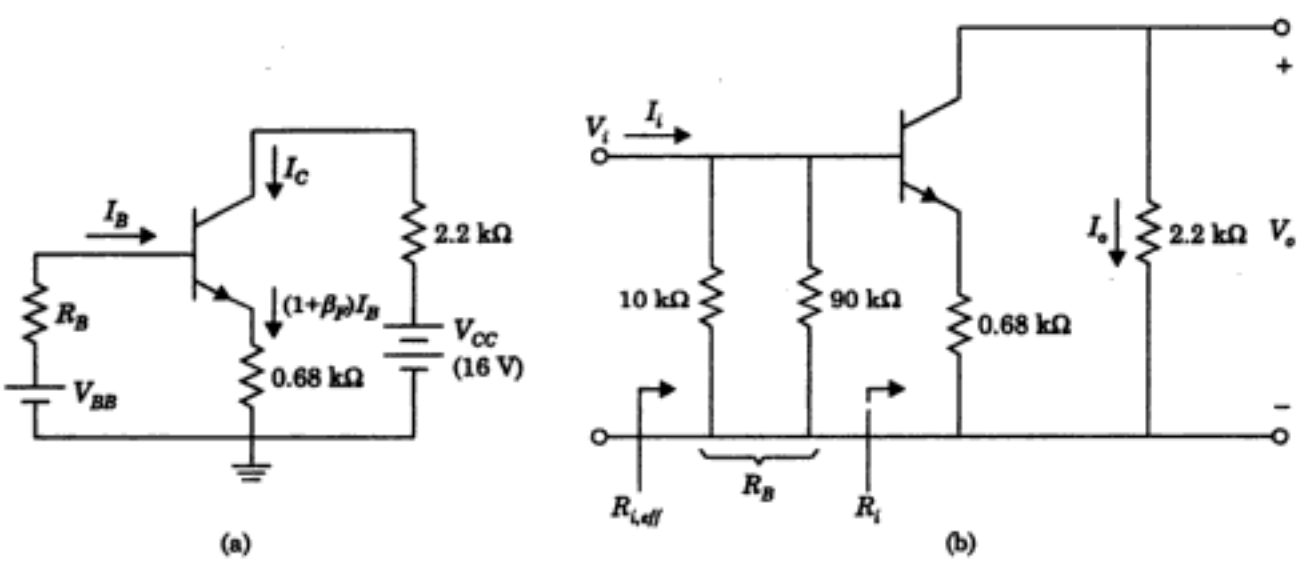


Fig. 6.45 (a) dc equivalent circuit for finding r_e (b) ac equivalent circuit.

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In Fig. 6.45(a),

$$R_B = R_1 \| R_2$$
$$= 90\ \text{k}\Omega \| 10\ \text{k}\Omega$$
$$= 9\ \text{k}\Omega$$

and
$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC}$$
$$= \frac{10}{90+10}(16) = 1.6\ \text{V}$$

From the base loop,

$$V_{BB} - V_{BE} = I_B R_B + (1 + \beta_F) I_B R_E$$
$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (1+\beta_F) R_E}$$
$$= \frac{1.6 - 0.7}{9 + 201 \times 0.68} = .006\ \text{mA}$$
$$I_C = \beta_F I_B$$
$$= 200 \times .006 = 1.2\ \text{mA}$$
$$I_E = I_C + I_B = 1.206\ \text{mA} = I_{EQ}$$

So
$$r_e = \frac{V_T}{I_{EQ}}$$
$$= \frac{26}{1.206} = 21.55\ \Omega$$

The ac equivalent circuit is shown in Fig. 6.45(b). In this circuit, transistor has not been replaced by transistor model, as the analysis has already been carried out in section 6.3.5 and the results derived earlier can be used.

Input resistance $R_{i,eff}$

R_i from Eq. (6.192) is:

$$R_i = \beta_o r_e + (1 + \beta_o) R_E$$
$$= 200 \times 21.55 + 201 \times 0.68$$
$$= 4.31 + 136.68$$
$$= 140.99\ \text{k}\Omega$$

and
$$R_{i,eff} = R_B \| R_i$$
$$= 9\ \text{k}\Omega \| 140.99\ \text{k}\Omega$$
$$= 8.45\ \text{k}\Omega$$

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Current gain A_I

From Eq. (6.193),

$$A_I = -\frac{\beta_o R_B}{R_B + \beta_o(r_e + R_E)} = -\frac{200 \times 9}{9 + 140.99} = -12$$

Voltage gain A_V

From Eq. (6.197),

$$A_V = -\frac{R_C}{R_E}$$

$$= -\frac{2.2}{0.68} = -3.24$$

Emitter follower with fixed-bias: Figure 6.46 shows the circuit diagram of a emitter follower using fixed-bias. The ac equivalent circuit using r_e-model for the transistor is shown in Fig. 6.47(a).

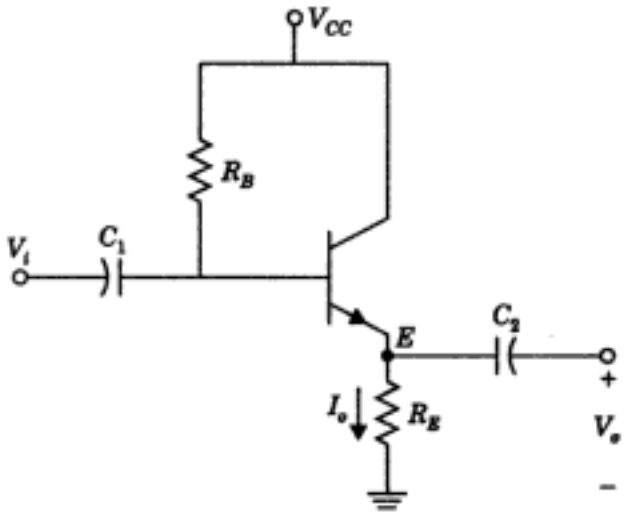


Fig. 6.46 Emitter follower with fixed-bias.

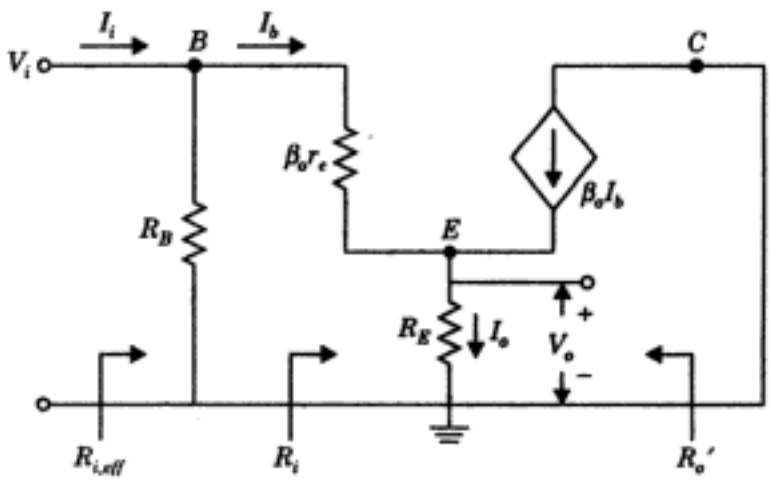


Fig. 6.47(a) ac equivalent circuit of the circuit shown in Fig. 6.46.

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Input resistance $R_{i,eff}$

Since
$$R_i = \frac{V_i}{I_b} = \frac{I_b[\beta_o r_e + (1+\beta_o)R_E]}{I_b}$$
$$= \beta_o r_e + (1+\beta_o)R_E \tag{6.203}$$

So
$$R_{i,eff} = R_B || R_i'$$

Current gain A_I

In Fig. 6.47(a),
$$\frac{I_b}{I_i} = \frac{R_B}{R_B + R_i}$$

and
$$I_o = (1+\beta_o)I_b$$

Thus,
$$\frac{I_o}{I_b} = (1+\beta_o)$$

Since
$$A_I = \frac{I_o}{I_i} = \frac{I_o}{I_b} \cdot \frac{I_b}{I_i}$$

We get
$$A_I = (1+\beta_o)\frac{R_B}{R_B + R_i} \tag{6.204}$$
$$\cong \frac{\beta_o R_B}{R_B + R_1} \tag{6.205}$$

Voltage gain A_V

Since
$$V_o = (1+\beta_o)I_b R_E \tag{6.206}$$

and
$$V_i = I_b[\beta r_e + (1+\beta_o)R_E] \tag{6.207}$$

Therefore,
$$A_V = \frac{V_o}{V_i} = \frac{(1+\beta_o)R_E}{\beta_o r_e + (1+\beta_o)R_E}$$
$$\cong \frac{\beta_o R_E}{\beta_o r_e + \beta_o R_E} \qquad (\text{for } \beta_o >> 1)$$
$$= \frac{R_E}{r_e + R_E} \tag{6.208}$$

As expected, the voltage gain of the emitter follower is less than unity and there is no phase change between the input and the output voltages.

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Output impedance R_o

To determine R_o, set $V_s = 0$ and $R_E = \infty$. Applying a test voltage source V between the emitter and ground, it can be seen from the equivalent circuit shown in Fig. 6.47(b) that the current drawn by the circuit is given by

$$I = (1 + \beta_o)I_b$$

and $$V = \beta_o r_e I_b$$

Therefore, $$R_o = \frac{V}{I} = \frac{\beta_o r_e I_b}{(1 + \beta_o)I_b} \quad (6.209)$$

$$= \frac{\beta_o r_e}{1 + \beta} \simeq r_e \quad (6.210)$$

Thus, $$R_o' = R_E || r_e$$

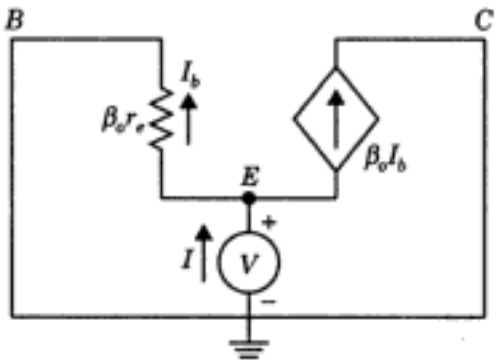


Fig. 6.47(b) Equivalent circuit for finding R_o, R_o'.

Effect of r_o

The following relations can be verified when r_o is taken into account:

$$R_i = \beta_o r_e + \frac{(1 + \beta_o)R_E}{1 + \frac{R_E}{r_o}}$$

If $$r_o \geq 10R_E$$

Then

$$R_i = \beta_o r_e + (1 + \beta_o)R_E \quad (6.211)$$

which is same as Eq. (6.203)

$$R_o = r_o || R_E || \frac{\beta_o r_e}{1 + \beta_o}$$

$$\cong r_o || R_E || r_e \quad [\text{for } \beta_o >> 1] \quad (6.212)$$

For $r_o >> r_e$ which is usually the case,

$$R_o \cong R_E || r_e$$

Common base (CB) configuration: The circuit diagram of *CB* amplifier is shown in Fig. 6.48(a) and its ac equivalent circuit with transistor replaced by common base r_e equivalent model is shown in Fig. 6.48(b). A *CB* amplifier is characterized by low input impedance (lowest of the three configurations) and high output impedance, and current gain almost equal to unity (but < 1). The voltage gain, however, can be quite large. Its main application is in cascode amplifier (*CE–CB* cascode) which is used in video amplifiers to increase the bandwidth.

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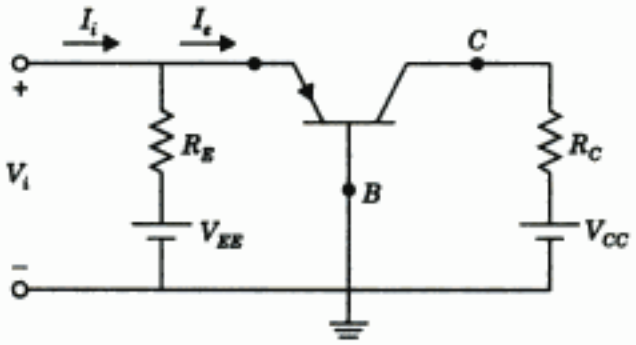


Fig. 6.48(a) Common base amplifier (using *pnp* transistor).

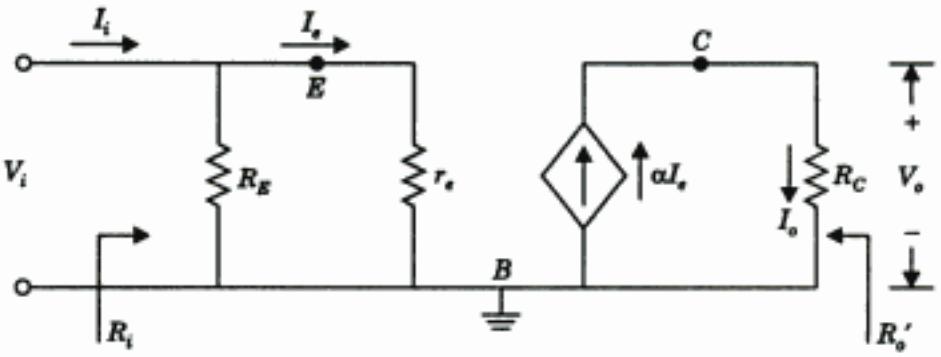


Fig. 6.48(b) ac equivalent circuit.

It may be noted that the output resistance r_o has not been included in the model as it is usually large (in mega ohms only) in comparison to R_C and can be neglected without causing large errors.

Current gain A_I

From Fig. 6.48(b), we may write

$$\frac{I_e}{I_i} = \frac{R_E}{R_E + r_e} \tag{6.213}$$

and

$$I_o = +\alpha I_e \tag{6.214}$$

Therefore,

$$A_I = \frac{I_o}{I_i} = \frac{I_o}{I_e} \cdot \frac{I_o}{I_i}$$

$$= \alpha \frac{R_E}{R_E + r_e}$$

$$\cong \alpha \quad [\text{For } r_e << R_E \text{ as is usually the case}] \tag{6.215}$$

Thus, the current gain of a *CB* amplifier is less than unity.

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Input impedance, R_i

From Fig. 6.48(b), $$R_i = R_E || r_e \tag{6.216}$$

Voltage gain A_V $$V_o = I_o R_C$$

$$= \alpha I_e R_C \tag{6.217}$$

Also $$I_e = \frac{V_i}{r_e} \tag{6.218}$$

So $$V_o = \frac{\alpha R_C V_i}{r_e}$$

Thus $$A_V = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e} \tag{6.219}$$

Note that V_o and V_i are in phase for *CB* amplifier. The value of r_e for *CB* configuration is very low (typically 20 Ω). Therefore, it is possible to obtain large voltage gain even for small values of load R_C.

It can be seen by inspection that the output resistance is given by

$$R_o = \infty \quad \text{and} \quad R_o' = R_C$$

APPENDIX 6.1

Miller's Theorem

There are amplifier circuits in which a feedback resistance is connected between the output node and the input node. As an example, in a CE amplifier using collector to base biasing circuit, a resistance R_B is connected between collector and base. The analysis of such a circuit for finding A_I, A_V, R_i and R_o becomes complicated. Such circuits are easily analysed by using Miller's Theorem.

Consider a general network shown in Fig. A6.1(a) where V_1, V_2 ..., V_N are the voltages at nodes 1, 2, ..., N and $V_N = 0$ as node N is considered as the reference node. An impedance Z is connected between nodes 1 and 2.

It can be shown that the impedance Z can be replaced by equivalent impedances $Z_1 = Z/(1 - A_V)$ connected between node 1 and ground terminal N and an impedance $Z_2 = Z/(1 - 1/A_V)$ connected between node 2 and terminal N. The equivalent circuit so obtained is shown in Fig. A6.1(b).

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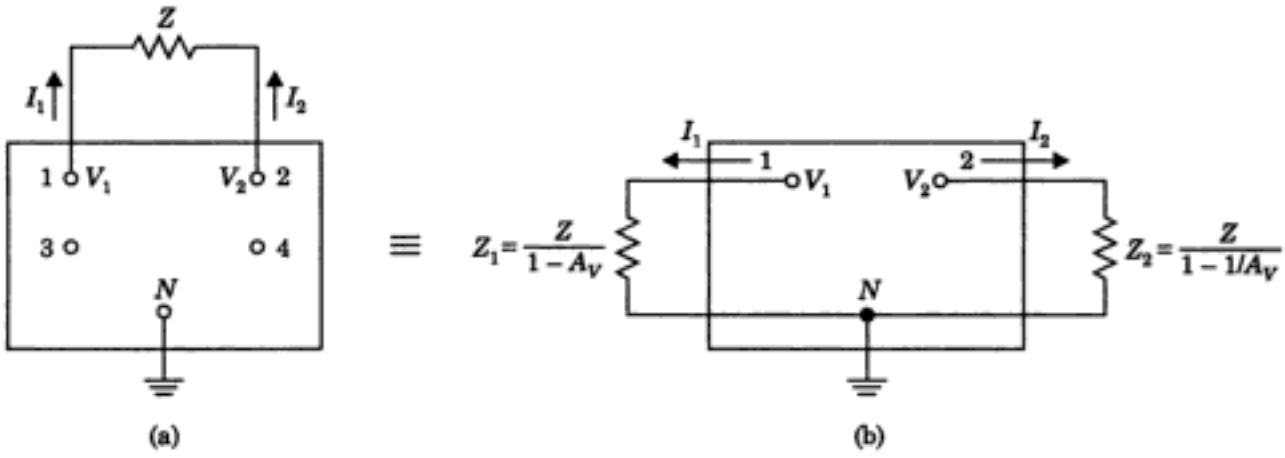


Fig. A6.1 (a) A general network, (b) Equivalent circuit using Miller's theorem, where $A_V = V_2/V_1$.

The current I_1 in Fig. A6.1(a) is given by

$$I_1 = \frac{V_1 - V_2}{Z} = \frac{V_1(1 - V_2/V_1)}{Z}$$

$$= \frac{V_1(1 - A_V)}{Z} = \frac{V_1}{Z/(1 - A_V)}$$

$$= \frac{V_1}{Z_1} \quad [Z_1 = Z/(1 - A_V)]$$

Thus, if $Z_1 = Z/(1 - A_V)$ is placed across the terminal 1 and N as shown in Fig. A6.1(b), the current drawn from node 1 would be same as that in the original circuit of Fig. A6.1(a). In a similar way, it can be shown that the current I_2 drawn from node 2 remains same even if the impedance Z is replaced by an equivalent impedance $Z_2 = Z/(1 - 1/A_V)$ between the node 2 and ground as shown in Fig. A6.1(b).

SUMMARY

- There are three small signal models used for the transistor analysis and design: h-parameter model, hybrid-π model and r_e (or T-) model.
- Hybrid-π and r_e-model parameters are dependent upon the dc operating conditions of the circuit and, therefore, provide accurate analysis. Analysis using h-model is not very accurate as its parameters are available only at a typical operation point.
- The important h-parameters are: h_i (input impedane); h_f (short circuit current gain); h_r (reverse voltage gain) and h_o (output conductance).
- The h-parameters are hybrid (or mixed) parameters as two parameters are short circuit parameters and two are open circuit parameters.

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- Given h-parameters for any one configuration, the parameters for other configurations can be obtained by using conversion formulas.
- Approximate h-model described by only h_{ie} and h_{fe} can be used for $h_{oe}R_L \leq 0.1$.
- A transistor is modelled as a current controlled current source in h-parameter model, and as a voltage controlled current source in hybrid-π model.
- The quantities of interest in any amplifier are: A_I, A_V, A_{Vs}, A_{Is}, R_i, R_o and R_o', indicating current gain, voltage gain, input and output impedances of the circuit.
- A *CE* amplifier provides large current gain and voltage gain. It has medium input impedance and high output impedance. It is the most versatile amplifier configuration.
- A *CC* amplifier, also known as **emitter follower** has large current gain, unity voltage gain, high input impedance and low output impedance. Its main application is as a buffer stage or impedance matching circuit.
- A *CB* amplifier provides unity current gain, moderate voltage gain, very low input impedance and high output impedance. The circuit is rarely used alone, however along with *CE* amplifier such as a cascode circuit (*CE-CB* cascode), it is used in video amplifiers to provide wide frequency response.

REVIEW QUESTIONS

6.1 Name the three small signal models used for a BJT. Which of the three models of a BJT provide accurate analysis and why?

6.2 Define the various h-parameters and give their units.

6.3 What is the alternative notations for 11, 12, 21 and 22 in h-parameters. Who gave these notations?

6.4 Explain how to calculate *CE*-h-parameters from the input and output characteristics.

6.5 List the advantages of using h-parameter model.

6.6 Prove the conversion formulae for h-parameters from *CE* to *CB* given in Table 6.2.

6.7 Draw the h-parameter model of a BJT for (i) *CE*, (ii) *CB* and (iii) *CC* configurations.

6.8 Draw hybrid-π model and explain the physical significance of various parameters used in it.

6.9 Define transconductance g_m and derive the expression for it.

6.10 Derive a relationship between β_o, r_π and g_m.

6.11 Draw the r_e-model for a BJT in (i) *CB* and (ii) *CE* configuration. Compare hybrid-π model to the r_e-model of a transistor.

6.12 List the steps followed for drawing the ac equivalent circuit for a transistor amplifier.

6.13 Give the exact formulas for A_I, R_i, A_V, R_o and R_o' of a *CE* amplifier.

6.14 Explain how circuit compute the value of r_π and g_m of a transistor.

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6.15 Derive the expression for the output resistance of an emitter follower using short circuit current and open circuit voltage method.

6.16 Draw a CE amplifier circuit that stabilizes voltage gain. Prove it.

6.17 Compare the important characteristics of *CE*, *CC* and *CB* amplifiers.

6.18 Which of the three BJT configurations has (i) highest R_i, (ii) lowest R_i, (iii) highest R_o, (iv) lowest R_o, (v) highest A_V and (vi) lowest A_V.

6.19 Explain Miller's theorem.

6.20 A high gain amplifier with high input resistance and high output resistance has to be designed. If a three-stage cascade is used, what configuration should be used for each stage? Explain.

NUMERICAL PROBLEMS

Using h-parameters

P6.1 (a) Derive the *CC* *h*-parameters in terms of *CE* *h*-parameters.

(b) Derive the *CE* *h*-parameters in terms of *CB* *h*-parameters.

P6.2 Given a single stage *CC* transistor amplifier, with $R_s = R_E = 10$ kΩ, calculate A_I, A_V, A_{Vs}, R_i and R_o. Take the values of *h*-parameters from Table 6.1.

(Ans. 40.8, 0.998, 0.974, 409.1 kΩ, 217 Ω)

P6.3 (a) Draw the ac equivalent circuit of *CE* and *CC* amplifiers subject to $R_L = 0$. Show that the input impedances of the two circuits are identical.

(b) Draw the circuits for *CE* and *CC* amplifiers with the input open circuited. Show that the output impedances of the two circuits are identical.

P6.4 For any single stage amplifier prove that

$$R_i = \frac{h_i}{1 - h_r A_V}$$

P6.5 Prove that

$$Y_o = h_o \left(\frac{R_s + R_{i\infty}}{R_s + R_{io}} \right)$$

where $R_{i\infty} = R_i$ for $R_L = \infty$

and $R_{io} = R_C$ for $R_L = 0$.

P6.6 For the circuit shown in Fig. 6.55 verify that the modified *h*-parameters are:

$$h_{ie}' = h_{ie} + \frac{(1 + h_{fe})R_E}{1 + h_{oe}R_E}$$

$$h_{re}' = \frac{h_{re} + h_{oe}R_E}{1 + h_{oe}R_E}$$

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$$h_{fe}' = \frac{h_{fe} - h_{oe}R_E}{1 + h_{oe}R_E}$$

$$h_{oe}' = \frac{h_{oe}}{1 + h_{oe}R_E}$$

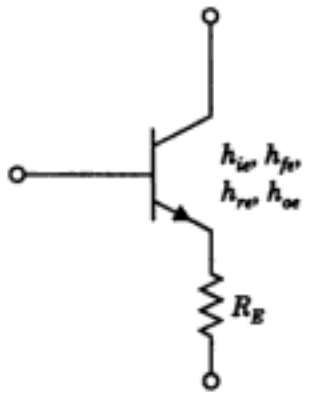


Fig. 6.55 Circuit for P6.6.

P6.7 For the transistor amplifier shown in Fig. 6.56 compute $A_V = V_o/V_s$, $A_i = I_L/I_s$, R_i and R_o'. Assume $h_{ie} = 1$ kΩ, $h_{fe} = 100$.

(***Ans.*** –46.5, –43.4, 0.86 kΩ, 1 kΩ)

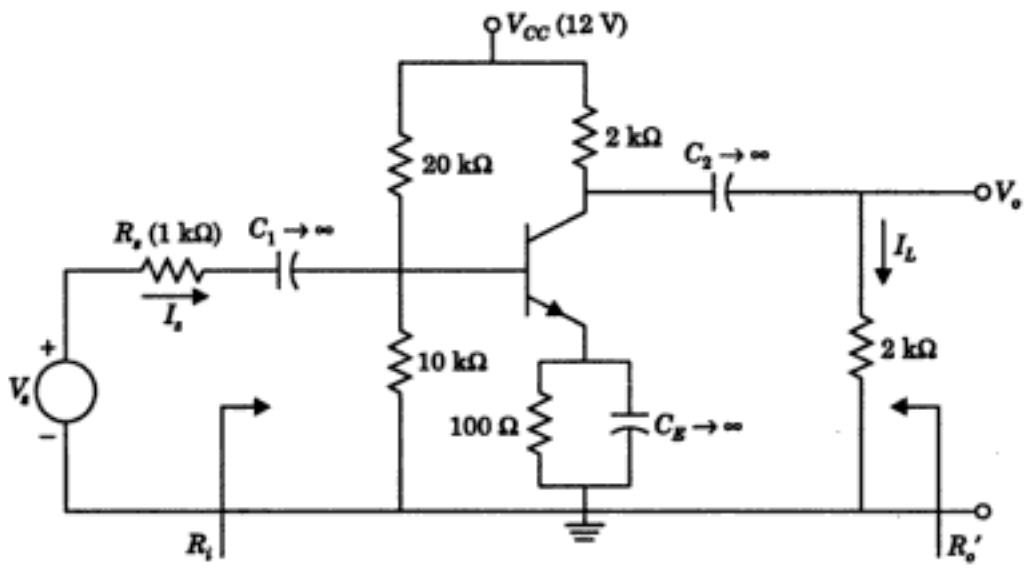


Fig. 6.56 Circuit for P6.7.

P6.8 Design an emitter follower (i.e. find R_s and R_E) with $R_i = 500$ kΩ and $R_o = 20$ Ω. Assume $h_{fe} = 50$, $h_{ie} = 1$ kΩ, $h_{oe} = 25$ μA/V.

(***Ans.*** 20 Ω, 13 kΩ)

P6.9 For the emitter follower in Problem 6.8, find A_i and A_V.

(***Ans.*** 38.5)

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P6.10 For the amplifier shown in Fig. 6.57 the transistor parameters are given as: h_{ie} = 1.1 kΩ, h_{fe} = 50, h_{oe} = 2.5 μA/s, and $h_{re} = 2.5 \times 10^{-4}$. Find $A_{Vs} = V_o/V_s$, $A_I' = I_o/I_s$.

(***Ans.*** –12.7, –13.15)

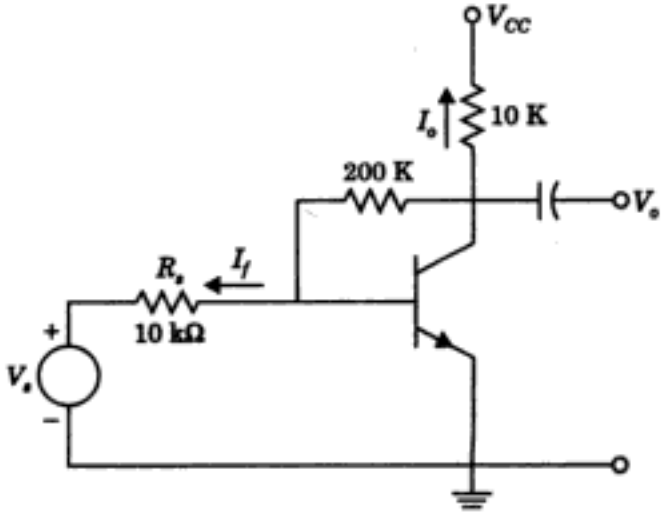


Fig. 6.57 Circuit for P6.10.

P6.11 The transistor of CE amplifier shown in Fig. P6.58 has the following parameters: h_{fe} = 120, $h_{ie} = 0.02/I_B$; $h_{re} = h_{oe} = 0$. Compute (i) h_{ie} (ii) $A_V = V_o/V_i$.

(***Ans.*** 833 Ω, –123.45)

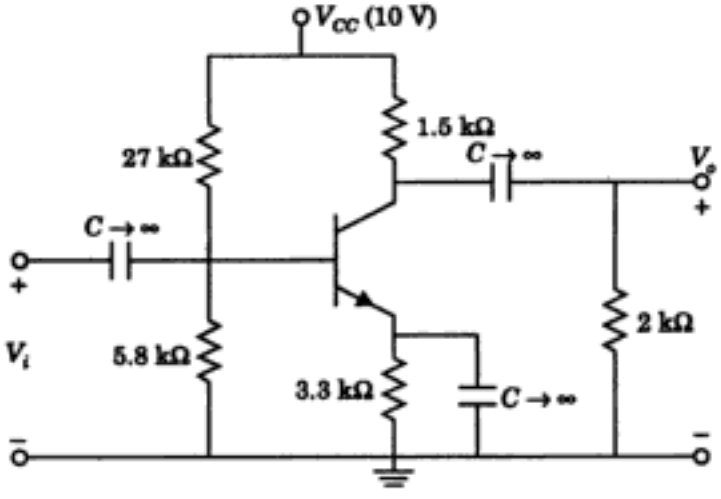


Fig. 6.58 Circuit for P6.11.

Using hybrid-π model (or r_e-model)

P6.12 A *CE* amplifier stage uses an *npn* transistor having β_o = 125 and is biased at I_{CQ} = 1 mA. If R_s = 300 Ω, R_C = 1.2 kΩ, determine A_V and R_i.

(***Ans.*** –43.78, 3.425 kΩ)

P6.13 An emitter follower uses a *pnp* transistor with β_o = 150 and biased at I_{CQ} = –0.25 mA is driven from a source of 3 kΩ resistance.

(a) Find the value of R_E so that R_o' = 110 Ω.

(b) Using the value of R_E in (a), determine A_V and R_i.

(***Ans.*** 1.42 kΩ, 0.924)

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P6.14 A *CE* amplifier shown in Fig. 6.59 is biased to operate at $I_C = 0.1$ mA. The transistor has $\beta_0 = 100$ and large V_A. Find R_i, $A_{Vs} = (V_o/V_s)$ and R_o for $R_C = 47$ kΩ and $R_s = 100$ kΩ.

(***Ans.*** 25 kΩ, –37.6, 47 kΩ)

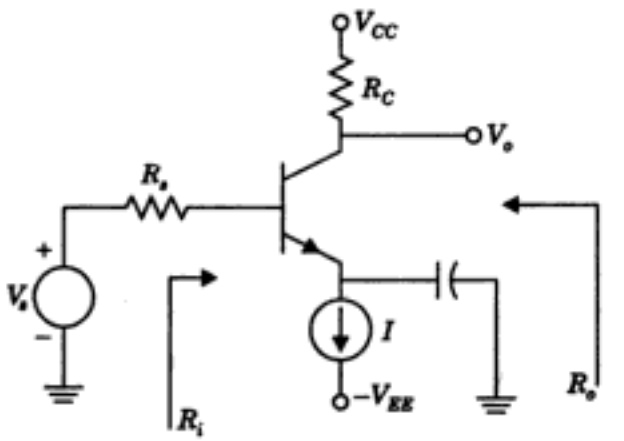


Fig. 6.59 Circuit for P6.14

P6.15 A *CE* amplifier shown in Fig. 6.60 uses a transistor with $\beta = 100$ and $V_A = 100$ V.
(a) Calculate the dc bias current I_E.
(b) Calculate R_i, $A_{Vs} = V_o/V_s$ and $A_I = I_L/I_i$.

(***Ans.*** (a) $I_E = 1.94$ mA, (b) 1.15 kΩ, –8.13, –45.3)

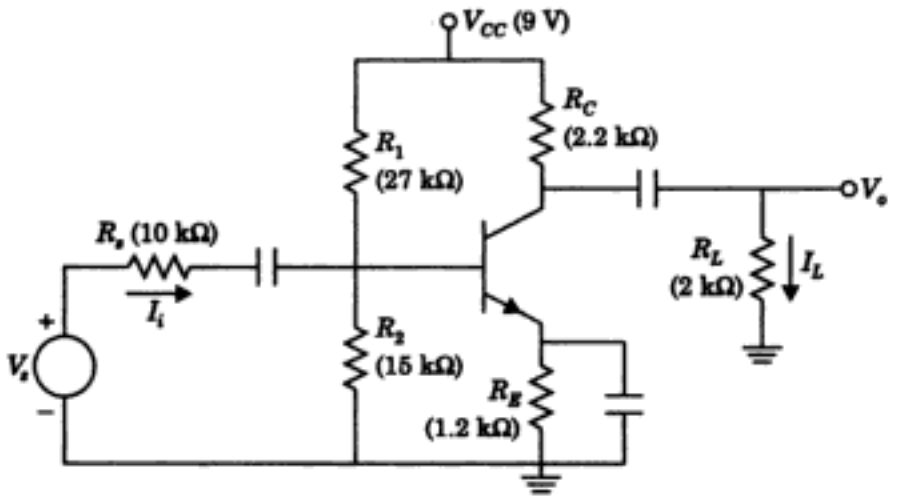


Fig. 6.60 Circuit for P6.15.

P6.16 A *CE* amplifier with a resistance in the emitter uses a transistor biased at 0.2 mA and having a $\beta = 125$. Given: $R_s = 2$ kΩ, $R_E = 100$ Ω, $R_C = 5$ kΩ, determine A_V, R_i.

(***Ans.*** –20.7, 15.7 kΩ)

P6.17 An emitter follower uses an *npn* transistor biased at $I_{CQ} = 2$ mA and has a $\beta = 125$. It is desired that $R_i \geq 500$ kΩ. Find (a) R_E, (b) A_V, R_o and R_o' for $R_s = 5$ kΩ.

(***Ans.*** 3.96 kΩ, 0.988, 52 Ω, 51 Ω)

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P6.18 In the circuit shown in Fig. 6.61, transistor used has $\beta = 100$.

(a) Find the value of R_E to establish a dc emitter current of about 1 mA.

(b) Find R_C to establish a dc collector voltage of about +5 V.

(c) For $R_L = 5$ kΩ and transistor $r_o = 100$ kΩ, determine the overall voltage gain.

(***Ans.*** 14.3 kΩ, 10 kΩ, –64.5)

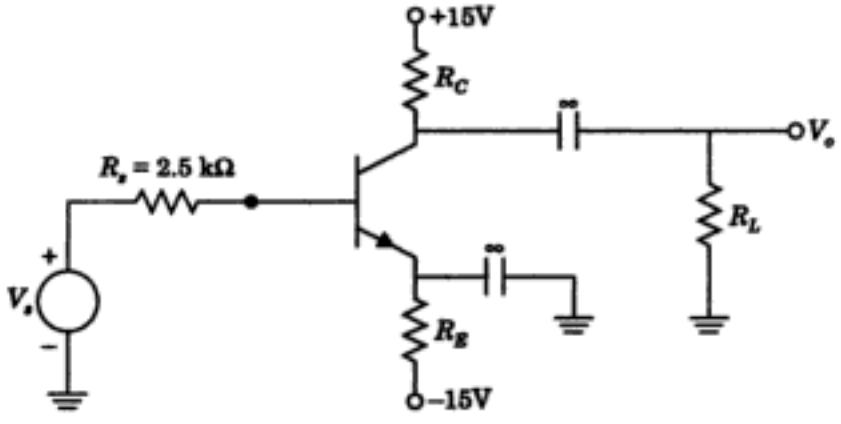


Fig. 6.61 Circuit for P6.18.

P6.19 In the circuit of Fig. 6.62, find R_{in} and gain $A_{V_s} = V_o/V_s$. Assume $\beta = 50$.

(***Ans.*** 1.75 kΩ, –11)

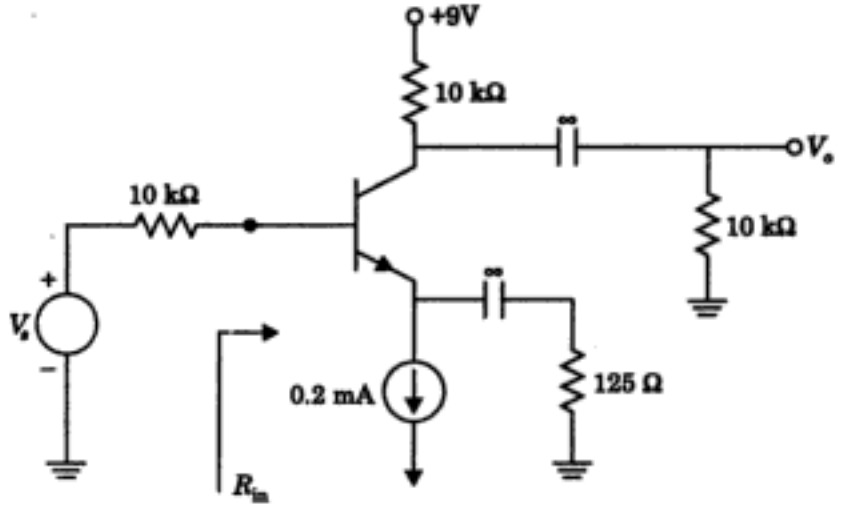


Fig. 6.62 Circuit for P6.19.

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P6.20 For the circuit shown in Fig. 6.63, find the input resistance R_i and the voltage gain V_o/V_s.

(***Ans.*** $R_i = 50\ \Omega$, $V_o/V_s = 9.9$)

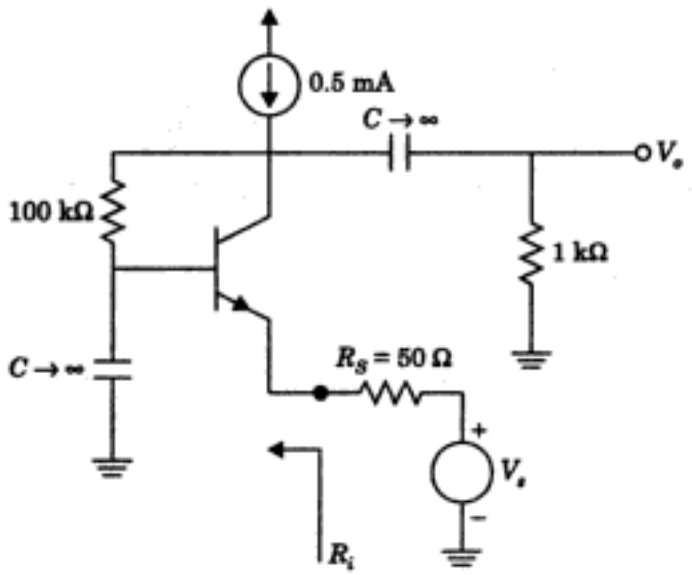


Fig. 6.63 Circuit for P6.20.

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CHAPTER 7

Field-Effect Transistors–Characteristics and Biasing

7.1 INTRODUCTION

The field-effect transistor (FET) is a three-terminal device with several features better than a BJT. The BJTs discussed in Chapters 4, 5 and 6 have mainly two drawbacks: (i) low input impedance (ii) high noise level. Both these drawbacks have been overcome in FETs. There are two types of FETs—Junction field-effect transistor (JFET or simply FET) and metal-oxide semiconductor field-effect transistor (MOSFET). Just as we have pnp and npn transistors, FETs can also be n-channel FET or p-channel FET. MOSFETs can further be of depletion or enhancement types as we shall see later.

The term 'field-effect' describes the physical operation taking place within the device. It will be shown that the current in an FET is controlled due to the electrical field established by the voltage applied to a control terminal. Further, current in an FET is due to only one type of carriers (electrons in an n-channel and holes in a p-channel) and, therefore, FET is also known as **unipolar transistor.**

The basic concept of FET has been known since 1930's, however, the device was used only in 1960's. Since 1970's, MOSFETs have become very popular as these devices have input impedance higher than JFET, can be made very small and are easy to fabricate. The various digital logics and memories used in digital computers can be implemented with circuits that use only MOSFETs, and no resistors or diodes are needed.

In this chapter, we will discuss the structure, physical operation and characteristics for JFET and MOSFET. Structure of complimentary MOS (CMOS) devices and MESFET (GaAs devices) are described. Then the biasing techniques for JFET and MOSFET are discussed.

7.2 STRUCTURE AND PHYSICAL OPERATION OF JFET

7.2.1 Structure of JFFT

The basic structure of an n-channel JFET is shown in Fig. 7.1(a). It consists of an n-type silicon bar called **channel** with two p^+ regions called **gates** diffused on the opposite sides.

The two p^+ regions are internally connected and an ohmic contact is brought out called **gate terminal.** Two ohmic contacts are also taken from the two ends of the Si bar (that is, channel) and are called **source** and **drain.** It can be seen that if a voltage supply is connected between source and drain terminals such that the positive end of the supply is connected to the drain terminal, the majority carrier electrons in the n-channel bar will flow from source to drain terminal.

The circuit symbol of n-channel JFET is shown in Fig. 7.1(b). In this the vertical line denotes the channel and the arrowhead on the gate line indicates the direction of flow of current in a pn junction. Thus, gate is p-type and channel is of n-type in this circuit symbol.

The structure and circuit symbol for p-channel JFET drawn on the same lines are shown in Fig. 7.2(a) and (b).

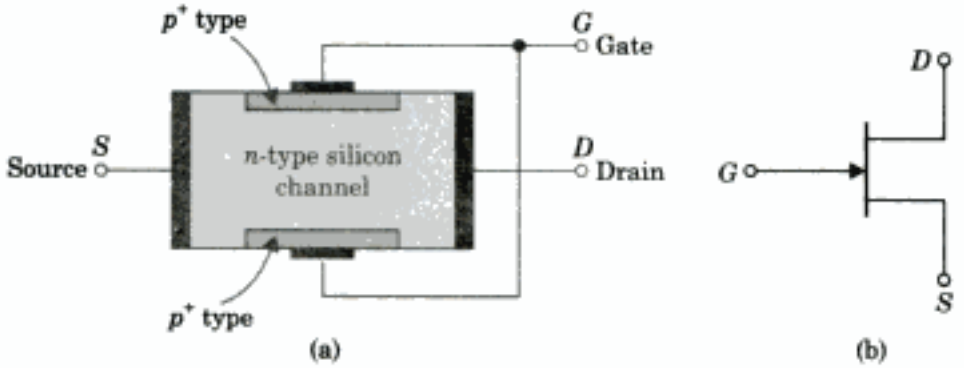


Fig. 7.1 An n-channel JFET (a) structure (b) symbolic representation.

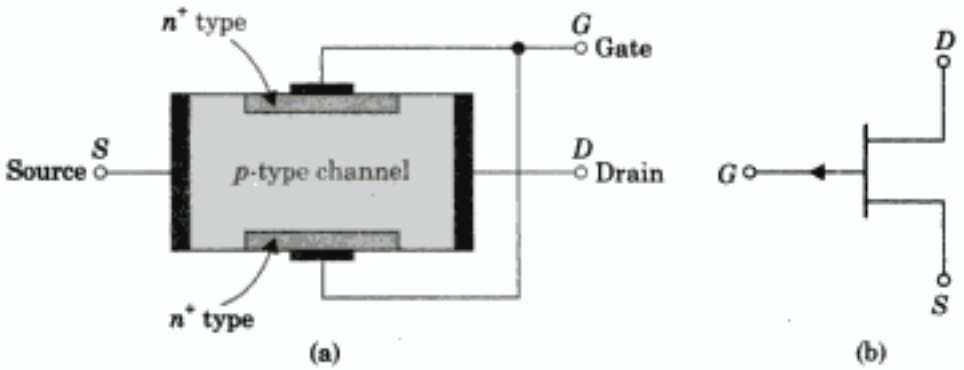


Fig. 7.2 p-channel JFET (a) structure (b) symbol.

The structure of the n-channel and p-channel JFET as shown in Figs. (7.1) and (7.2) are only for the sake of explaining the physical operation of the device. The actual fabrication of FET is done by using the planar IC technology. The cross section of an n-channel JFET using this technology is shown in Fig. 7.3.

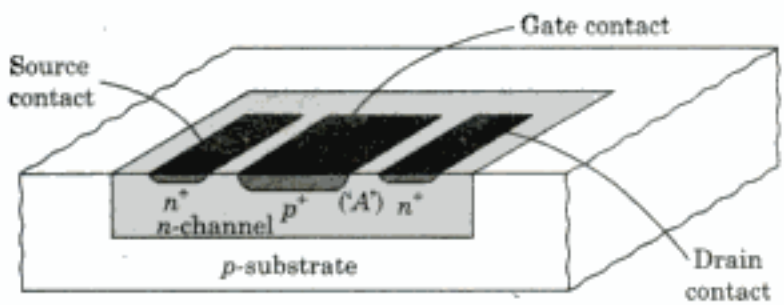


Fig. 7.3 Planar IC n-channel JFET structure.

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7.2.2 Physical Operation of JFET

For understanding the operation of JFET, consider an *n*-channel FET, shown in Fig. 7.4, where p^+ gates are connected to a negative supply V_{GG} and no voltage is applied between the source and drain terminals. It can be seen that p^+ gate regions and the *n*-channel form two *pn*-junctions which are reverse biased. This produces space charge region or depletion region on both sides of the reverse biased *pn*-junctions. However, the penetration of the depletion region in the p^+ gates will be small as compared to its penetration inside the *n*-channel. For this reason, the depletion region inside the p^+ gates have not been shown in Fig. 7.4. If the reverse biased voltage V_{GG} is increased, the depletion region will extend further into the *n*-channel. This in turn will decrease the effective width of the channel.

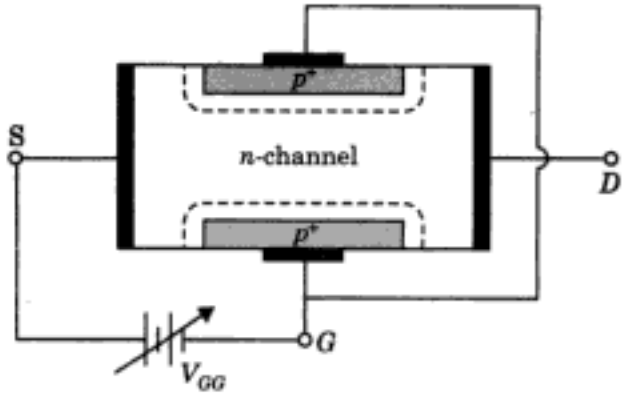


Fig. 7.4 Operation of JFET with gate reverse biased.

If we continue to increase the reverse bias voltage V_{GG}, the channel width will eventually reduce to zero as all the free carriers would have been removed from the channel. The voltage V_{GG} at which the effective channel width get reduced to zero is called the **pinch-off voltage V_p**. A JFET is usually operated with gate reverse-biased so that the gate current $I_G = 0$. This is a very important characteristic of an FET as it provides high input impedance for FET.

Now, consider Fig. 7.5(a) where gate is reverse biased by a constant voltage V_{GG} and a positive voltage V_{DD} is also applied between drain and source and is increased. As drain is at a positive potential w.r.t. source, the electrons which are majority carriers in the *n*-channel start moving from source to drain and therefore, constitute a drain current, I_o flowing from drain to source terminal. Due to this drain current, there will be a uniform voltage drop across the channel as the channel simply acts as a semiconductor bar. For example, if $V_{DD} = 2$ V, then there will be a continuous voltage drop from source end to drain end as shown in Fig. 7.5(b). This voltage will further reverse biases the *pn*-junction. It can

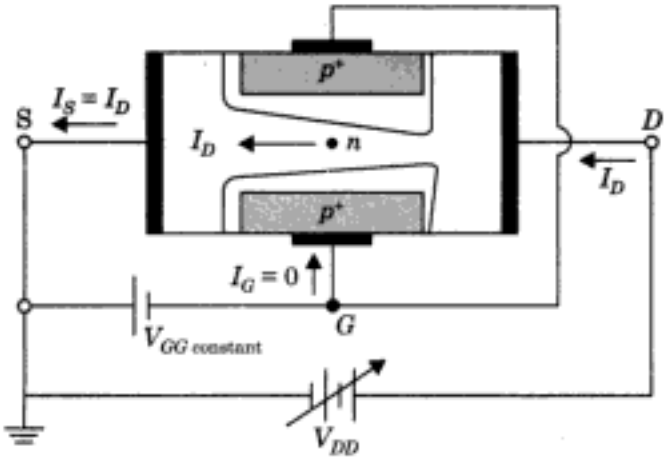


Fig. 7.5(a) Operation of JFET with V_{GG} and V_{DD} applied.

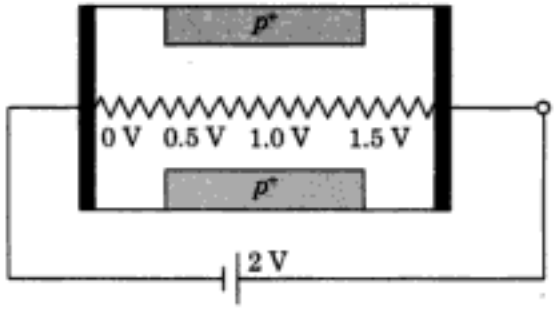


Fig. 7.5(b) Showing voltage drop across the channel due to V_{DD}.

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be seen that the region at the source end will be less reverse biased and as we more towards the drain, *pn*-region will be more reverse biased. Due to this non-uniform reverse biasing, penetration of the depletion region is also non-uniform as shown in Fig. 7.5(a) by the wedge shaped depletion region. If the drain supply voltage V_{DD} is further increased, a situation will arrive when the depletion region at the drain end will almost close the channel or the channel is pinched off at the drain end to the extent that the free carriers cannot cross it.

With the above explanation in mind, we can now describe the volt-ampere characteristics of an FET.

7.3 VOLT-AMPERE CHARACTERISTICS OF A JFET

There are two important characteristics of a JFET

(i) Output or drain characteristics

(ii) Transfer characteristics

7.3.1 Drain Characteristics

Figure 7.6(a) shows an *n*-channel FET in which supply connections correspond to common source configuration (CS) and its drain characteristics are shown in Fig. 7.6(b). The four distinct regions of operation marked on the characteristics are: (i) ohmic region, (ii) saturation or pinch-off region, (iii) breakdown region and (iv) cut-off region. The working of FET in these regions is now examined in detail.

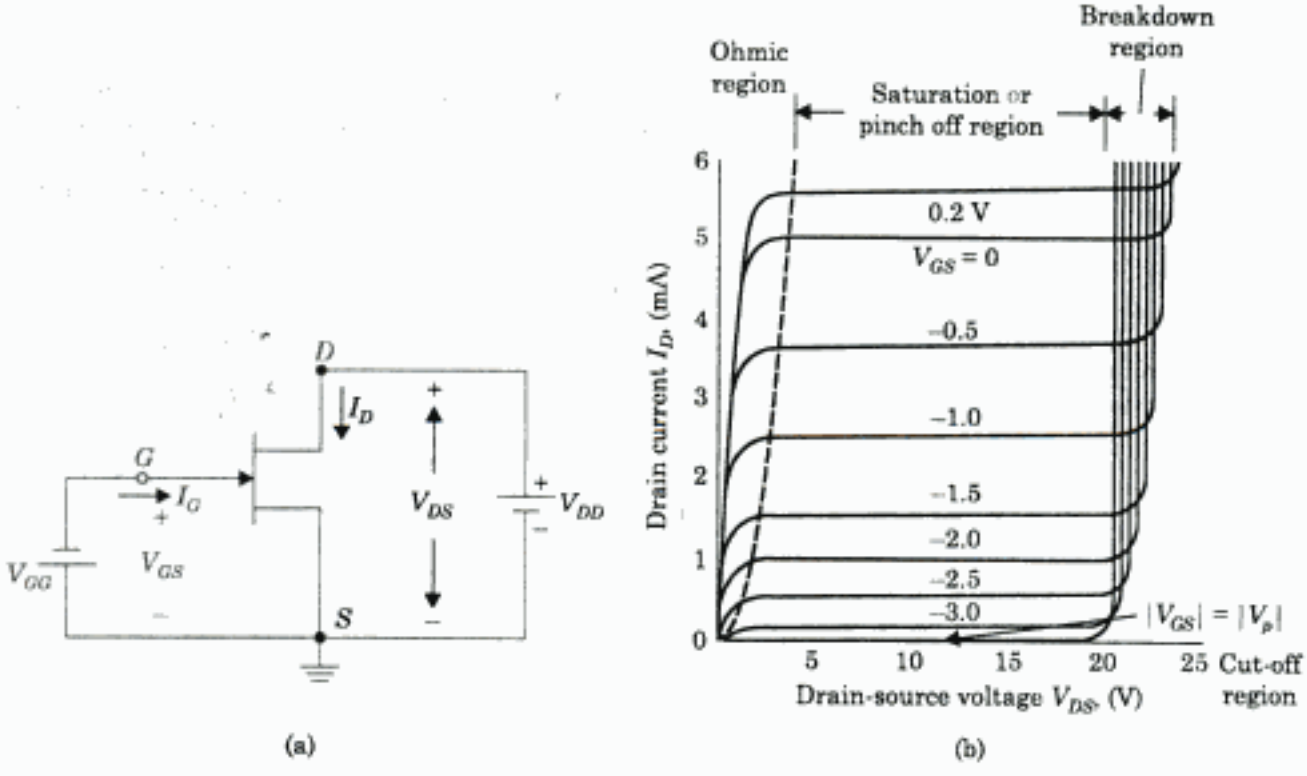


Fig. 7.6 (a) An n-channel JFET biased for CS configuration, (b) Drain characteristics.

Ohmic region: It can be seen from Fig. 7.6(b) that the characteristics are linear in the ohmic region. Consider the curve for $V_{GS} = 0$ V. We are considering this curve first as JFET is operated only for $V_{GS} \leq 0$ V, that is, for negative values of V_{GS}. If $V_{DS} = 0$, no current flows in the channel and $I_D = 0$. For small values of V_{DS} (~ 0.1 to 0.2 V), n-type silicon bar acts as a simple semiconductor resistor and current increases linearly with V_{DS}, following the ohm's law. For negative values of V_{GS} (reverse-biased gate), i.e. for $V_{GS} = -0.5$ V, -1.0 V, -1.5 V and so on the channel width goes on decreasing as V_{GS} is made more and more negative. This in turn increases the resistance of the channel and current I_D reduces.

The value of drain current I_D in the ohmic region is obtained from the cross-sectional view of JFET as shown in Fig. 7.7. In this figure, $2a$ is the maximum channel width for $V_{GS} = 0$ and decreases as V_{GS} is made more and more negative.

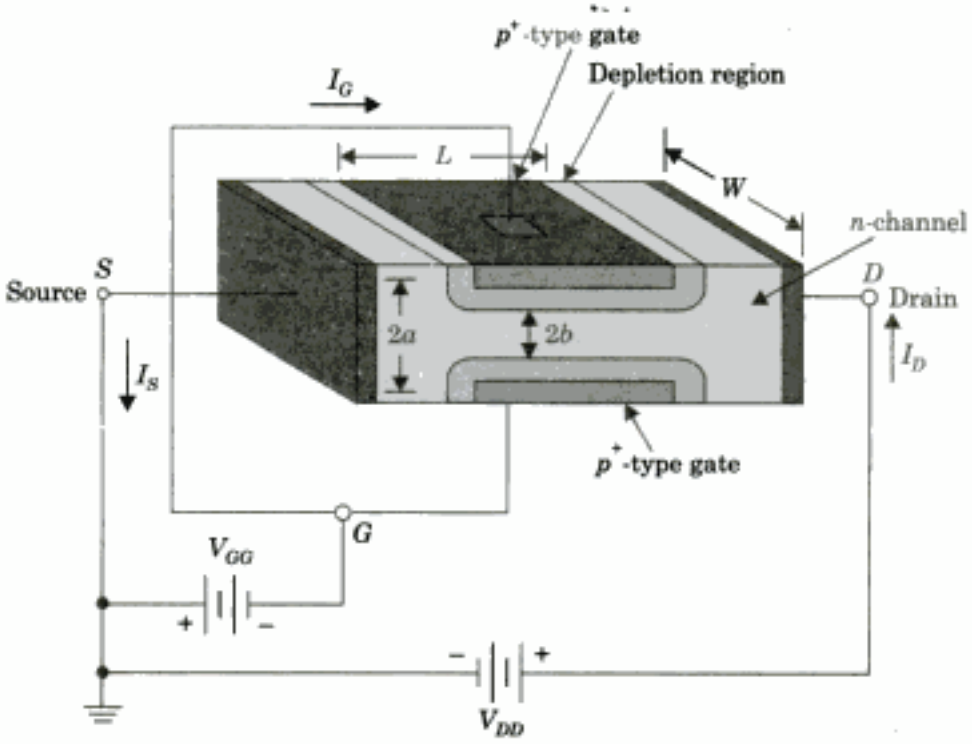


Fig. 7.7 Cross-sectional view of n-channel JFET.

For V_{DS} very small, the depletion region can be taken as uniform, so that the channel cross-sectional area A will be constant throughout its length. Hence $A = 2bW$, where $2b$ is the channel width corresponding to zero drain current for a specified V_{GS} and W is the channel dimension perpendicular to b-direction.

Using ohm's law, the drain current is given by

$$I_D = AqN_D\mu_n\varepsilon \tag{7.1}$$

$$= 2bWqN_D\mu_n \frac{V_{DS}}{L} \tag{7.2}$$

$$= 2bqN_D\mu_n \left(\frac{W}{L}\right) V_{DS} \tag{7.3}$$

where A = Cross-sectional area of the channel (= $2bW$)
$2b$ = Channel width for a specified V_{GS}
W = Channel dimension perpendicular to the b-direction

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N_D = Number of donor atoms in the n-bar
μ_n = Mobility of electrons
L = Length of the channel

Equation (7.3) shows that for small values of V_{DS}, FET behaves like an ohmic resistance whose value is determined by V_{GS} as it controls the channel width b. The slope of the I_D versus V_{DS} characteristics at the origin for a given V_{GS} is called the *on drain resistance*, $r_{D(ON)}$. For $V_{GS} = 0$, $b = a$ in Fig.7.7, therefore

$$r_{D(ON)} = \frac{1}{2aqN_D\mu_n}\left(\frac{L}{W}\right) \tag{7.4}$$

The parameter $r_{D(ON)}$ is important for switching applications as it is a measure of how much FET deviates from ideal switch.

The ratio W/L is also an important quantity in the design of FETs. For a given doping density N_D, it is possible to fabricate FETs on the same chip with different current handling capabilities simply by using different W/L ratios.

Saturation region: Consider the curve for $V_{GS} = 0$. As V_{DS} is increased beyond the ohmic region, the current I_D produces a uniform voltage drop across the channel as explained in Fig. 7.5(b). Due to non-uniform reverse biasing, depletion region penetration is also non-uniform as shown in Fig. 7.5(a). As the channel has got constricted, the current I_D no longer increases linearly and the V-I characteristics become curved.

As V_{DS} is further increased, a value of voltage V_{DS} is reached when the channel is "pinched-off" towards the drain end. The current I_D now saturates or simply levels off. The value of V_{DS} at which the channel is pinched off is called the pinch-off voltage V_P. The pinch-off voltage cannot be defined exactly on the characteristics. The region of the characteristics where the drain current I_D becomes fairly constant is called pinch-off or saturation region. The region to the left of saturation region is called ohmic or non-saturation region. One question that comes in mind is that why does the current I_D not become zero when channel is pinched-off at the drain end. It is infact practically not possible for the current I_D to become zero, as the very reverse bias which has caused this 'pinch-off' will not be available. The channel infact does not close completely at the drain end ever.

For the negative gate source voltage V_{GS}, pn-junction is more reverse biased and the penetration of depletion region is more into the channel resulting in reduced channel width. The pinch-off now occurs at a smaller value of V_{DS} and the saturation current I_D also reduces. Thus as V_{GS} is made more and more negative, the V-I curves shift downwards.

If, however, V_{GS} is made positive so as to forward-bias the pn-junction as shown by the curve for $V_{GS} = +0.2$ V, the current I_D increases. The gate current I_G will be however, very small as this voltage is less than the cut-in voltage V_r (= 0.5 V for Si). A JFET is never operated with V_{GS} as positive, as for higher values of V_{GS}, the gate current will increase and reduce the effective amplifier operation.

The saturation drain current for $V_{GS} = 0$ V is designated as I_{DSS} and is a useful parameter. It is usually specified in the manufacturer's data sheet and is useful in finding the transconductance of an FET.

Breakdown region: If we go on increasing V_{DS}, a value is reached at which the pn-junction between the drain region and substrate suffers avalanche breakdown. This breakdown usually occurs at 50 V to 100 V and results in a rapid increase of current.

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It can be seen that the breakdown occurs at a lower value of V_{DS} as the gate is more and more reverse biased. This is due to the fact that reverse bias gate voltage gets added to the drain voltage, thereby increasing the effective voltage across the *pn*-junction. The breakdown voltage between drain and source with the gate short circuited to the source is designated as BV_{DSS} in the manufacture data sheets.

Cut-off region: As V_{GS} is made more and more negative to reverse bias the gate, the width of the conducting channel goes on decreasing. For $|V_{GS}| = |V_p|$, the channel width is reduced to zero and saturation current $I_{DS} = 0$. In a practical situation, leakage current $I_{D,OFF}$ flows even under the cut-off condition $|V_{GS}| > |V_p|$, and is of the order of about 1 pA in IC devices.

In the cut-off state, a small current in the range of pA also flows from gate to source. This current is called **gate reverse current** or **gate cut-off current** and is designated by I_{GSS}.

7.3.2 Transfer Characteristics

The transfer characteristics of an FET is drawn between the output drain current I_D and input gate source voltage V_{GS} for a fixed V_{DS}. These characteristics can be easily obtained from the output characteristics of an FET as shown in Fig. 7.8.

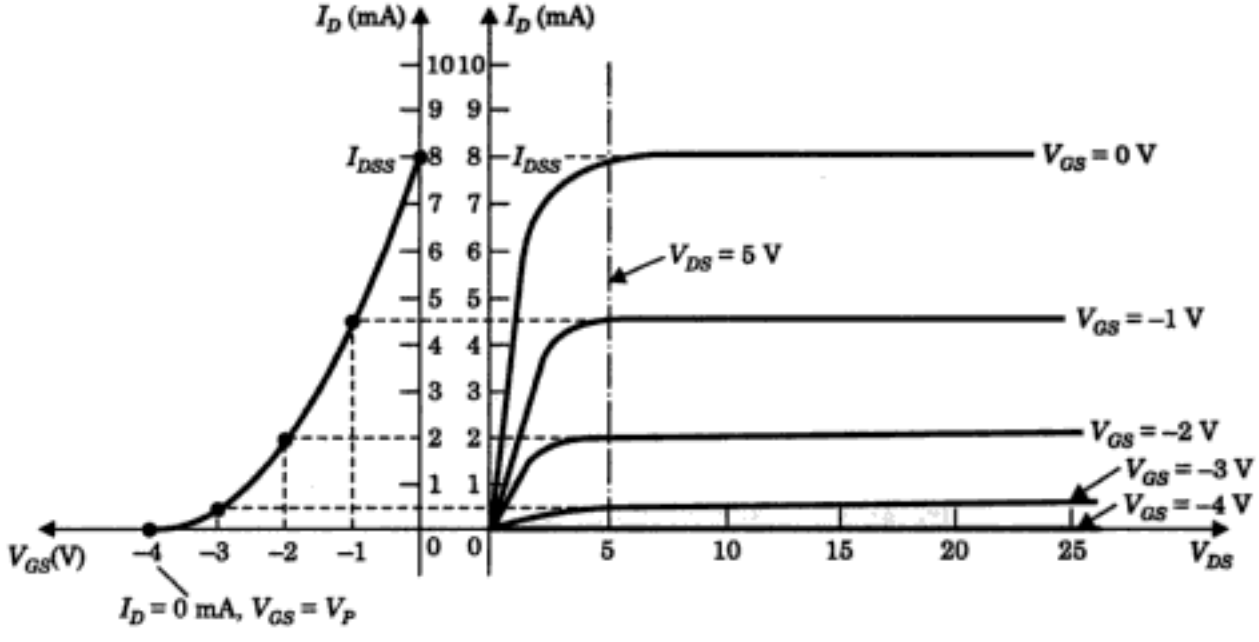


Fig. 7.8 Obtaining transfer characteristics from output/drain characteristics of a JFET.

For V_{DS} = 5 V, say, the values of I_D for V_{GS} varying from 0 V to $V_{GS} = V_p$ (in this case –4 V) are plotted on I_D vs V_{GS} graph on the left. It can be seen that a parabolic curve results because the vertical spacing in the output characteristics is not constant for the same change in V_{GS}. As V_{GS} becomes more and more negative, the spacing in the output characteristics goes on decreasing.

The transfer characteristics can also be expressed analytically by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \tag{7.5}$$

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There is no mathematical derivation of this equation, however it fits best in the parabolic shape of the transfer curve. This equation is valid for both *p*-channel and *n*-channel JFETs as V_{GS} and V_p both are either positive (for *p*-channel) and negative (for *n*-channel).

For dc analysis of FET amplifiers, that is, for finding the Q-point, a graphical approach is found to be more convenient compared to mathematical. The graphical approach requires equation (7.5) representing transfer curve to be plotted for finding the Q-point. Since transfer curve has to be plotted invariably for the dc analysis of FET, we discuss a simple way to plot these characteristics.

For $V_{GS} = V_p/2$, the resulting I_D is found from the Shockley's equation as:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \tag{7.6}$$

$$= I_{DSS}\left(1 - \frac{V_p/2}{V_p}\right)^2$$

$$= I_{DSS}\,(0.25) \tag{7.7}$$

Thus,
$$I_D = \frac{I_{DSS}}{4}\bigg|_{V_{GS}=V_p/2} \tag{7.8}$$

If we choose, $I_D = I_{DSS}/2$ and substitute into Eq. (7.5) we find that

$$V_{GS} = V_p\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \tag{7.9}$$

$$= V_p\left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right)$$

$$= V_p(1 - \sqrt{0.5})$$

$$= V_p(0.293) \tag{7.10}$$

or
$$V_{GS} \cong 0.3V_p\big|_{I_D=I_{DSS}/2} \tag{7.11}$$

The transfer curve now can be plotted to a satisfactory level of accuracy using the four points shown in Table 7.1.

Table 7.1 Points for Plotting Transfer Curve of a JFET

V_{GS}	I_D
0	I_{DSS}
$0.3V_p$	$I_{DSS}/2$
$0.5V_p$	$I_{DSS}/4$
V_p	0 mA

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EXAMPLE 7.1

Plot the transfer curve of an FET if I_{DSS} = 12 mA and V_p = –5V.

Solution: Two end points of the transfer curve are defined by

I_{DSS} = 12 mA for V_{GS} = 0 V

I_D = 0 mA for $V_{GS} = V_p$ = –5 V

Also, for $V_{GS} = 0.3V_p$

$= 0.3(-5)$

$= -1.5$ V

$I_D = I_{DSS}/2 = 6$ mA

and for $V_{GS} = 0.5V_p$

$= 0.5(-5$ V$)$

$= -2.5$ V

$I_D = I_{DSS}/4$

$= 3$ mA

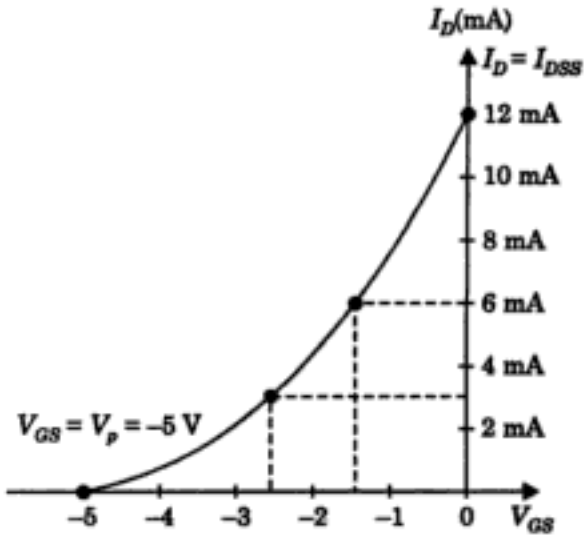


Fig. 7.9 Transfer curve for Example 7.1.

The transfer curve using these four points are shown in Fig. 7.9.

7.4 COMPARISON OF FET WITH BJT

The junction field-effect transistor or JFET came as an improvement over BJT and has many features which are an advantage over BJTs. Here are listed some of the important differences in FETs and BJTs:

(i) An FET is essentially a unipolar device as the current is conducted by only one type of carriers (electrons for *n*-channel and holes for *p*-channel FET). The BJT on the other hand is a bipolar device as conduction of current is due to both holes and electrons.

(ii) An FET is characterized by high input impedance, usually of the order of several hundred mega ohms, whereas for BJT it is of the order of few kilo ohms. This feature makes FET more suitable as a voltage amplifier compared to BJT.

(iii) FETs are more temperature stable compared to BJTs.

(iv) FETs are simple to fabricate and occupies less area on the silicon chip.

(v) It is less noisy than BJT.

(vi) FET is a voltage controlled device whereas BJT is a current controlled device.

(vii) It has zero off-set voltage at zero drain current unlike the cut-in voltage (V_γ) for a BJT and hence makes an excellent signal chopper.

7.5 METAL-OXIDE SEMICONDUCTOR FET (MOSFET)

As a further improvement over JFET, the metal-oxide semiconductor field-effect transistor (MOSFET) got introduced in 1970's. MOSFETs have input impedance even higher than

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JFET, can be made very small and their fabrication is relatively simple. So much so, that MOSFETs have made JFETs virtually obsolete. The use of JFETs is limited to applications using discrete components both as an amplifier and as a switch. In IC applications, it is used in the design of the differential input stage of some operational amplifiers. However, most of the VLSI circuits at present are made using MOS technology. Examples include microprocessors and memory chips. MOS technology is being extensively used in the design of analog integrated circuits and in ICs that combine both analog and digital circuits. There are two types of MOSFETs: (i) Enhancement MOSFET, (ii) Depletion MOSFET. We shall study the structure, physical operation and volt-ampere characteristics of both types of MOSFETs.

7.5.1 Structure and Physical Operation of Enhancement-MOSFET

The enhancement type of MOSFET is the most widely used field-effect transistor. Figure 7.10(a) and (b) shows the detailed physical structure and cross-sectional view, respectively of the *n*-channel enhancement-type MOSFET. The transistor is fabricated on a *p*-type

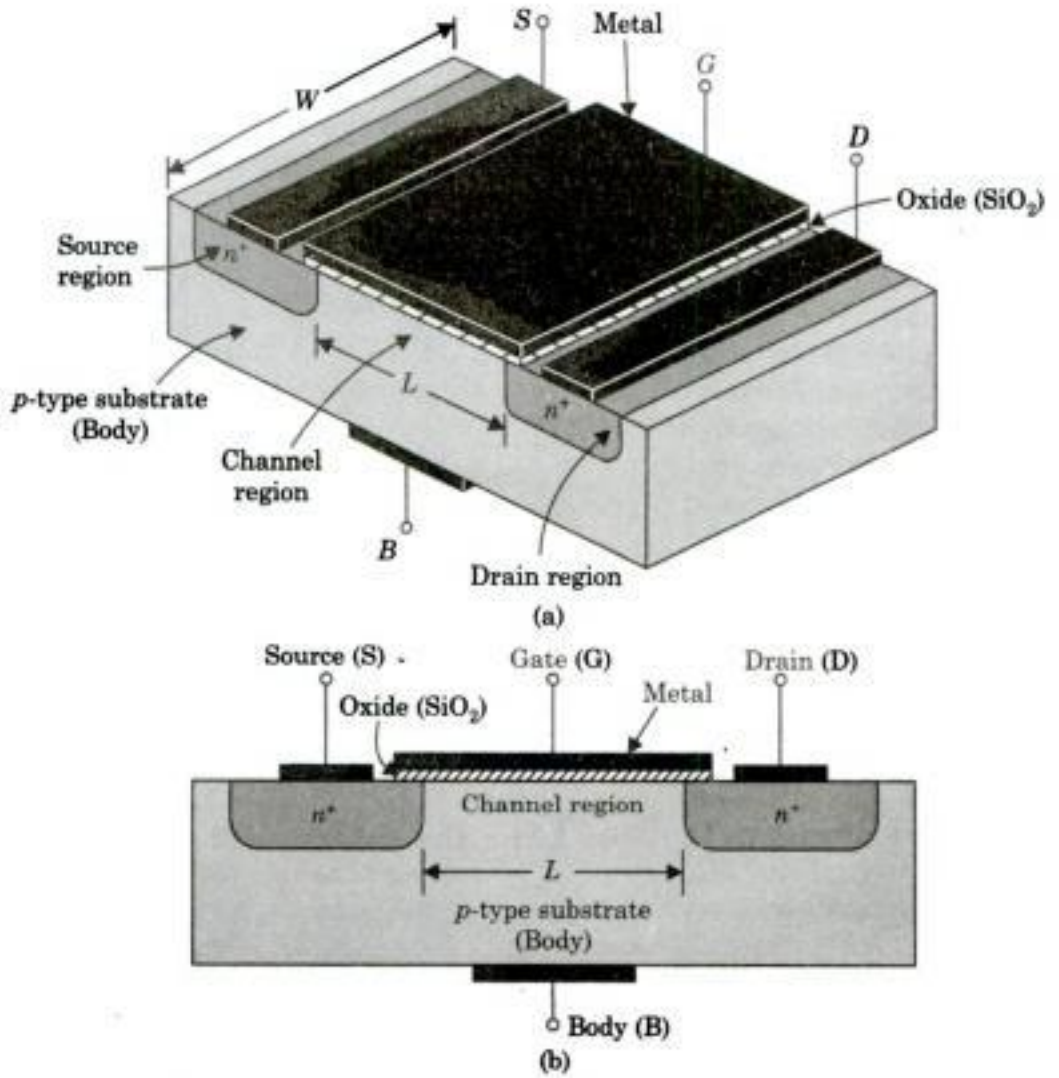


Fig. 7.10 Physical structure of the enhancement-type NMOS transistor (a) Detailed view; (b) Cross-section. [Typically L = 1 to 10 μm, W = 2 to 500 μm]

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substrate which provides physical support for the device. Two heavily doped n-type regions indicated in the figure as the n^+ source and n^+ drain are diffused into the substrate. A very thin (0.02 to 0.1 μm) layer of silicon dioxide (SiO_2) which is an excellent electrical insulator is grown on the surface of substrate covering the area between the source and drain regions. Metal (Aluminium) is deposited on top of SiO_2 layer to form the gate electrode of the device. Metal contacts are also taken out from the source region (S), drain region (D), and the substrate also known as the **body.** It can be seen that the name metal-oxide semiconductor FET is derived from the physical structure only.

Nowadays, MOSFETs are fabricated using silicon-gate technology in which a polysilicon layer is used to form the gate electrode. This, however, does not change the operation of the MOSFET.

MOSFET is also commonly known as **insulated gate FET** or **IGFET** for the simple reason as the gate electrode is electrically insulated from the substrate or device body by the oxide layer. It is because of this insulating layer (silicon oxide or polysilicon) that the gate current is extremely small (of the order of 10^{-15} A) and input impedance is high (10^{10} to 10^{15} Ω).

If no voltage is applied to the gate terminal (i.e. $V_{GS} = 0$), it can be seen that there are two back to back diodes in series between drain and source regions. One diode is formed between n^+ drain region and the p-type substrate and the other diode is formed between p-type substrate and the n^+ source region. Now, even if a voltage V_{DS} is applied, current can not flow through these back-to-back diodes.

Now consider the case when source and drain both are grounded as shown in Fig. 7.11 and a positive voltage V_{GS} is applied to the gate. This positive voltage establishes an electric field which induces negative charges in the p-substrate just below the SiO_2 layer. The 'induced n' region inside the p-substrate forms a channel for current flow from drain to source. The gate and substrate infact forms a parallel plate capacitor with oxide layer acting as a dielectric. The positive gate voltage causes positive charge to accumulate on the gate electrode. This in turn induces negative charge on the bottom plate, i.e., p-substrate thereby producing an induced channel.

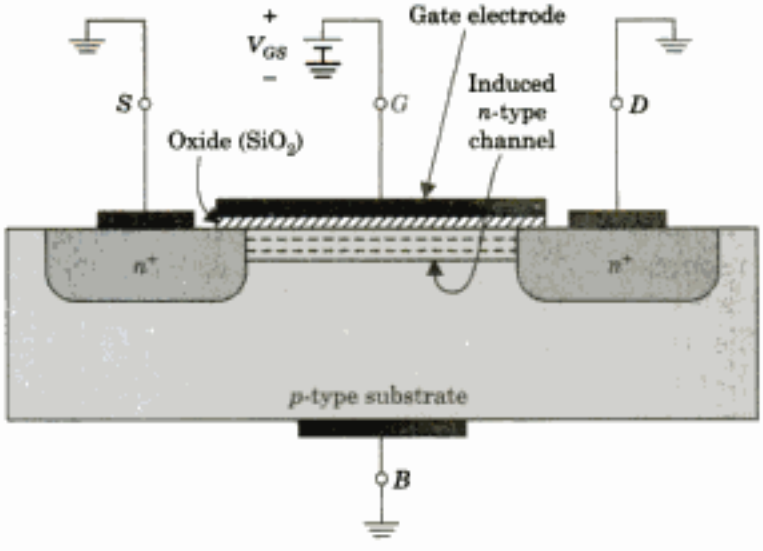


Fig. 7.11 The enhancement-type NMOS showing induced channel for $V_{GS} > 0$ and $V_{DS} = 0$.

It is because of this n-type induced channel that the structure shown in Fig. 7.11 is called ***n*-channel MOSFET** or simply **NMOS transistor.** The induced channel is also called **inversion layer** as the induced electrons change p-type substrate into n-type.

There is a value of gate voltage V_{GS} at which sufficient number of mobile electrons get induced into the p-type substrate to form a conducting channel. This voltage is called **threshold voltage** and is designated as V_T. Obviously, the value of V_T for an n-channel

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FET is positive. The value of V_T can be controlled by various fabrication techniques and typically lies in the range of 1 to 3 V.

Once a channel is formed, if now a positive voltage V_{DS} is applied between drain and source as shown in Fig. 7.12, it can be seen that a current I_D flows through the induced channel. Current is carried by the free electrons travelling from source to drain. Conventionally, the direction of current is positive opposite to the direction of flow of negative charge, hence the current I_D is positive from drain to source as indicated in Fig. 7.12. The magnitude of I_D depends upon the density of the electrons in the channel which in turn depends upon the magnitude of gate voltage V_{GS}. For $V_{GS} = V_T$, the threshold voltage, channel is just induced and current is negligibly small. As V_{GS} is increased above V_T, the channel depth increases. This increases the number of electrons and hence I_D increases. Thus, increasing V_{GS} above V_T enhances the channel and hence the name enhancement-mode operation or enhancement type MOSFET.

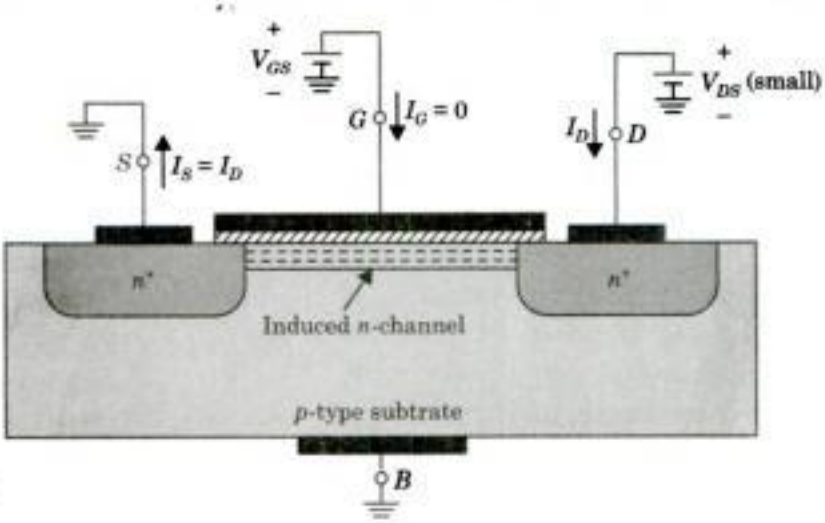


Fig. 7.12 An NMOS transistor with $V_{GS} > V_T$ and small V_{DS}.

For small values of V_{DS} (in the range 0.1 to 0.2 V), the device operates as a linear resistor whose value is controlled by V_{GS}. The relationship between I_D and V_{DS} follows simple ohm's law.

As V_{DS} is increased further, the voltage V_{DS} appears as a voltage drop across the length of the channel. That is, as we move from source to drain, the voltage increases from 0 to V_{DS}. Because of this, the voltage between the gate and the points along the channel decreases from a value V_{GS} at the source end to $(V_{GS} - V_{DS})$ at the drain end. The channel depth, therefore, is no longer uniform and is tapered as shown in Fig. 7.13. The current I_D no longer increases linearly as we have seen in the case of FET. Eventually, as V_{DS} is further increased, the channel depth at the drain end becomes almost zero and channel is pinched-off. Now, even if V_{DS} is further increased, the shape of the channel does not change much and the current through the channel remains constant at the value reached for $V_{DS} = V_{GS} - V_T$. The drain current has thus saturated and MOSFET is said to have entered

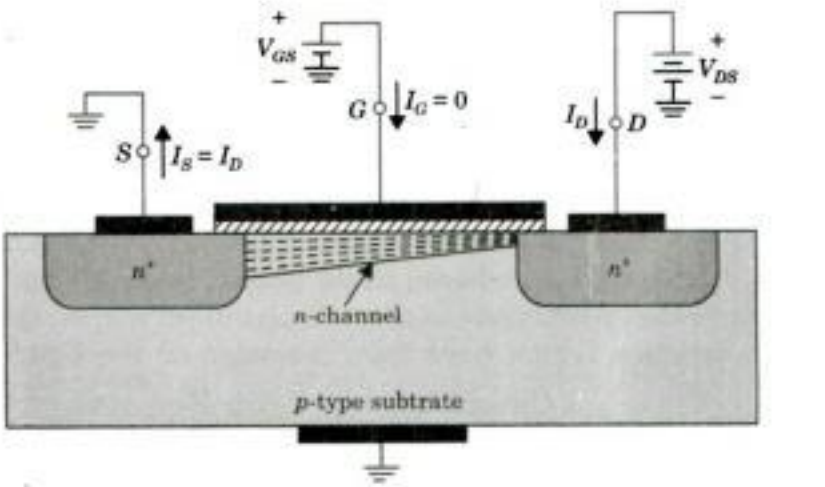


Fig. 7.13 NMOS transistor showing tapered induced channel for V_{DS} increased.

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The transfer curve is now given by the relation:

$$I_D = 0.25 \times 10^{-3} (V_{GS} - 1)^2 \quad (7.17)$$

Two points are already available on the transfer curve as:

$$V_{GS} = 1 \text{ V}, I_D = 0$$

and

$$V_{GS} = 5 \text{ V}, I_D = 4 \text{ mA}$$

For $V_{GS} = 4$ V, the value of I_D is found from Eq. (7.17) as

$$I_D = 0.25 \times 10^{-3} (4 - 1)^2$$
$$= 0.25 \times 10^{-3} \times 9$$
$$= 2.25 \text{ mA}$$

One may find I_D for one more value of V_{GS}, say at $V_{GS} = 3$ V to plot the transfer characteristics.

EXAMPLE 7.2

An enhancement type NMOS transistor with $V_T = 2$ V has source terminal grounded. If $V_{GS} = 3$ V, define the regions of operation for (a) $V_{DS} = +0.5$ V, (b) $V_{DS} = 1$ V, (c) $V_{DS} = 5$ V.

Solution: It is easily seen that the transistor is either in ohmic region or saturation region as $V_{GS} > V_T$.

(a) $$V_{GS} - V_T = 3 - 2$$
$$= 1 \text{ V}$$

Since $$V_{DS} < V_{GS} - V_T$$

Therefore, transistor is in ohmic region.

(b) $$V_{DS} = 1 \text{ V}$$

As $$V_{DS} = V_{GS} - V_T = 1 \text{ V},$$

the transistor is in saturation region.

(c) $$V_{DS} = 5 \text{ V}$$

therefore, $$V_{DS} > V_{GS} - V_T$$

the transistor is in saturation region.

7.5.3 *p*-channel Enhancement MOSFET

The structure of a *p*-channel enhancement MOSFET is shown in Fig. 7.17. It can be seen that it has two p^+-type regions in an *n*-type substrate. The physical operation of a *p*-channel MOSFET is same as that for NMOS device discussed earlier. The circuit symbol for *p*-enhancement-type MOSFET is shown in Fig. 7.18(a). If the substrate is connected to source internally, the simplified symbol of Fig. 7.18(b) is used. The voltage and current polarities are shown in Fig. 7.18(c) and can be seen to be opposite to that for NMOS.

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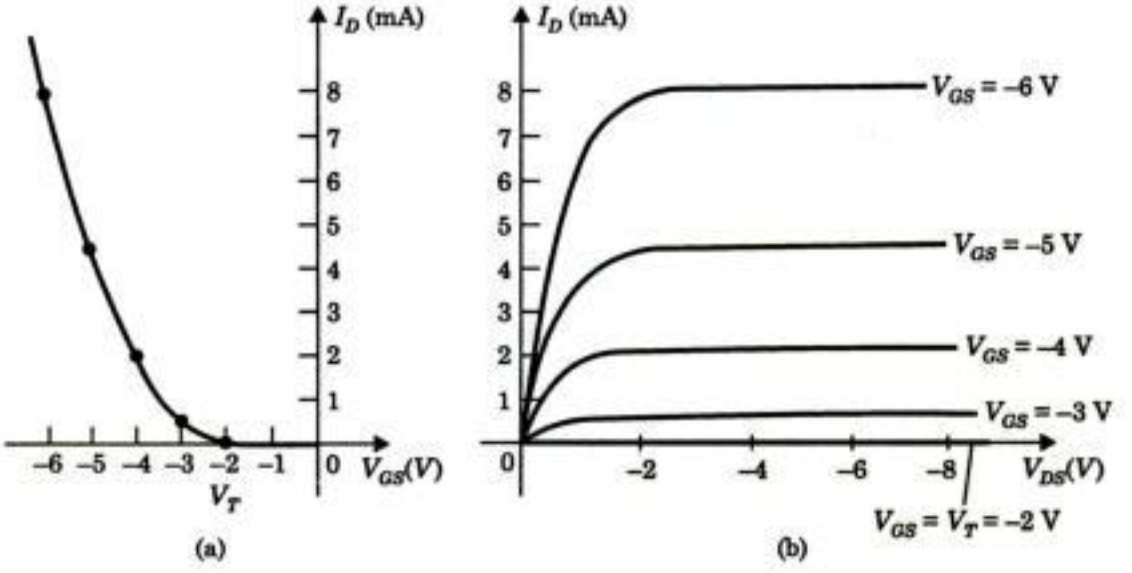


Fig. 7.19 *p*-channel enhancement-type MOSFET with $V_T = -2$ V.

7.6 THE DEPLETION-TYPE MOSFET

We now discuss a second type of MOSFET, the depletion-type of MOSFET. The structure of an *n*-channel depletion-type MOSFET is shown in Fig. 7.20. The main difference between depletion MOSFET from enhancement-type MOSFET is the presence of a narrow *n*-channel embedded into the substrate in the region between n^+ source and n^+ drain. Now, if a voltage V_{DS} is applied between drain and source, a current I_D flows even for $V_{GS} = 0$ due to the presence of free electrons in the channel. This means that there is no need to induce a channel to cause a current to flow as in the case of enhancement MOSFET.

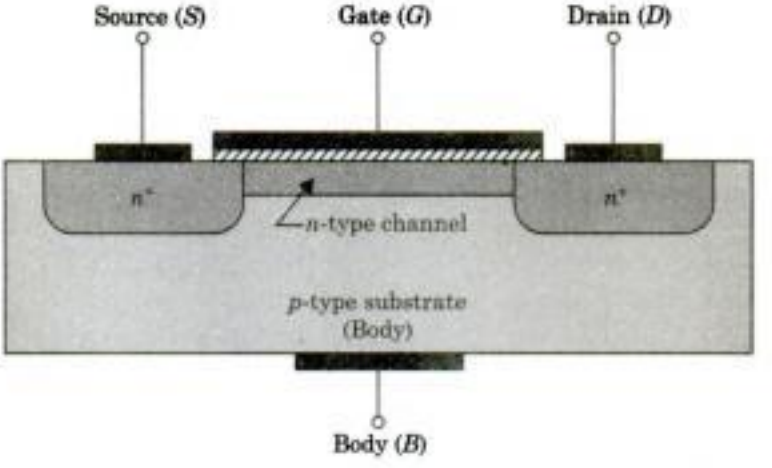


Fig. 7.20 Structure of an *n*-channel depletion-type MOSFET.

The channel depth and hence its conductivity is controlled by V_{GS}. A positive V_{GS} enhances the conductivity of the channel by inducing more free electrons to it. However, if we apply a negative V_{GS}, electrons are repelled from the channel decreasing its conductivity. The negative V_{GS} is said to deplete the channel of its charge carriers and this mode of

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operation is called **depletion mode.** If the gate voltage is made more negative, a value is reached at which the channel is completely depleted of charge carriers and current I_D is reduced to zero even though V_{DS} may still be applied. This negative value of V_{GS} is called the **threshold voltage** V_T of the n-channel depletion type MOSFET. It is easily seen that a depletion-type MOSFET can be operated in the enhancement mode by applying a positive V_{GS} and in the depletion mode by applying a negative V_{GS}.

The circuit symbol for the n-channel depletion-type MOSFET is shown in Fig. 7.21(a). The only difference between this from the symbol of enhancement-type device is that the vertical line representing the channel is solid, signifying that a physical channel exists. When substrate (or body) is connected to source, the simplified symbol shown in Fig. 7.21(b) is used where the shaded area indicates the embedded channel.

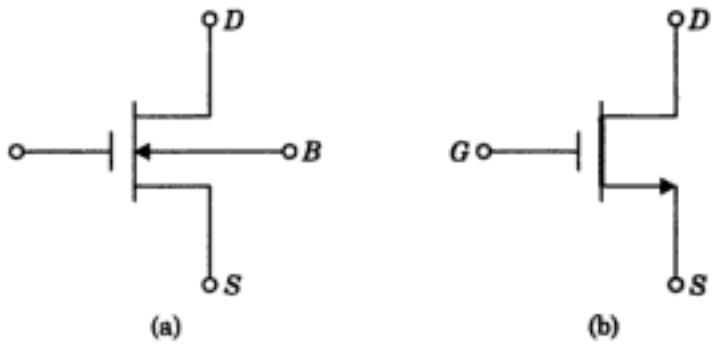


Fig. 7.21 (a) Circuit symbols for the n-channel depletion-type MOSFET. (b) Simplified circuit symbol when source (S) is connected to substrate (B).

Figure 7.22(a) shows a n-channel depletion-type MOSFET biased for common source (CS) configuration, for which the $V_{DS} - I_D$ characteristics are shown in Fig. 7.22(b). The various regions of operation: cut-off, ohmic and saturation regions have been shown on the curves. It may be noted that as the threshold voltages V_T is negative, the depletion NMOS operates in the ohmic region for $V_{DS} \leq V_{GS} - V_T$. In the saturation region, $V_{DS} \geq V_{GS} - V_T$.

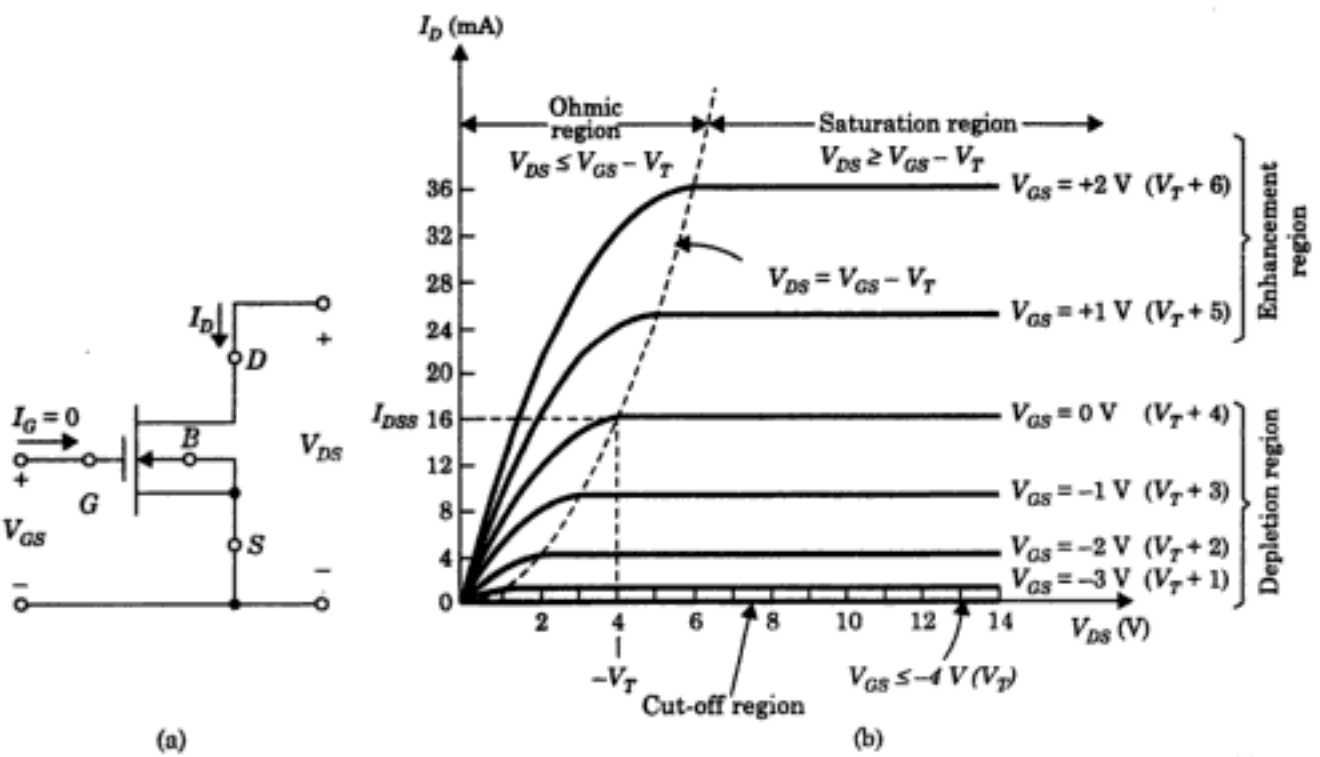


Fig. 7.22 (a) A depletion type n-channel MOSFET biased in common source (CS) configuration, (b) Drain characteristics.

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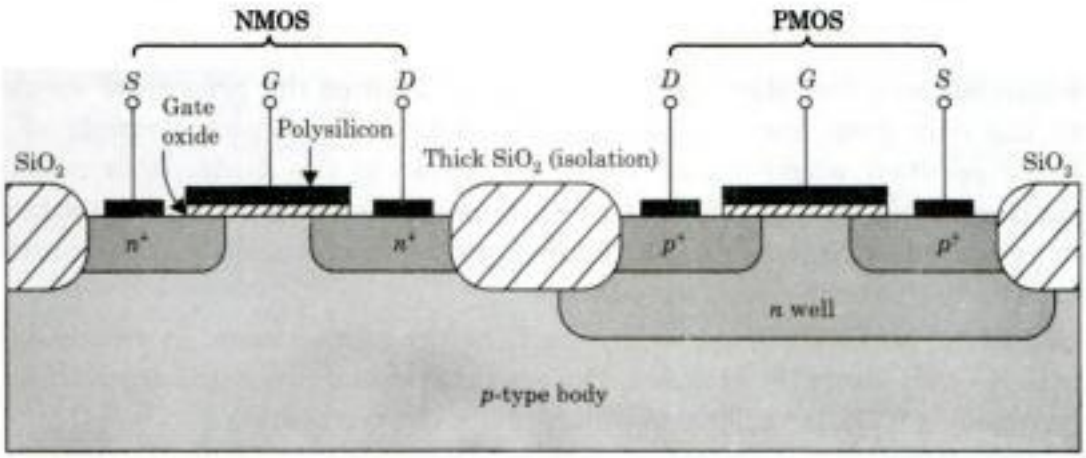


Fig. 7.24 A cross-sectional view of a CMOS.

One of the main advantages of CMOS devices is that it is possible to reduce the power dissipation to very low levels (< 50 nW) which is a very important criterion in all the VLSI circuits.

7.8 THE MESFET—GALLIUM ARSENIDE (GaAs) DEVICES

The various devices discussed in the text so far, that is, BJTs and FETs are made of silicon. There is however one more semiconductor material, gallium arsenide (GaAs) which has been found to be very useful in digital applications that require extremely high speed of operation and analog applications that require very high operating frequencies. Gallium Arsenide is a compound semiconductor formed of gallium from III-group and arsenic from the *V*-group; thus GaAs is also known as III-V semiconductor.

The GaAs technology is still in the early stages of development. The active device available in this technology is an *n*-channel FET known as **metal semiconductor FET** or **MESFET.** The technology also provides a diode known as **Schottky barrier diode (SBD).** Fig. 7.25 illustrates the structure of these two basic devices. The GaAs devices are fabricated

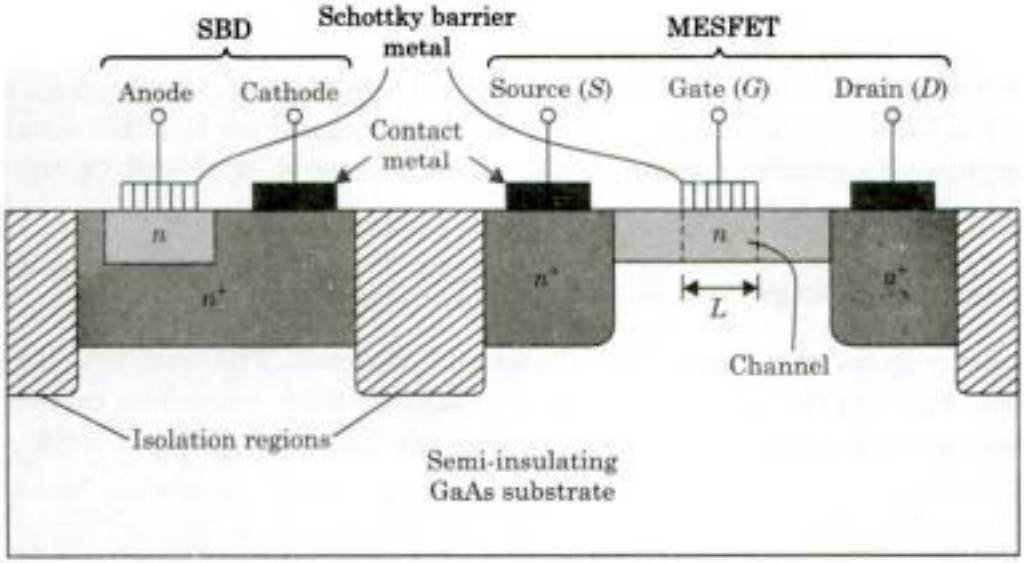


Fig. 7.25 Cross-section of a GaAs Schottky barrier diode (SBD) and a MESFET.

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on an undoped GaAs substrate for which the conductivity is very low. The substrate thus is semi-insulating and, therefore, this technology simplifies the process of insulating the devices on the chip from one another. The Schottky barrier diode consists of a metal-semiconductor junction where metal forms the anode of the diode. It is referred to as Schottky barrier metal as it is different from the metal used for making a contact. The n-type GaAs forms the cathode and the n^+ GaAs between the n-region and the cathode metal contact reduces the parasitic series resistance.

The gate of the MESFET is formed by the Schottky barrier metal in direct contact with the n-type GaAs that forms the channel. The source and drain contacts are also surrounded by heavily doped (n^+) GaAs regions to reduce parasitic resistances.

The MESFET operates in a very similar manner to JFET with the Schottky metal playing the role of the p-type gate of the JFET. The most common GaAs MESFETs available are of the depletion type with a threshold voltage V_T in the range of -0.5 to -2.5 V. Only n-channel MOSFETs are available in GaAs technology. This is because holes have relatively low drift mobility in GaAs and hence p-channel MOSFETs are less attractive.

The circuit symbol for the depletion type n-channel GaAs MESFET and Schottky-barrier diode are shown in Fig. 7.26(a) and (b) respectively.

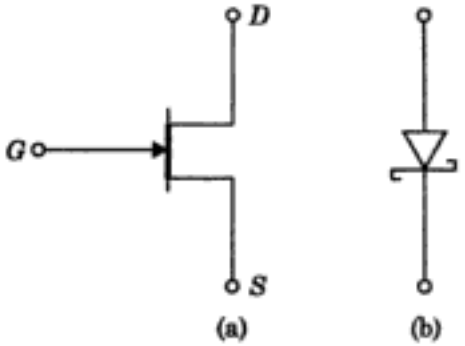


Fig. 7.26 Circuit symbols for (a) n-channel depletion type GaAs MESFET, (b) Schottky barrier diode (SBD).

7.9 BIASING IN JFET/MOSFET

It has been shown in Chapter 5 that it is essential to establish an appropriate dc operating point for the BJT when it is used as an amplifier. Similarly, for the design of an (FET/MOSFET amplifier, a biasing circuit is needed to establish an appropriate dc operating point. The dc analysis for FET is slightly complicated compared to BJT due to the nonlinear relationship between input and output quantities. The relationship between I_D and V_{GS} for both JFET/MOSFET contains a square term and thus complicates the mathematical analysis. The graphical approach is found to be more convenient, and will be shown for the various biasing schemes.

7.9.1 Biasing Arrangements for JFET

Fixed-bias arrangement: Figure 7.27 shows an n-channel JFET amplifier biased by a dc voltage source V_{GG} and the ac input signal v_i applied through a coupling capacitor C_1. The ac output voltage v_o is taken from the drain through the coupling capacitor C_2.

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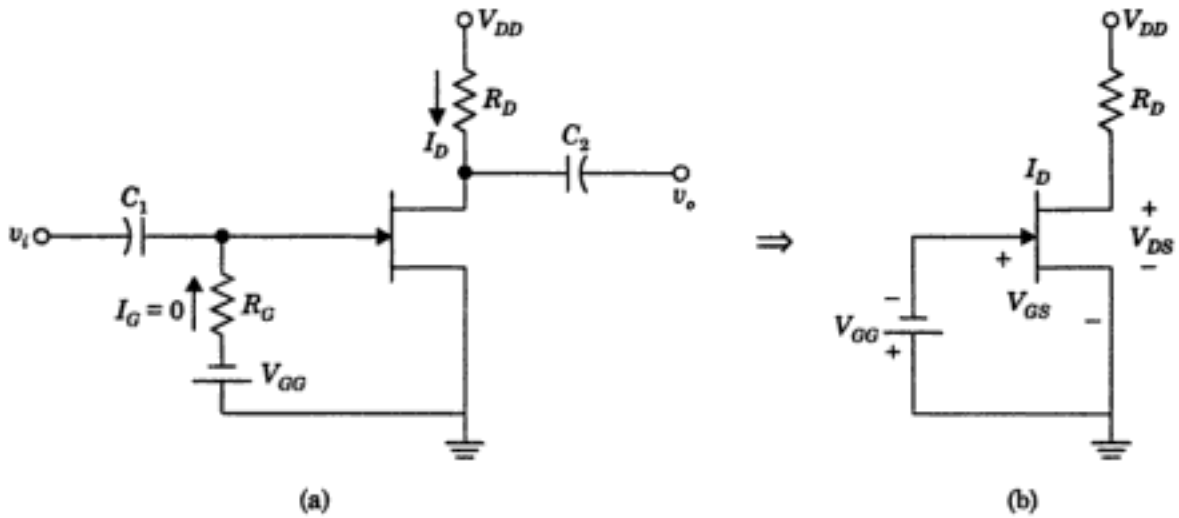


Fig. 7.27 (a) Fixed-bias arrangement for an *n*-channel JFET, (b) DC equivalent circuit.

The resistance R_G is usually high (in MΩ) and ensures that the input signal v_i appears at the input of the FET for ac analysis. As we are interested in the dc analysis, capacitors C_1 and C_2 can be taken as 'open circuits'. Further, as gate current $I_G = 0$, the voltage drop across R_G is zero and hence can be replaced by a short circuit in the dc equivalent circuit shown in Fig. 7.27(b).

It can be easily seen from Fig. 7.27(b) that

$$V_{GS} = -V_{GG} \tag{7.18}$$

As V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed and hence the name 'fixed-bias configuration'. The drain current I_D can be computed from the Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \tag{7.19}$$

where the values of I_{DSS} and V_P are provided by the manufacturer for a given transistor.

As is seen, the analysis in this circuit is simple, direct and can be done mathematically and one need not use graphical analysis.

The drain-to-source voltage, V_{DS} can be found by writing KVL for the output circuit as:

$$V_{DD} = I_D R_D + V_{DS} \tag{7.20}$$

or

$$V_{DS} = V_{DD} - I_D R_D \tag{7.21}$$

The fixed-bias arrangement, although very simple has the disadvantage that it uses a separate supply for biasing. This biasing arrangement is, therefore, rarely used in practice. This problem is eliminated in the self-biased arrangement.

EXAMPLE 7.3

Figure 7.28 shows an *n*-channel JFET using fixed bias configuration. It is given that I_{DSS} = 12 mA and $V_p = -4$ V. Determine I_{DQ} and V_{DSQ}.

Solution: As $I_G = 0$, we get from the gate source circuit,

$$V_{GS} = -1.5 \text{ V}$$

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Using Shockley's equation,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$= 12\left(1 - \frac{(-1.5)}{(-4)}\right)^2$$

$$= 12\left(1 - \frac{1.5}{4}\right)^2 = 4.7 \text{ mA}$$

So $I_{DQ} = 4.7$ mA

From the drain source circuit,

$$V_{DS} = V_{DD} - I_D R_D$$
$$= 12 - (4.7)(1.2)$$
$$= 12 - 5.64$$
$$= 6.36$$

i.e. $V_{DSQ} = 6.36$ V

Thus, the Q-point is:

$$I_{DQ} = 4.7 \text{ mA}$$
$$V_{DSQ} = 6.36 \text{ V}$$

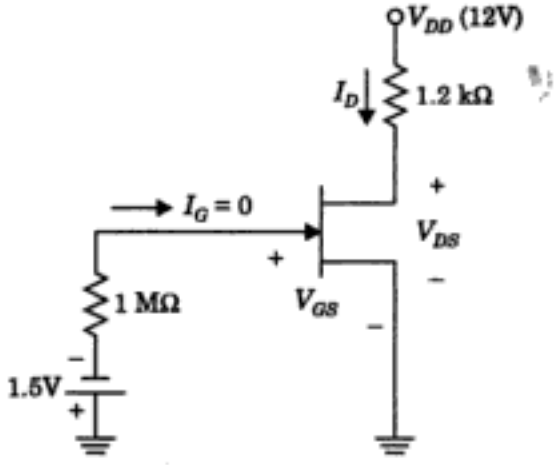


Fig. 7.28 Circuit for Ex. 7.3.

Self-bias configuration: A self-biased *n*-channel FET amplifier using a single power supply is shown in Fig. 7.29(a).

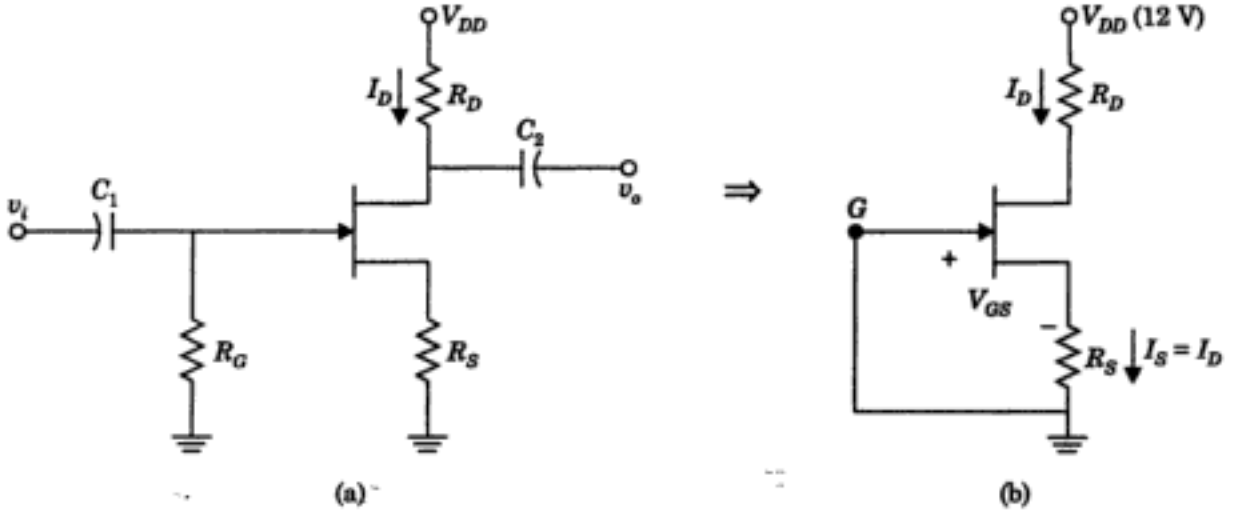


Fig. 7.29 (a) A self-biased *n*-channel JFET, (b) dc equivalent circuit.

In the dc equivalent circuit shown in Fig. 7.29(b) capacitors C_1 and C_2 are replaced by 'open circuits' and resistance R_G has been replaced by a short circuit as $I_G = 0$. In Fig. 7.29(b), it is seen from the gate source loop,

$$V_{GS} = -I_D R_S \qquad (7.22)$$

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For a mathematical solution, the value of V_{GS} is substituted in Shockley's equation as:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \tag{7.23}$$

$$= I_{DSS}\left(1 + \frac{I_D R_S}{V_p}\right)^2 \tag{7.24}$$

This gives a quadratic equation in I_D and can be solved for an appropriate solution for I_D. However, a graphical approach in this case is found to be more convenient.

In the graphical approach, first we plot the transfer characteristics of the JFET by the procedure described in section 7.3.2 and shown in Fig. 7.30. Equation 7.22 represents a straight line called the **bias line** and is plotted on the transfer characteristics. It can be seen that the bias line goes through the origin and has a slope of $-1/R_S$.

The intersection of the bias line with the transfer characteristics gives the operating point, that is, the values of the drain current I_{DQ} and gate-to-source voltage V_{GSQ} as shown in Fig. 7.30. The value of drain to source voltage V_{DSQ} can now be obtained from the KVL equation for the output loop

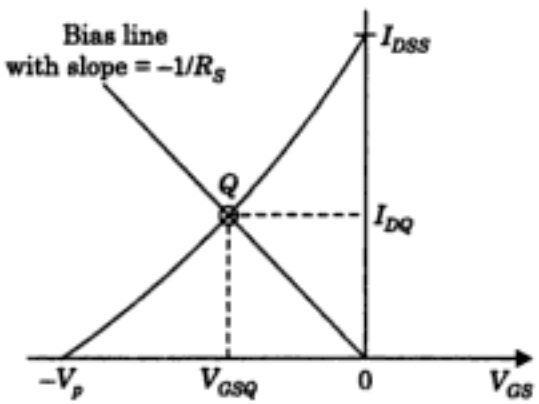


Fig. 7.30 Transfer characteristics of a JFET.

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S \tag{7.25}$$

Substituting the value of $I_D = I_{DQ}$ in Eq. (7.25), we can determine the value of V_{DSQ}.

EXAMPLE 7.4

Given $I_{DSS} = 6$ mA and $V_p = -6$ V for an n-channel JFET in the circuit shown in Fig. 7.31. Determine V_{DSQ}, I_{DSQ}, V_D and V_S.

Solution: The circuit is using self-bias configuration, therefore, it is convenient to use the graphical approach. As a first step, we plot the transfer characteristics using the Shockley's equation:

$$\therefore \quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$= 6\text{ mA}\left(1 - \frac{V_{GS}}{(-6\text{ V})}\right)^2$$

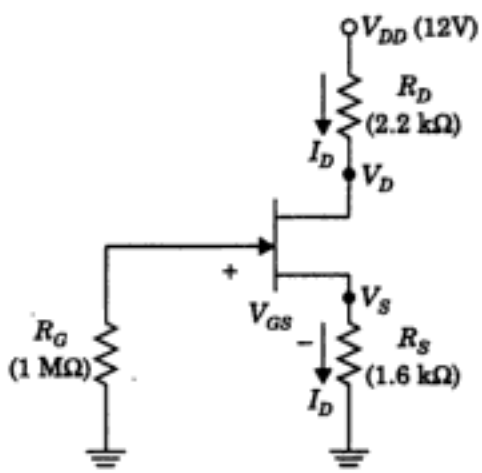


Fig. 7.31 Circuit for Example 7.4.

Using the four-point method for plotting the transfer characteristics discussed in section 7.3.2, we get

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Point 1: $V_{GS} = 0$ V $I_D = I_{DSS} = 6$ mA

Point 2: $V_{GS} = V_p = -6$ V $I_D = 0$ mA

Point 3: $V_{GS} = 0.3V_p = -1.8$ V $I_D = I_{DSS}/2 = 3$ mA

Point 4: $V_{GS} = 0.5V_p = -3.0$ V $I_D = I_{DSS}/4 = 1.25$ mA

The transfer curve using these four points is shown in Fig. 7.32.

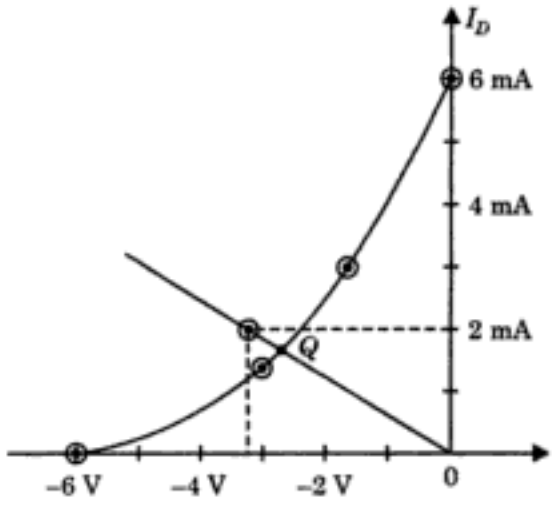


Fig. 7.32 Transfer characteristic for Example 7.4.

The bias line is obtained from the gate source circuit as:

$$V_{GS} = -I_D R_S$$
$$= -I_D\ (1.6\ \text{k}\Omega)$$

This is the equation of a straight line and we need two points to draw it. These two points can be

Point 1: $V_{GS} = 0$ V for $I_D = 0$

Point 2: $V_{GS} = 3.2$ V for $I_D = 2$ mA

and are shown in Fig. 7.32.

The operating point is found from the point of intersection of transfer characteristics with the bias curve as:

$$I_{DQ} = 1.6 \text{ mA}$$
$$V_{GSQ} = -2.7 \text{ V}$$

Writing the KVL for the output loop,

$$V_{DD} = I_D(R_D + R_S) + V_{DS}$$

So
$$V_{DSQ} = V_{DS} = V_{DD} - I_{DQ}\ (R_D + R_S)$$
$$= 12 - 1.6\ (2.2 + 1.6)$$
$$= 12 - 6.08 = 5.92 \text{ V}$$

Also
$$V_S = I_D R_S$$
$$= 1.6 \times 1.6$$
$$= 2.56 \text{ V}$$

and
$$V_D = V_{DSQ} + V_S$$
$$= 5.92 + 2.56$$
$$= 8.48 \text{ V}$$

Voltage-divider biasing: Another commonly used biasing arrangement called **voltage-divider biasing** is shown in Fig. 7.33(a). It can be seen that it is similar to self-bias or emitter bias circuit used for BJT biasing.

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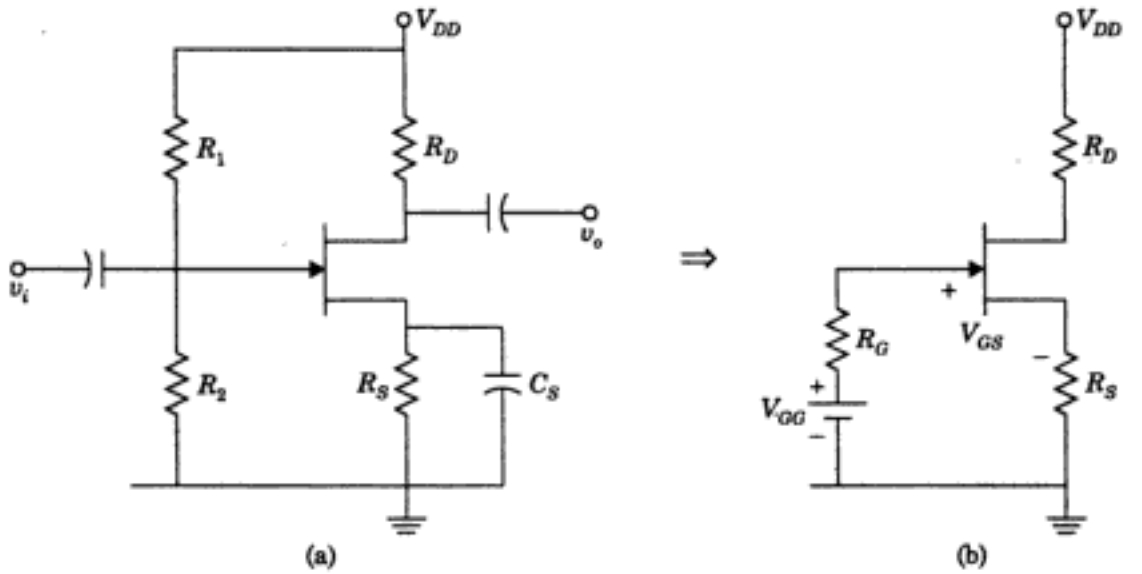


Fig. 7.33 (a) Voltage-divider biasing scheme for an *n*-channel JFET, (b) Simplified dc equivalent circuit.

The simplified dc equivalent circuit is shown in Fig. 7.33(b) where resistance divider network R_1 and R_2 have been replaced by its Thevenin's equivalent. The method of analysis for this circuit is demonstrated in Example 7.5.

EXAMPLE 7.5

An *n*-channel JFET has $V_p = -5$ V; $I_{DSS} = 12$ mA and is used in the circuit shown in Fig. 7.34. Determine the operating point.

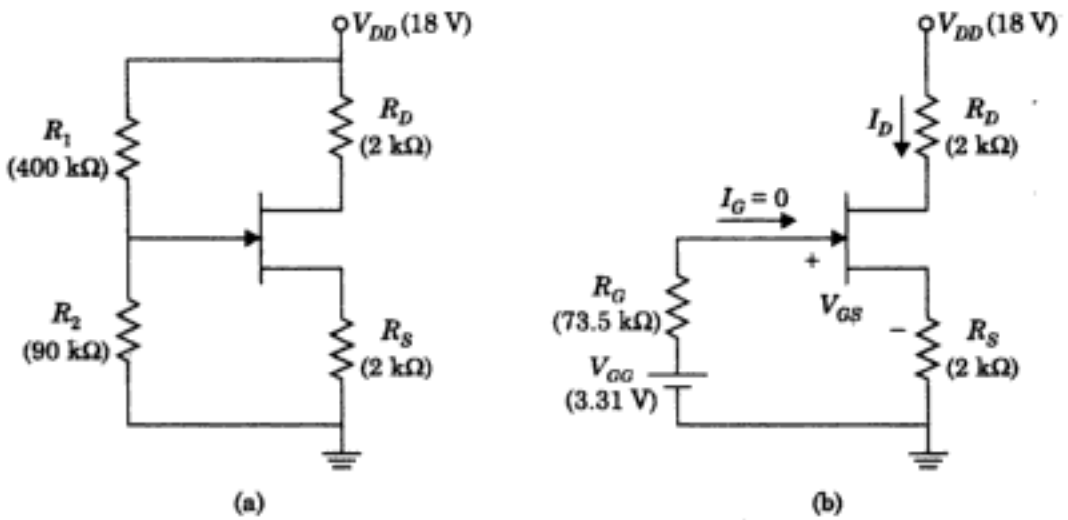


Fig. 7.34 (a) Circuit for Example 7.5, (b) Simplified circuit.

Solution: The transfer characteristic shown in Fig. 7.35 is first drawn by finding four points using the equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

where $I_{DSS} = 12$ mA and $V_p = -5$ V

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A simplified circuit is obtained by replacing the gate-bias resistor divider network R_1 and R_2 by its Thevenin's equivalent as shown in Fig. 7.33(b). Here,

$$V_{GG} = \frac{R_2}{R_1 + R_2} . V_{DD}$$

$$= \frac{90}{400 + 90} .18 = 3.31 \text{ V}$$

and $$R_G = R_1 \parallel R_2$$

$$= 400 \text{ k}\Omega \parallel 90 \text{ k}\Omega = 73.5 \text{ k}\Omega$$

The value of R_G infact is not required as current I_G through it is zero and as such there is no voltage drop across it. The bias line is obtained from the KVL for the gate-loop as:

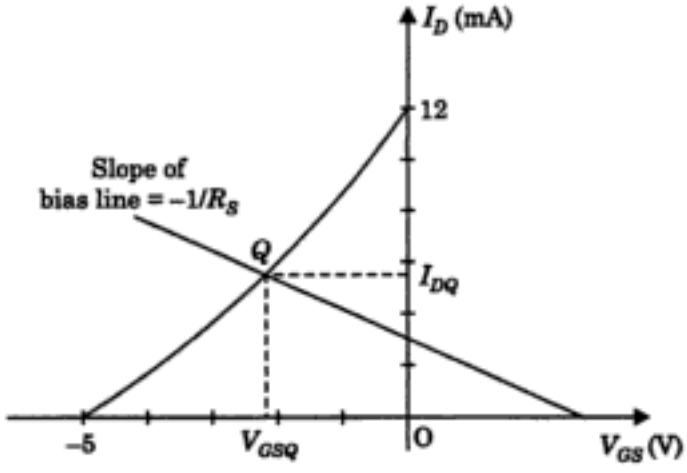


Fig. 7.35 Transfer-characteristics for the given JFET.

$$V_{GG} = V_{GS} + I_D R_S$$

or $$I_D = -\frac{V_{GS}}{R_S} + \frac{V_{GG}}{R_S}$$

For R_S = 2 kΩ, the intersection of the bias line with the transfer curve shown in Fig. 7.35 gives the Q-point as:

$$V_{GSQ} = -2.53 \text{ V}$$

$$I_{DQ} = 2.92 \text{ mA}$$

Writing KVL for the drain source loop, we have

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$V_{DS} = V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_S)$$

$$= 18 - 2.92 \ (2 + 2)$$

$$= 6.32 \text{ V}$$

Thus, $V_{DSQ} = 6.32$ V, $I_{DQ} = 2.92$ mA. **Ans.**

7.9.2 Biasing for MOSFETs

We have earlier discussed the two types of MOSFETs: (i) enhancement-type (ii) depletion-type. It may be noted that the transfer characteristics for JFET and depletion-type MOSFET are quite similar except the difference that the depletion-type MOSFET permits operation for positive values of V_{GS} as well and current I_D exceeds I_{DSS}. Due to the similarity of transfer characteristics, the various biasing configurations discussed for JFET are found to be suitable for depletion type MOSFETs as well.

However, the transfer characteristics of the enhancement-type MOSFET are quite different from that of JFET and depletion-type MOSFETs. It may be recalled that the drain characteristics of an n-channel enhancement-type MOSFET are given by

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$$I_D = k(V_{GS} - V_T)^2 \tag{7.26}$$

The value of k is determined from the typical values of I_D, V_{GS} and V_T provided. Once k is defined, the transfer characteristics are plotted. For an n-channel enhancement MOSFET, V_T is positive and transfer curve is plotted for the positive values of $V_{GS} > V_T$.

Out of the three biasing arrangements discussed for JFET, it is possible to use fixed-bias and voltage divider arrangement for biasing n-channel enhancement-type MOSFETs. However, the self-bias arrangement of the type shown in Fig. 7.29 cannot be used as the voltage drop across the resistance R_S is in a direction to reverse bias the gate, whereas we require a positive gate bias for n-channel enhancement-type MOSFETs.

A popular biasing arrangement for n-channel enhancement-type MOSFET is shown in Fig. 7.36(a).

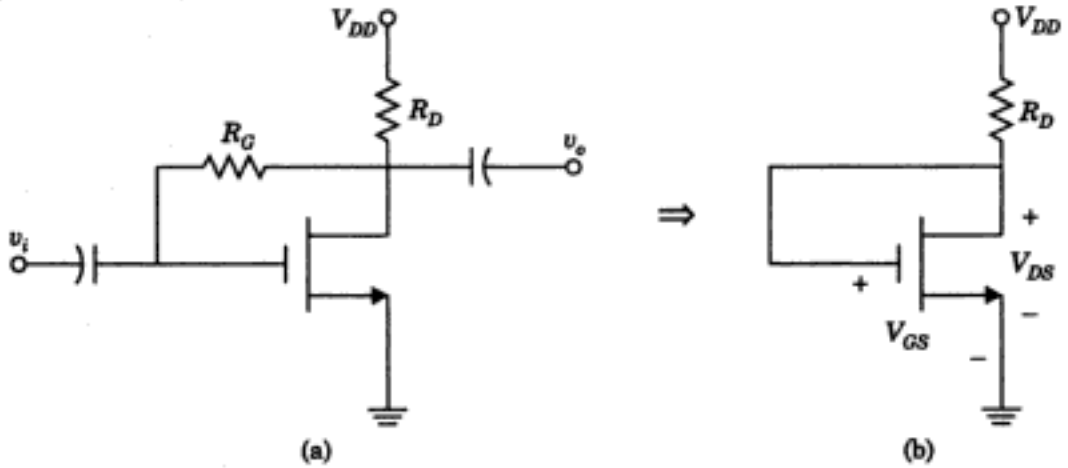


Fig. 7.36 (a) Feedback biasing arrangement for n-channel enhancement type MOSFET, (b) dc equivalent circuit.

The circuit uses a large feedback resistor R_G that forces the dc voltage at the gate to be equal to that at drain (as $I_G = 0$). From the dc equivalent circuit shown in Fig. 7.36(b) it can be seen that

$$V_{GS} = V_{DS} \tag{7.27}$$

and from the output circuit,

$$V_{DS} = V_{DD} - I_D R_D \tag{7.28}$$

or

$$V_{GS} = V_{DD} - I_D R_D \tag{7.29}$$

This equation when plotted on the transfer characteristics provides the Q-point at the point of intersection as shall be shown by Example 7.6

EXAMPLE 7.6

An n-channel enhancement type MOSFET amplifier shown in Fig. 7.37 has $I_D = 6$ mA for $V_{GS} = 8$ V and $V_T = 3$ V. Determine the dc operating conditions that is, compute V_{DSQ} and I_{DQ}.

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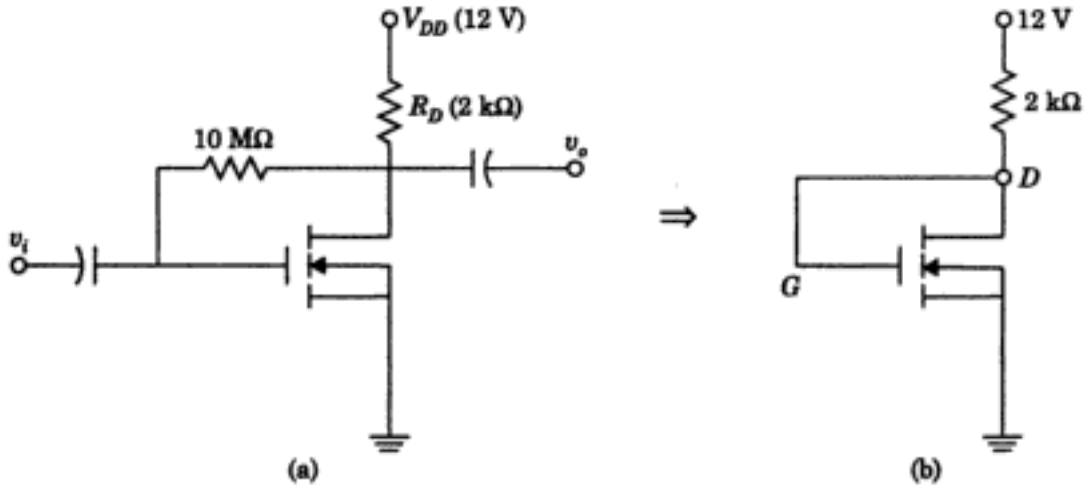


Fig. 7.37 (a) Circuit for Ex. 7.6, (b) Simplified dc equivalent circuit.

Solution: The transfer curve for the *n*-channel enhancement MOSFET is obtained from Eq. (7.16).

$$I_D = k(V_{GS} - V_T)^2$$

Therefore,

$$k = \frac{I_D}{(V_{GS} - V_T)^2}$$

$$= \frac{6}{(8-3)^2}$$

$$= 0.24 \times 10^{-3} \text{ A/V}^2$$

The curve,

$$I_D = 0.24 \times 10^{-3} (V_{GS} - 3)^2$$

is plotted as shown in Fig. 7.38.

The simplified dc equivalent circuit is shown in Fig. 7.37(b). The bias line is

$$V_{GS} = V_{DD} - I_D R_D$$
$$= 12 - I_D \times 2$$

The two extreme points on the bias line shown in Fig. 7.37(b) are given as:

V_{GS} = 12 V for I_D = 0 mA

and for V_{GS} = 0 V,

$$I_D = \frac{12}{2} = 6 \text{ mA}$$

The point of intersection gives the *Q*-point as:

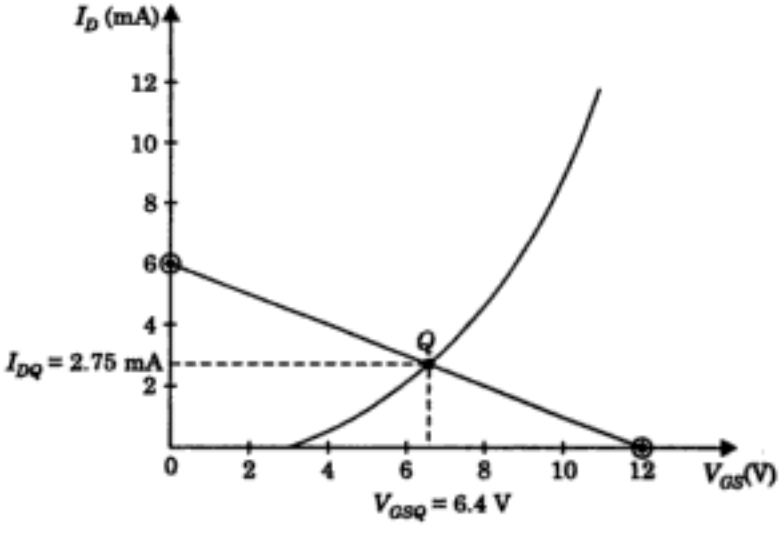


Fig. 7.38 Transfer characteristics for finding *Q*-point graphically.

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$$V_{GSQ} = 6.4 \text{ V}$$

$$I_{DQ} = 6.4 \text{ V}$$

and $$V_{DSQ} = V_{GSQ} = 6.4 \text{ V}$$

EXAMPLE 7.7

Determine the operating point, i.e., I_{DQ}, V_{DSQ} and V_{GSQ} for the voltage divider biased n-channel enhancement type MOSFET shown in Fig. 7.39(a). It is given that $V_T = 3$ V, and $I_D = 5$ mA for $V_{GS} = 6$ V.

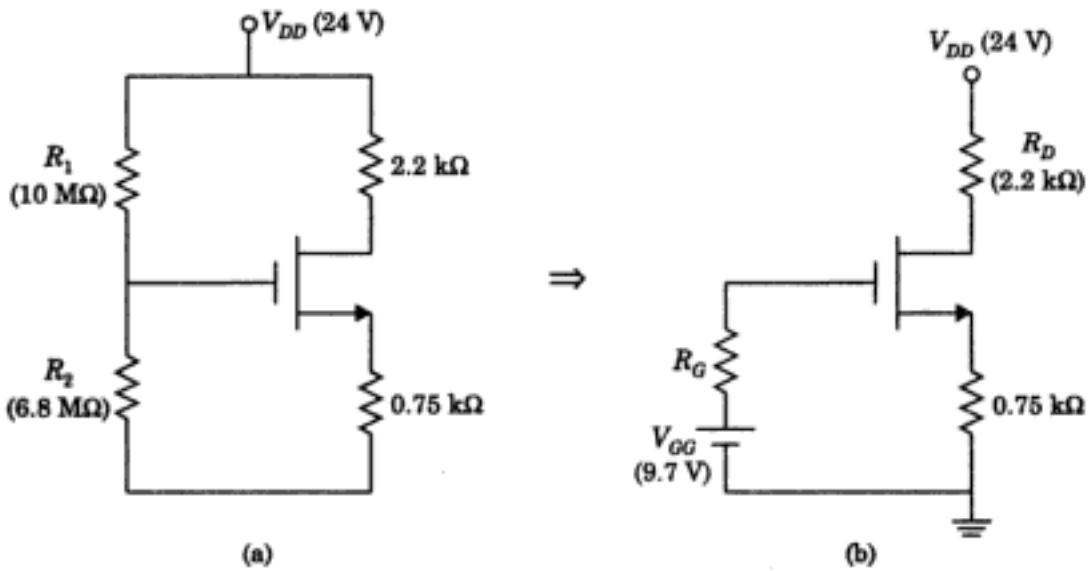


Fig. 7.39 (a) Circuit for Example 7.7, (b) Simplified circuit diagram.

Solution: The transfer characteristics of the n-channel enhancement type MOSFET are obtained using Eq. (7.16).

$$k = \frac{I_D}{(V_{GS} - V_T)^2}$$

$$= \frac{5}{(6-3)^2}$$

$$= 0.56 \times 10^{-3} \text{ A/V}^2$$

Thus, $$I_D = k(V_{GS} - V_T)^2$$

$$= 0.56 \times 10^{-3} (V_{GS} - 3)^2$$

The transfer curve obtained is shown in Fig. 7.40.

The simplified circuit diagram using Thevenin's equivalent representation of voltage divider network is shown in Fig. 7.39(b), where

$$V_{GG} = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{(6.8)(24)}{10 + 6.8} = 9.7 \text{ V}$$

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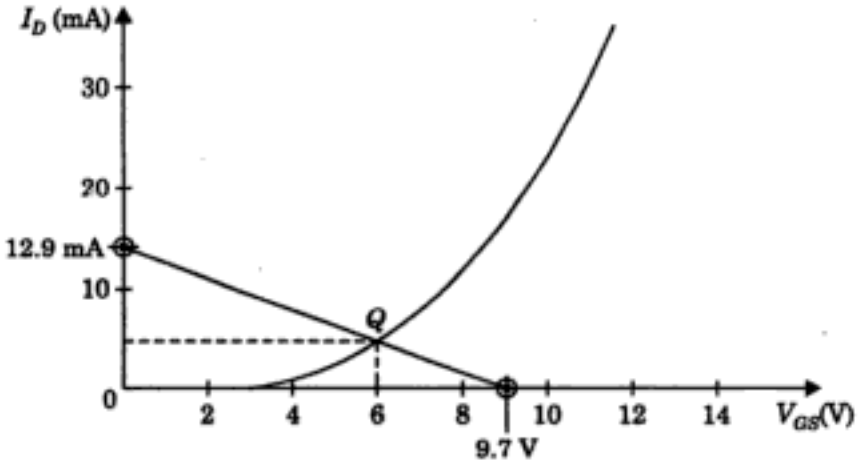


Fig. 7.40 Transfer curve for finding Q-point.

There, is no need to compute the value of R_G as no current flows through it. The equation for the bias curve is obtained by writing KVL for the gate-source loop as:

$$V_{GS} = V_{GG} - I_D R_S$$
$$= 9.7 - I_D(0.75)$$

Thus, for $I_D = 0$ mA, $V_{GS} = 9.7$ V

and for $V_{GS} = 0$ V, $I_D = \dfrac{9.7}{0.75} = 12.9$ mA

The bias curve is obtained by joining these two extreme points as shown in Fig. 7.40. The point of intersection of the bias curve with transfer characteristics gives the Q-point and is obtained from Fig. 7.40, as:

$$V_{GSQ} = 6 \text{ V}$$
$$I_{DQ} = 5 \text{ mA}$$

The value of V_{DSQ} is obtained from the output circuit as,

$$V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_S)$$
$$= 24 - 5\ (2.2 + 0.75)$$
$$= 24 - 14.75 = 9.25 \text{ V}$$

SUMMARY

- FET is a unipolar device as current is conducted by one type of carriers only (electrons in n-channel and holes in p-channel).
- Compared to BJTs, FETs have higher input impedance, better temperature stability, less noise, are smaller in size and easy to fabricate.
- FETs are suitable for VLSI circuits as they occupy less area on the silicon chip compared to BJT.

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- An FET is a voltage controlled device whereas BJT is a current controlled device.
- The output/drain characteristics of a JFET have four regions of operation: (i) ohmic region, (ii) saturation or pinch-off region, (iii) breakdown region and (iv) cut-off region.
- The transfer characteristics of a JFET is expressed by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

where I_{DSS} is the value of I_D for $V_{GS} = 0$.

- MOSFETs are of two types: (i) enhancement MOSFET and (ii) depletion MOSFET.
- MOSFETs provide very high input impedance (~ 10^{10} to 10^{18} Ω) compared to JFET as the gate is insulated from the substrate by a silicon dioxide or polysilicon layer.
- In enhancement MOSFET, the gate-to-source voltage V_{GS} should be greater than a threshold voltage, V_T so as to conduct the device. V_T is positive for *n*-channel enhancement MOSFET and negative for a *p*-channel enhancement MOSFET.
- The three regions of operation of a *n*-channel enhancement MOSFET are:

Cut-off:	$V_{GS} \leq V_T$
Ohmic:	$V_{DS} \leq V_{GS} - V_T$
Saturation:	$V_{DS} \geq V_{GS} - V_T$

- The transfer characteristics of an NMOS are given by the relationship:

$$I_D = k(V_{GS} - V_T)^2$$

- For use as an amplifier, FET should be biased in the saturation region. For switching applications, device operates in the cut-off and ohmic regions.
- *p*-channel enhancement MOSFET (PMOS) are less popular as they provide less current (hole mobility < electron mobility) and occupy three times the area occupied by NMOS.
- Depletion-type MOSFET have an *n*-channel embedded in the substrate between source and drain.
- A depletion-type MOSFET can be used both with V_{GS} positive and negative, i.e., enhancement and depletion modes, respectively.
- Complementary MOS devices (CMOS) have virtually replaced NMOS in all the VLSI circuits due to very low power dissipation.
- MESFET (GaAs-devices) are useful in high speed digital applications and high frequency analog applications.
- The biasing of JFET/MOSFET can be done by using: (i) fixed-bias, (ii) self-bias or (iii) voltage divider biasing as in the case of BJT.
- The dc analysis of JFET/MOSFET is usually done by graphical analysis, that is, first plotting the transfer characteristics and finding the point of intersection with the bias-line.

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P7.2 Sketch the transfer characteristics of a JFET with I_{DSS} = 12 mA and V_p = –4 V.

P7.3 Sketch the transfer characteristics of an *n*-channel enhancement type MOSFET if V_T = 3.5 V and $k = 0.4 \times 10^{-3}$ A/V^2.

P7.4 Given V_T = 4 V and I_D = 4 mA at V_{GS} = 6 V, determine k and plot the transfer characteristics of the MOSFET.

(***Ans.*** 1×10^{-3} A/V^2)

P7.5 Given $k = 0.4 \times 10^{-3}$ A/V^2 and I_D = 3 mA at V_{GS} = 4 V, determine V_T.

(***Ans.*** 1.27 V)

P7.6 If V_T = –5 V and $k = 0.45 \times 10^{-3}$ A/V^2, what type of MOSFET it is? Sketch its transfer characteristics.

P7.7 For a depletion-type MOSFET, it is given that I_D = 14 mA at V_{GS} = 1 V. Determine V_p if I_{DSS} = 9.5 mA.

(***Ans.*** V_p –4.76 V)

P7.8 For an *n*-channel JFET shown in Fig. 7.41 determine V_D. Given: I_{DSS} = 8 mA, V_P = –4 V.

(***Ans.*** 18 V)

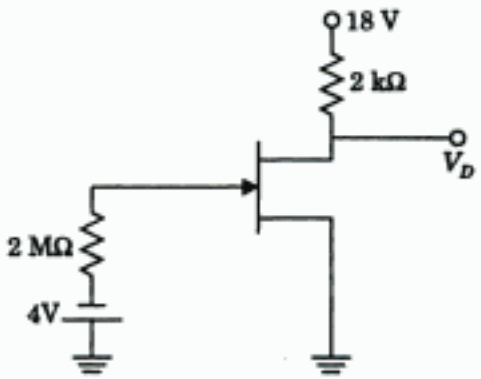


Fig. 7.41 Circuit for P7.8.

P7.9 For the *n*-channel JFET using self-bias as shown in Fig. 7.42, it is given that voltage at source V_S = 1.7 V. Determine (i) I_{DQ} (ii) V_{GSQ} (iii) I_{DSS} and V_D.

(***Ans.*** 3.33 mA, –1.7 V, 10.06 mA, 11.34 V)

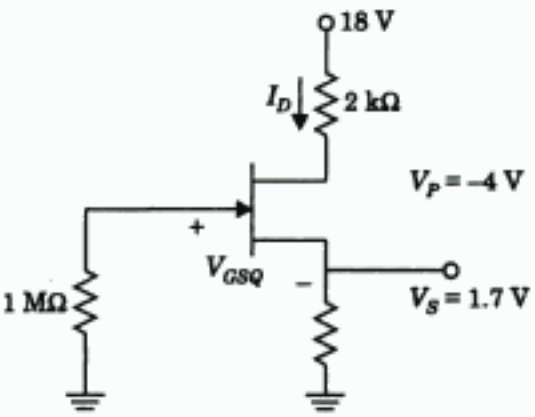


Fig. 7.42 Circuit for P7.9.

P7.10 The JFET in the circuit of Fig. 7.43 has I_{DSS} = 4 mA and V_P = –4 V. Find

(a) V_o for V_i = 0

(b) V_o for V_i = 15 V

(***Ans.*** 1.85 V, 15.95 V)

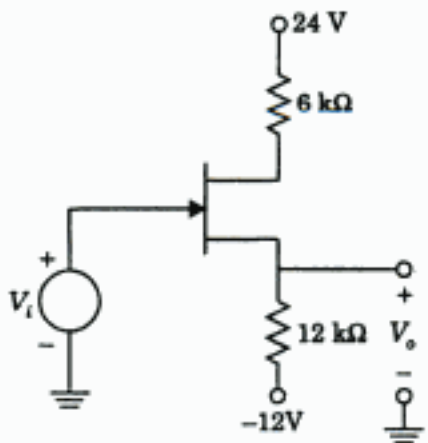


Fig. 7.43 Circuit for P7.10.

P7.11 For the given readings in each configuration shown in Fig. 7.44, discuss the operation of the network.

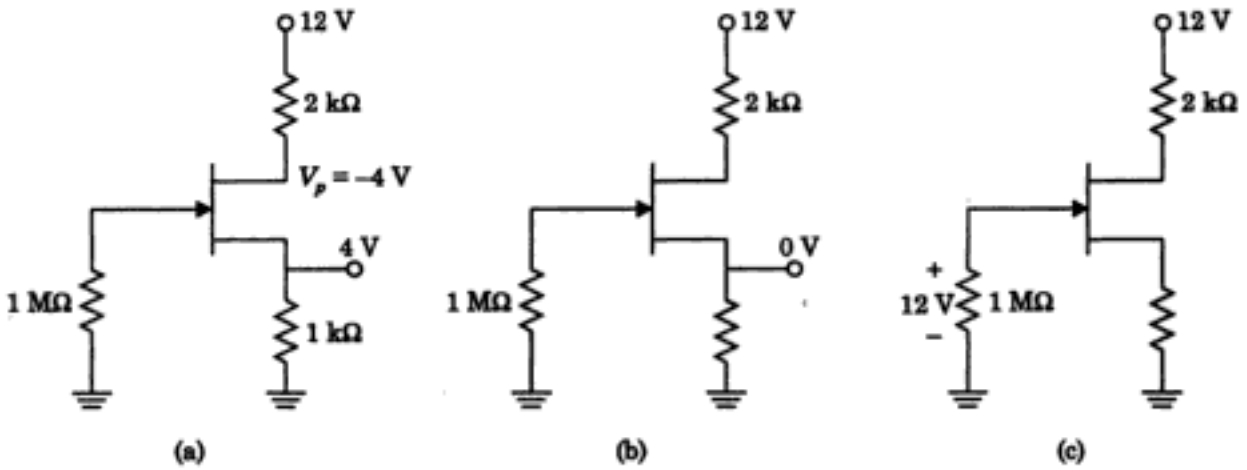


Fig. 7.44 Circuits for P7.11

P7.12 Design a self-bias configuration for a *n*-channel JFET having I_{DSS} = 8 mA and $V_p = -6$ V. The *Q*-point is at I_{DQ} = 4 mA with a supply voltage of 14 V. Assume $R_D = 3\ R_S$.

(***Ans.*** R_S = 0.43 kΩ, R_D = 1.3 kΩ)

P7.13 The *n*-channel JFET in Fig. 7.45 has I_{DSS} = 10 mA and V_p = –3.5 V. Determine: I_{DQ}, V_{GSQ} and V_{DSQ}.
(***Ans.*** I_{DQ} = 5.8 mA, V_{GSQ} = –0.85 V, V_{DSQ} = 4.29 V)

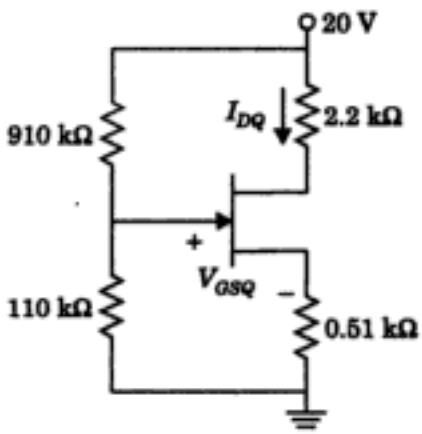


Fig. 7.45 Circuit for P7.13.

P7.14 Determine the operating point (I_{DQ}, V_{GSQ}) for a self-biased depletion-type *n*-channel MOSFET shown in Fig. 7.46. Given: I_{DSS} = 6 mA, V_p = –4 V.

(***Ans.*** 2.9 mA, –1.2 V)

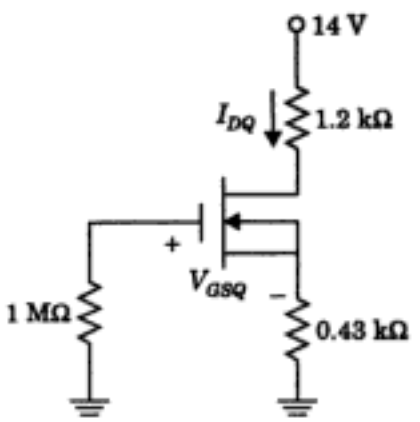


Fig. 7.46 Circuit for P7.14.

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P7.15 An *n*-channel enhancement-type MOSFET uses the biasing arrangement as shown in Fig. 7.47. The device parameters are given as $V_T = 4$ V, $I_D = 5$ mA at $V_{GS} = 7$ V. Determine I_{DQ}, V_{GSQ} and V_{DSQ}.

(***Ans.*** $I_{DQ} = 8.25$ mA, $V_{GSQ} = V_{DSQ} = 7.9$ V)

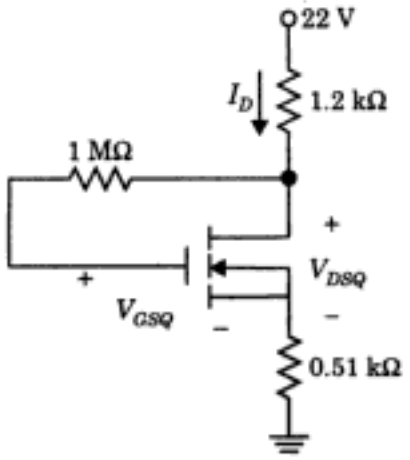


Fig. 7.47 Circuit for P7.15.

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CHAPTER 8 FET Amplifiers

8.1 INTRODUCTION

It was shown in Chapter 7 that FET behaves as a voltage controlled current source as the output (drain) current is controlled by means of a small (gate voltage) input voltage. In comparison, BJT is a current controlled current source as the output (collector) current is controlled by input (base) current. Further, FET has much higher input impedance compared to BJT. Because of these characteristics of an FET, this device is more suitable as a voltage amplifier compared to BJT.

In this chapter, we discuss the small signal model of JFET for (i) low frequencies (b) high frequencies. These models are valid for MOSFET as well. The analysis of JFET as an amplifier in different configurations, that is, CS, CD and CG are discussed.

An FET whether a JFET or MOSFET can be used both as an amplifier or a switch. However, MOSFETs are more popular as these can be made quite small and their fabrication process is relatively simple. Various digital logic circuits and memory circuits can be implemented using MOSFETs only (no resistors or diodes are needed). The basic circuit application of the MOSFET as a resistance and a digital logic inverter is discussed.

8.2 FET SMALL SIGNAL MODEL AT LOW FREQUENCIES

A linear small signal model for an FET can be developed by expressing the drain current i_D as a function of gate-source voltage v_{GS} and drain source voltage v_{DS} as:

$$i_D = f(v_{GS}, v_{DS}) \tag{8.1}$$

The change in the drain current when both v_{GS} and v_{DS} are varied about the Q-point is expressed approximately by the first two terms of Taylor's series as:

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$$\Delta i_D = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{DS}} \times \Delta v_{GS} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{V_{GS}} \times \Delta v_{DS} + \cdots \text{ neglecting the higher order terms} \quad (8.2)$$

Using the small signal notation as in the case of BJTs, Eq. (8.2) can be written as

$$i_d = g_m v_{gs} + \frac{1}{r_d} v_{ds} \quad (8.3)$$

where

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{DS}}$$

$$\simeq \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_{V_{DS}} = \left.\frac{i_d}{v_{gs}}\right|_{V_{DS}} \quad (8.4)$$

and is called **transconductance** or **mutual conductance.** The value of g_m is found at the operating point $V_{DS} = V_{DSQ}$, which is found by dc analysis as discussed in Chapter 7. The second parameter in Eq. (8.3) r_d is called the **drain resistance** which is defined as:

$$r_d = \left.\frac{\partial v_{DS}}{\partial i_D}\right|_{V_{GS}}$$

$$\simeq \left.\frac{\Delta v_{DS}}{\Delta i_D}\right|_{V_{GS}} = \left.\frac{v_{ds}}{i_d}\right|_{V_{GS}} \quad (8.5)$$

There is one more parameter called **amplification factor** μ for an FET defined by

$$\mu = -\left.\frac{\partial v_{DS}}{\partial v_{GS}}\right|_{I_D}$$

$$= -\left.\frac{\Delta v_{DS}}{\Delta v_{GS}}\right|_{I_D} = -\left.\frac{v_{ds}}{v_{gs}}\right|_{i_d = 0} \quad (8.6)$$

In this definition of μ, a negative sign has been intentionally taken to obtain a positive value of μ as V_{DS} and V_{GS} are of opposite sign. It can be easily shown that μ is related to g_m and r_d by the relation:

$$\mu = r_d g_m \quad (8.7)$$

Based on Eq. (8.3), we can draw a circuit as shown in Fig. 8.1(a), and it gives the low frequency small signal model of an FET.

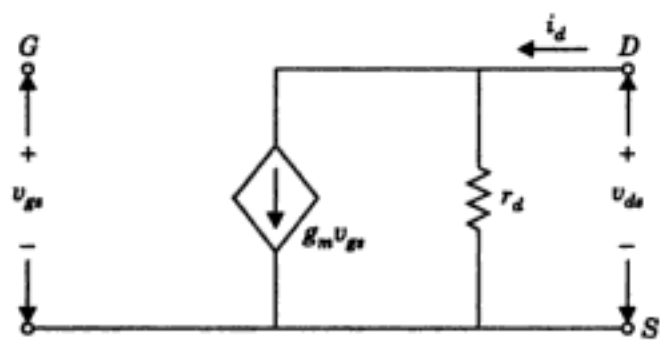


Fig. 8.1(a) Low frequency small signal FET model.

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The small signal model shown in Fig. 8.1(a) characterizes the device as a voltage controlled current source. The device can also be modelled as a voltage controlled voltage source by replacing it by Thevenin's equivalent circuit as shown in Fig. 8.1(b). The voltage controlled voltage model is found to be very convenient in amplifier analysis as shall be seen later. It may be noted from both the models shown in Figs. 8.1(a) and 8.1(b) that the input impedance between gate and source is infinite, since gate is reverse biased and $I_G = 0$.

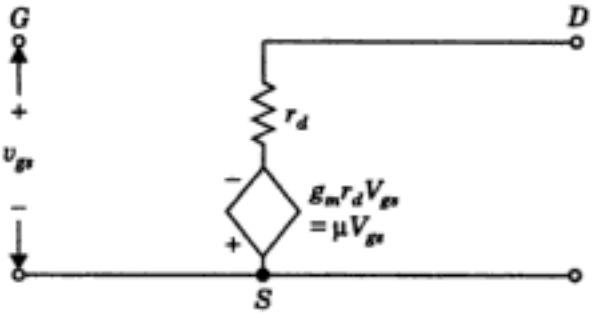


Fig. 8.1(b) Voltage controlled voltage source model of FET.

High frequency model of JFET. The small signal models developed in Figs. 8.1(a) and (b) are valid only at low frequencies where internal junction capacitances have not been taken into account. The use of these models would predict constant amplifier gain which does not change with frequency. However, in practice, the gain of an amplifier falls off at some high frequency. This fall of gain at high frequencies is due to the presence of internal junction capacitances. Thus, the model of JFET at high frequencies is modified to the one shown in Fig. 8.2. This model will be used when we discuss the frequency response of JFET amplifiers in Chapter 10.

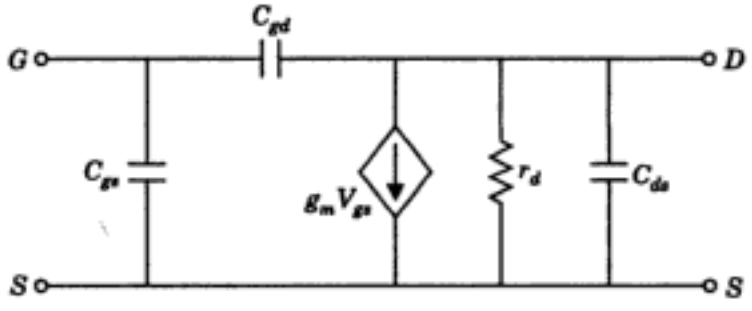


Fig. 8.2 High frequency model of FET with internal capacitances.

Determination of g_m and r_d. The value of g_m of a JFET can be found graphically from the transfer characteristics. Figure 8.3 shows the transfer characteristics for an *n*-channel JFET.

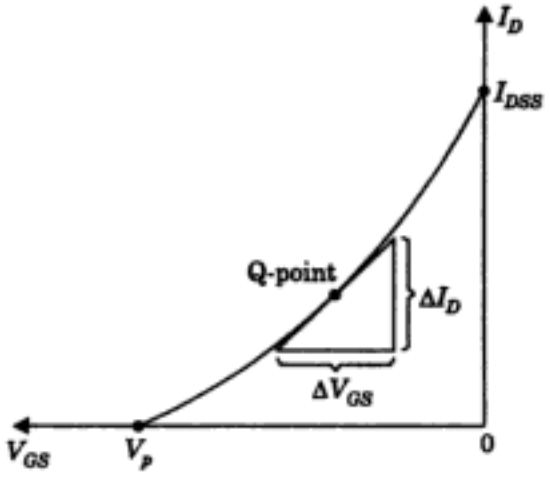


Fig. 8.3 Defining g_m on the transfer characteristics.

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In Fig. 8.3 it can be seen that g_m is the slope of the transfer characteristics at the quiescent point. Thus, for the Q-point in Fig. 8.3,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ (= slope at Q-point)} \tag{8.8}$$

The value of g_m increases as we move from V_p to I_{DSS} on the transfer characteristics.

EXAMPLE 8.1

A JFET has I_{DSS} = 12 mA and V_p = –5 V. Find the magnitude of g_m at V_{GS} = –1.5 V.

Solution: First plot the transfer characteristics using the 4-point method described in Chapter 7, Section 7.3.2. The transfer characteristics so obtained are shown in Fig. 8.4. The Q-point has also been indicated at V_{GS} = –1.5 V.

The value of g_m is obtained as:

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{GS}=-1.5\,\text{V}}$$

$$= \frac{3.4\,\text{mV}}{1\,\text{V}} = 3.4\,\text{mA/V}$$

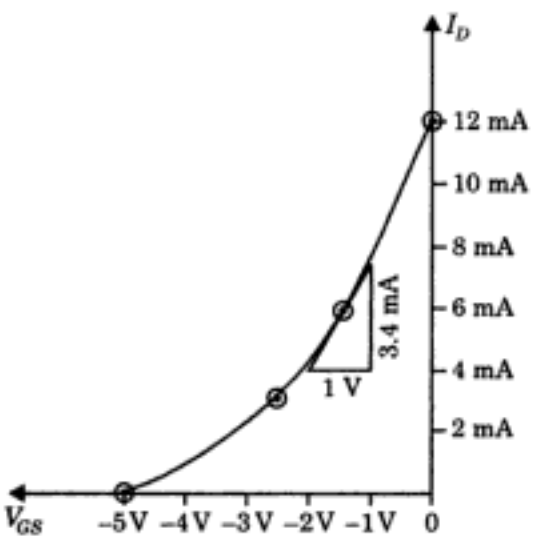


Fig. 8.4 Calculating g_m from the transfer characteristics in Example 7.1.

The graphical approach for finding the value of g_m is quite cumbersome, therefore, we now discuss an alternate method of computing g_m analytically.

Using Shockley's equation,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \tag{8.9}$$

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and differentiating w.r.t. V_{GS}, we can write

$$g_m = \frac{dI_D}{dV_{GS}}\bigg|_{\text{Q-point}} = 2I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)\frac{d}{dV_{GS}}\left(1-\frac{V_{GS}}{V_p}\right) \tag{8.10}$$

$$= 2I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)\left(-\frac{1}{V_p}\right)$$

$$= \frac{2I_{DSS}}{|V_p|}\left(1-\frac{V_{GS}}{V_p}\right) \tag{8.11}$$

or
$$g_m = g_{mo}\left(1-\frac{V_{GS}}{V_p}\right) \tag{8.12}$$

where
$$g_{mo} = g_m\big|_{V_{GS}=0} = \frac{2I_{DSS}}{|V_p|} \tag{8.13}$$

Now, solving Example 7.1 by using Eqs. (8.12) and (8.13), we get

$$g_{mo} = \frac{2\times 12}{5} = 4.8\ \text{mS}$$

So
$$g_m = 4.8\left(1-\frac{1.5}{5}\right) = 3.36\ \text{mS}$$

Thus, we can see that analytical approach is much simpler.

The parameter r_d in the small signal model of JFET represents its output impedance and therefore is computed from the drain or output characteristics as shown in Fig. 8.5.

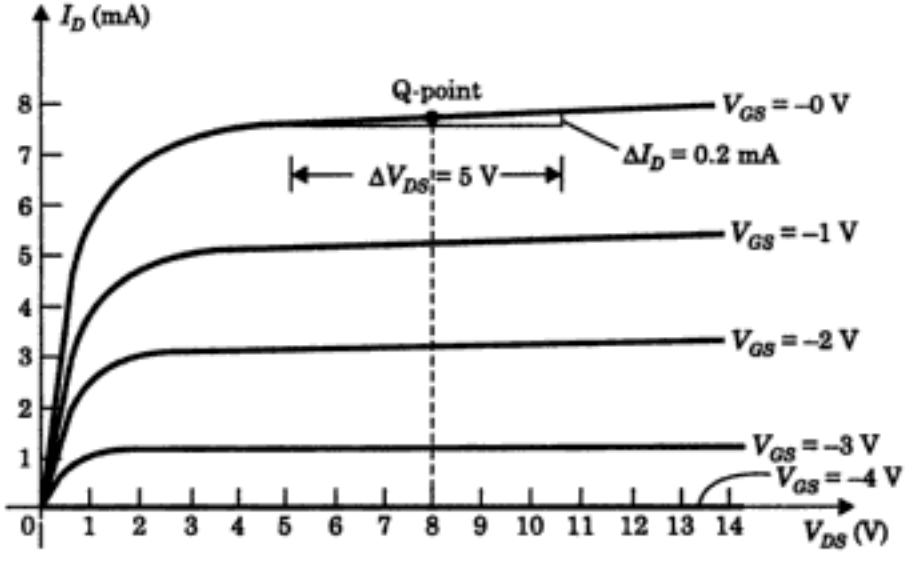


Fig. 8.5 Calculating r_d from the drain characteristics of a JFET.

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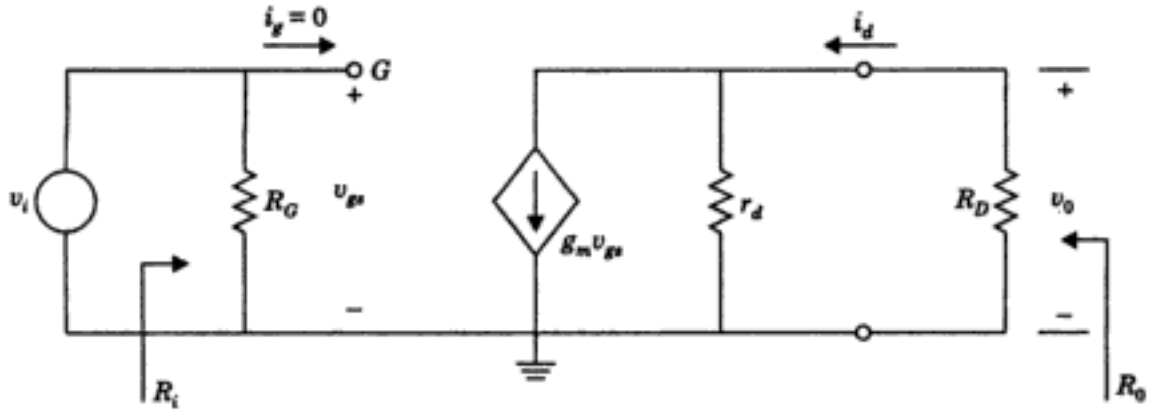


Fig. 8.6(b) ac equivalent circuit of CS amplifier shown in Fig. 8.6(a).

Input impedance R_i

The input impedance of JFET as seen at the gate terminal is infinity, thus it is clearly seen that the overall input impedance R_i in Fig. 8.6(b) is:

$$R_i = R_G \tag{8.15}$$

Output impedance R_0

In Fig. 8.6(b), setting $v_i = 0$ will make the current source $g_m v_{gs}$ equal to zero. Thus,

$$R_0 = r_d \parallel R_D \tag{8.16}$$

Voltage gain A_V

In Fig. 8.6(b),

$$v_{gs} = v_i \tag{8.17}$$

and

$$v_0 = g_m v_{gs} (r_d \parallel R_D) \tag{8.18}$$

Therefore,

$$A_V = \frac{v_0}{v_i}$$

$$= -g_m (r_d \parallel R_D) \tag{8.19}$$

$$= -g_m \frac{r_d R_D}{r_d + R_D}$$

$$= -\frac{\mu R_D}{r_d + R_D} \tag{8.20}$$

For

$$r_d \geq 10\, R_D$$

$$A_V \simeq -g_m R_D \tag{8.21}$$

The negative sign in Eq. (7.21) clearly indicates that FET also provides a 180° phase shift between input and output voltages as in the case of BJT.

EXAMPLE 8.2

Calculate the voltage gain of a fixed-bias CS amplifier shown in Fig. 8.7. The FET parameters are: $g_m = 2$ mA/V, $r_d = 10$ kΩ.

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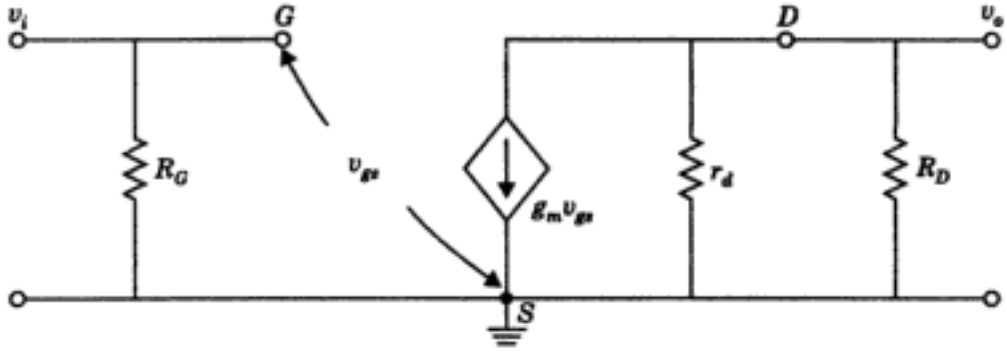


Fig. 8.8(b) ac equivalent circuit of circuit shown in Fig. 8.8(a).

It can be easily seen that the ac equivalent circuit shown in Fig. 8.8(b) is same as that for a fixed-bias configuration. Thus, the expressions for R_i, R_0 and A_V remains to be same.

Unbypassed R_s: A self-biased JFET amplifier where resistance R_S has not been bypassed is shown in Fig. 8.9(a).

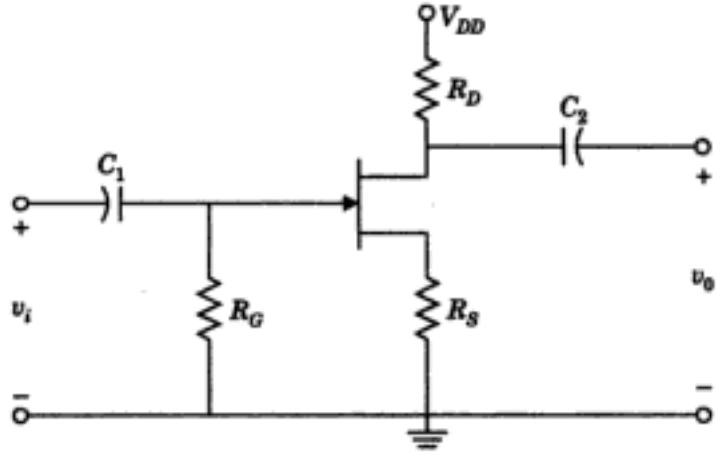


Fig. 8.9(a) A self-biased JFET amplifier with unbypassed R_S.

The ac equivalent circuit using the voltage controlled voltage source model of JFET is shown in Fig. 8.9(b).

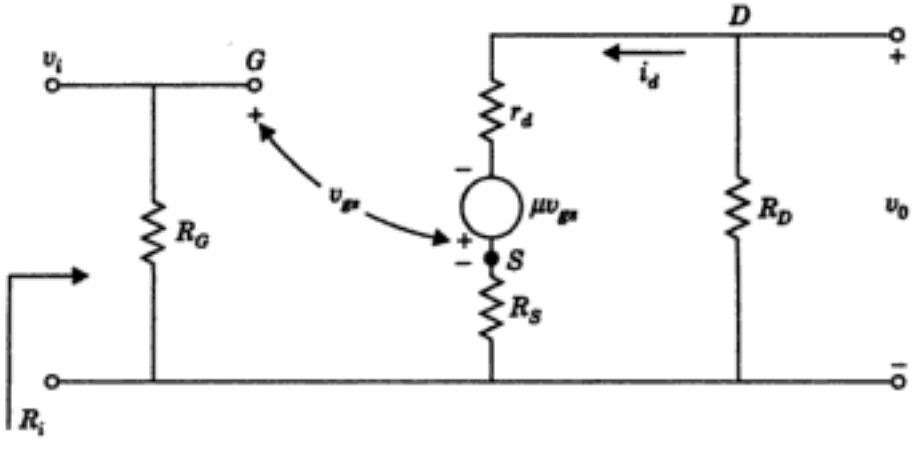


Fig. 8.9(b) ac equivalent circuit.

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Voltage gain A_V

Using Eq. (8.27),

$$A_V = -\frac{\mu R_D}{R_D + r_d + (1+\mu)R_S}$$

$$= -\frac{(75.5)}{3.3 + 50 + (1+75.5)1}$$

$$= -1.91$$

It may be noted that the voltage gain of a JFET amplifier is usually much smaller than that can be obtained from a BJT amplifier of the same configuration. However, as input resistance R_i is much greater compared to that of a BJT amplifier, the overall gain of the FET system is quite reasonable.

8.3.2 JFET Common Drain (CD) Amplifier (Source Follower)

A JFET source follower has the same features as that of an emitter follower in BJT circuits. The circuit of a JFET source follower is shown in Fig. 8.12(a). The output is taken from the source terminal and drain is directly connected to the dc supply. Thus, the drain terminal is at ground potential under ac conditions and hence the name common drain amplifier. As expected, voltage gain of a source follower is less than unity, has a high input impedance and low output impedance. The ac equivalent circuit is shown in Fig. 8.12(b) where the JFET has been replaced by its voltage source equivalent model, capacitors C_1, C_2 and supply voltage V_{DD} are short circuited.

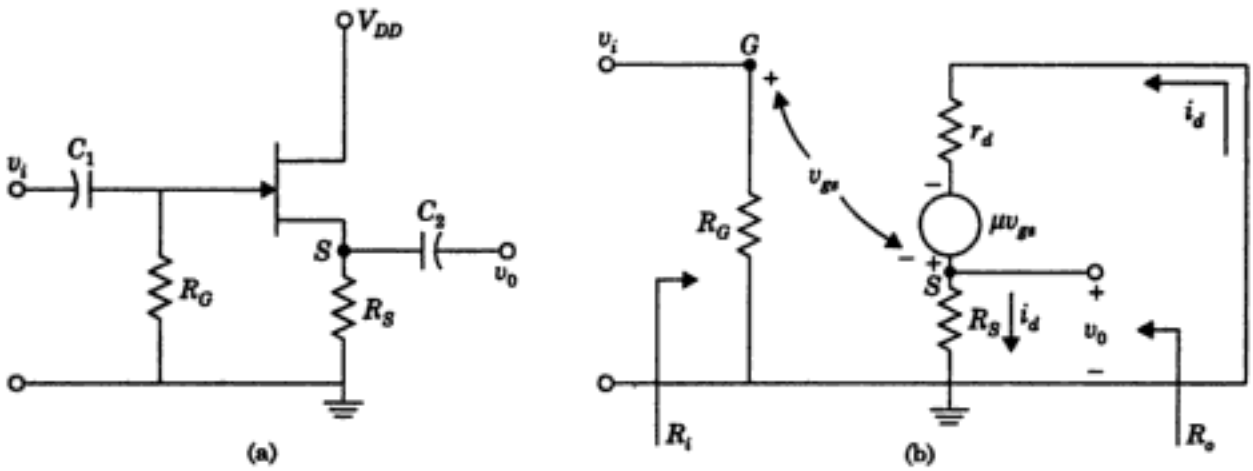


Fig. 8.12 (a) A JFET source follower, (b) ac equivalent circuit.

Voltage gain A_V

From the ac equivalent circuit, we may write,

$$v_i = v_{gs} + i_d R_S \tag{8.35}$$

and

$$i_d(r_d + R_S) - \mu v_{gs} = 0 \tag{8.36}$$

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$$I_{DQ} = 4.56 \text{ mA}$$

$$V_{GSQ} = -2.8 \text{ V}$$

The value of g_m is found from Eq. (8.12)

$$g_m = g_{mo}\left(1 - \frac{V_{GSQ}}{V_p}\right)$$

where $$g_{mo} = \frac{2I_{DSS}}{|V_p|}$$ [Eq. (8.13)]

$$= \frac{2 \times 16}{4} = 8 \text{ mA/V}$$

Therefore, $$g_m = 8\left(1 - \frac{(-2.86)}{(-4)}\right)$$

$$= 2.28 \text{ mA/V}$$

Given $r_d = 40 \text{ k}\Omega$

So $\mu = r_d g_m$

$= (40)\ (2.28) = 91.2$

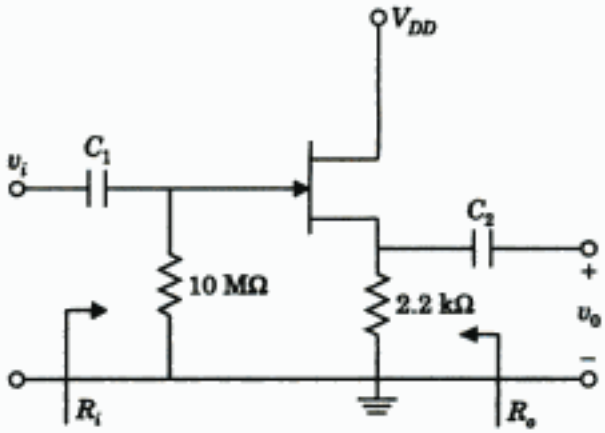


Fig. 8.14 Circuit for Example 8.4.

From Eq. (8.39),

$$A_V = \frac{\mu R_S}{r_d + (1+\mu)R_S}$$

$$= \frac{(91.2)(2.2)}{40 + (1 + 91.2)\,2.2} = 0.82$$

From Eq. (8.40)

$$R_i = 10 \text{ M}\Omega$$

From Eq. (8.44)

$$R_0 = \frac{r_d R_S}{r_d + (1+\mu)R_S}$$

$$= \frac{40 \times 2.2}{40 + (1 + 91.2)\,2.2}$$

$$= 0\,362 \text{ k}\Omega$$

8.3.3 JFET Common Gate Amplifier

The circuit of a JFET common gate amplifier is shown in Fig. 8.15(a). The circuit provides low input impedance, high output impedance and moderate voltage gains. Note that the resistance connected at the input terminals is R_S and not R_G. The value of R_S is usually a few kiloohms and not as large as R_G.

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Using Eqs. (8.45), (8.46), (8.47) and solving for R_i gives

$$R_i = \frac{(R_D + r_d)R_S}{R_D + r_d + (1+\mu)R_S} \tag{8.51}$$

which can also be written as:

$$R_i = R_S \,||\, \frac{(R_S + r_d)}{(1+\mu)} \tag{8.52}$$

Thus, R_i' in Fig. 8.16(b) is:

$$R_i' = \frac{(R_S + r_d)}{(1+\mu)} \tag{8.53}$$

Output impedance R_0

Setting $v_i = 0$ in Fig. 8.15(b) makes $v_{gs} = 0$. Thus, the voltage source $\mu v_{gs} = 0$ and r_d comes in parallel with R_D.

Therefore, $$R_0 = r_d \,||\, R_D \tag{8.54a}$$

If $r_d \geq 10\, R_D$,

Then

$$R_0 \cong R_D \tag{8.54b}$$

EXAMPLE 8.5

A common gate JFET amplifier is shown in Fig. 8.16. Determine A_V, R_i, R_0 if the operating point is given as I_{DQ} = 1.2 mA, V_{GSQ} = –1.8 V and r_d = 40 kΩ.

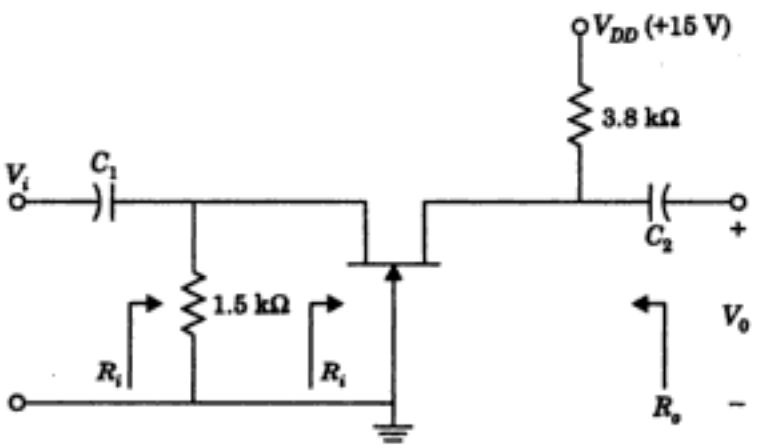


Fig. 8.16 Circuit for Example 8.5.

Solution: Given,

$$V_{GSQ} = -1.8 \text{ V}$$
$$I_{DQ} = 1.2 \text{ mA}$$

$$g_{mo} = \frac{2I_{DSS}}{|V_p|} \quad \text{[From Eq. (8.13)]}$$

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A very popular biasing arrangement used with enhancement MOSFET is the drain feedback configuration shown in Fig. 8.17(a).

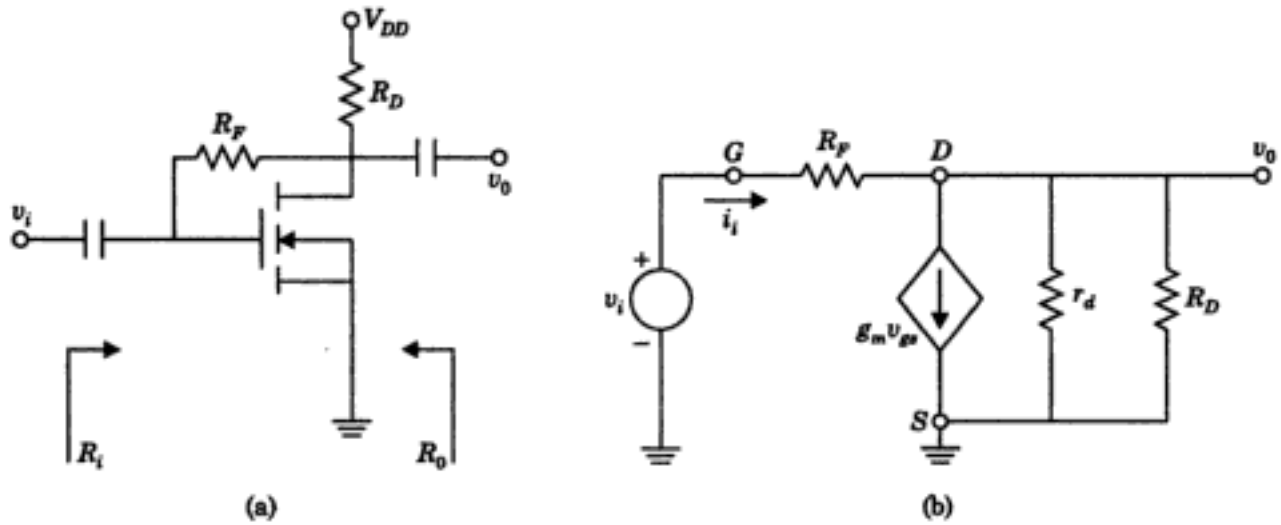


Fig. 8.17 (a) An enhancement MOSFET amplifier, (b) ac equivalent circuit.

The ac equivalent circuit is shown in Fig. 8.17(b) where the E-MOSFET has been replaced by its current source equivalent model.

Applying KCL at node D gives

$$i_i = g_m v_{gs} + \frac{v_0}{r_d \,\|\, R_D} \tag{8.56}$$

Also
$$v_{gs} = v_i \tag{8.57}$$

and
$$i_i = \frac{v_i - v_0}{R_F} \tag{8.58}$$

Solving for $A_V = v_0/v_i$, we get

$$A_V = \frac{v_0}{v_i} = \frac{\left[\frac{1}{R_F} - g_m\right]}{\frac{1}{r_d \,\|\, R_D} + \frac{1}{R_F}} = \frac{\frac{1}{R_F} - g_m}{\frac{1}{R_F \,\|\, r_d \,\|\, R_D}} \tag{8.59}$$

Since R_F is usually large (~ 10 mΩ), therefore,

$$g_m >> \frac{1}{R_F}$$

Thus, the voltage gain from Eq. (8.59) may be written as:

$$A_V = -g_m(R_F \;\|\; r_d \;\|\; R_D) \tag{8.60}$$

Solving Eqs. (8.56), (8.57), (8.58) and simplifying, we get an expression for the input impedance as

$$R_i = \frac{v_i}{i_i} = \frac{R_F + r_d \,\|\, R_D}{1 + g_m(r_d \,\|\, R_D)} \tag{8.61}$$

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8.5 THE MOSFET AS A RESISTANCE

A very important advantages of the MOSFET is that it can be used as a capacitor or a resistor and as well as an active element. The use of an enhancement NMOS transistor connected as a resistance is shown in Fig. 8.19(a).

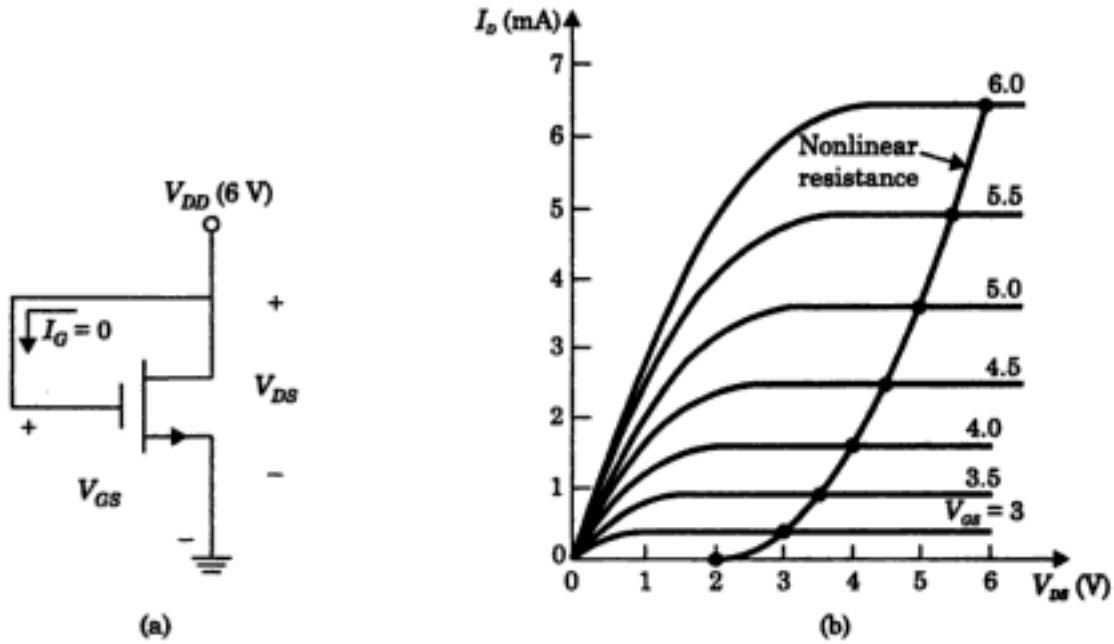


Fig. 8.19 (a) An enhancement NMOS connected as a resistor, (b) The nonlinear resistance characteristics shown on the output characteristics.

As gate is connected to drain terminal, $V_{GS} = V_{DS}$. The locus of points for which $V_{GS} = V_{DS}$ is plotted on the output characteristics of the enhancement type NMOS in Fig. 8.19(b). It is clear that the MOSFET is operating as a nonlinear resistance. An important application where MOSFET is used as a resistor and switch is a MOSFET inverter circuit. A MOSFET inverter is a basic building block used to realize digital circuits. A complete VLSI system can be fabricated by using MOSFET transistors only.

8.6 THE MOSFET INVERTER

Figure 8.20 shows an NMOS inverter which has two enhancement NMOS transistors where Q_1 is the driver (or switch) and Q_2 acts as the load resistor.

In order to show that the circuit of Fig. 8.20 works as an inverter, we first plot the transfer characteristics between out voltage, v_o and input voltage v_i. This is obtained by first plotting the load line using the nonlinear resistance characteristics of transistor Q_2.

Writing KVL for the drain loop in Fig. 8.20,

$$V_{DS1} + V_{DS2} = V_{DD} \tag{8.65}$$

or

$$V_{DS1} = V_{DD} - V_{DS2} \tag{8.66}$$

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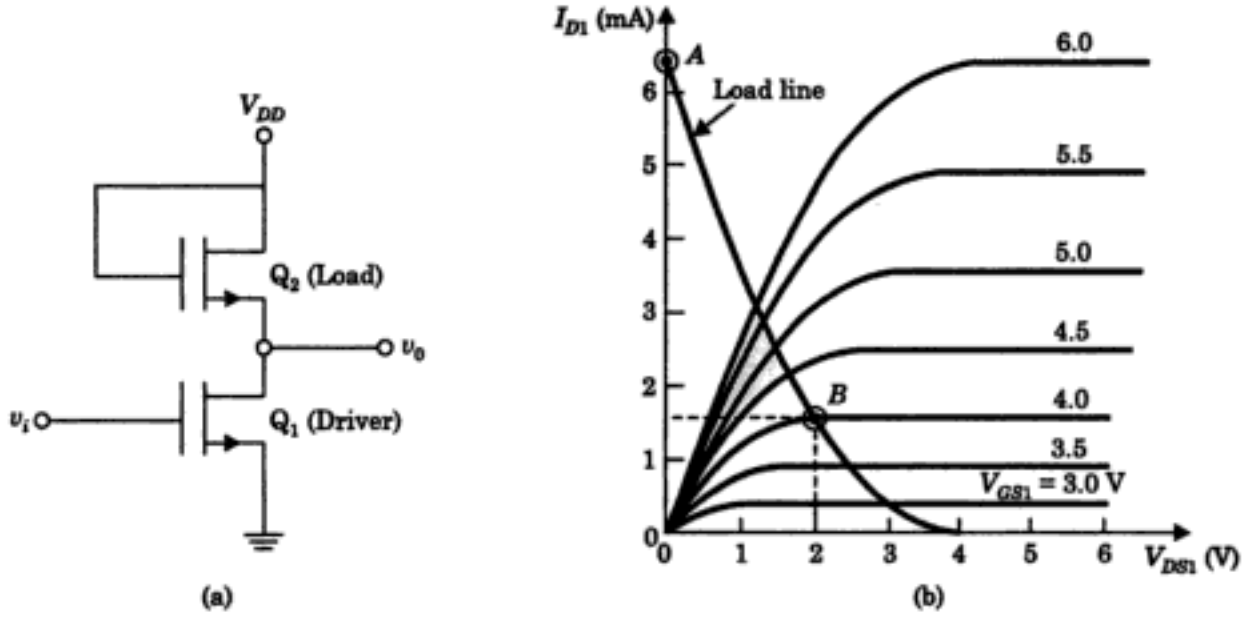


Fig. 8.20 (a) NMOS inverter circuit, (b) NMOS output characteristics showing load line.

Also, since $I_G = 0$ for both Q_1 and Q_2,

$$I_{D1} = I_{D2} \tag{8.67}$$

The load line is a plot of I_{D2} versus V_{DS2} as transistor Q_2 is acting as a load in the inverter circuit. The various points for plotting the load line are obtained from Fig. 8.19(b), where the nonlinear resistance characteristics for the transistor Q_2 acting as a load are shown.

For example, in Fig. 8.19(b),

$$I_{D2} = 6.5 \text{ mA}; \quad V_{GS2} = V_{DS2} = 6 \text{ V} \qquad \text{[since gate is tied to drain]}$$

Now, using Eq. (8.66),

$$\begin{aligned} V_{DS1} &= V_{DD} - V_{DS2} \\ &= 6 - 6 \\ &= 0 \text{ V} \end{aligned}$$

and $$I_{D1} = I_{D2} = 6.5 \text{ mA}$$

Thus, we obtain one point: $I_{DS1} = 6.5$ mA, $V_{DS1} = 0$ V of the load line and is shown as Point A on the output characteristics of transistor Q_1 (drawn between V_{DS1} and I_{DS1}) shown in Fig. 8.20(b).

Similarly for $I_{D2} = 1.5$ mA, $V_{GS2} = V_{DS2} = 4$ V

Thus, $$\begin{aligned} V_{DS1} &= 6 - 4 \\ &= 2 \text{ V} \end{aligned}$$

and $$I_{D1} = I_{D2} = 1.5 \text{ mA}$$

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This point (2 V, 1.5 mA) of the load line is shown as Point B in Fig. 8.20(b). Thus, for various values of I_{D2}, V_{GS2}, one can obtain the corresponding values of V_{DS1} and I_{DS1} and the load line is obtained as shown in Fig. 8.20(b).

The transfer characteristics is now obtained from the various points of intersection of the load line with the output characteristics, i.e., values of V_{DS1} (output v_o) as a function of V_{GS1} (input v_i) and is shown in Fig. 8.21. It is seen that

For $v_i = V_{GS1} \leq V_T$ (2 V)

$I_{D1} = 0$ and $V_{DS1} = 4$ V

For $v_i = 5$ V, $V_{DS1} = 1.5$ V

Thus, the circuit is indeed working as an inverter.

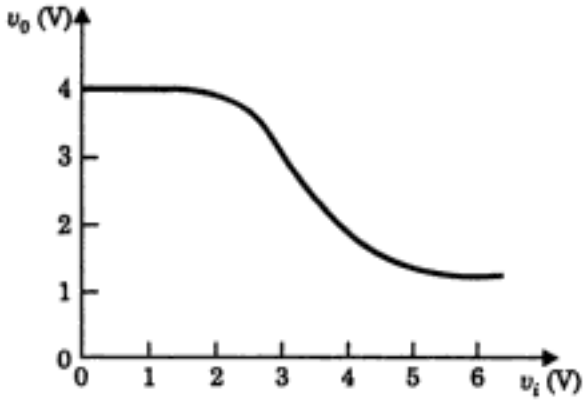


Fig. 8.21 Voltage transistor characteristics (v_o vs. v_i) for the inverter circuit shown in Fig. 8.20(a).

8.7 MOSFET AS A SWITCH

The MOSFET inverter circuit shown in Fig. 8.20(a) behaves as a switch. Consider a step voltage shown in Fig. 8.22(a) applied as input to the inverter circuit.

For $t < T$, the input voltage is 1.5 V. From the transfer characteristics shown in Fig. 8.21, we find that $v_0 = 4$ V. The current I_{D1} in the circuit is zero as can be seen from the load line. The circuit, therefore, is working as an "open switch" as output voltage is high and current is zero.

For $t > T$, the input voltage is 5 V. The output voltage v_0 now is 1.5 V and $I_{D1} = 2.4$ mA [Fig. 8.20(b)]. Thus, the circuit is behaving as a "closed switch" as the appreciable current exists with low output voltage (between D and S).

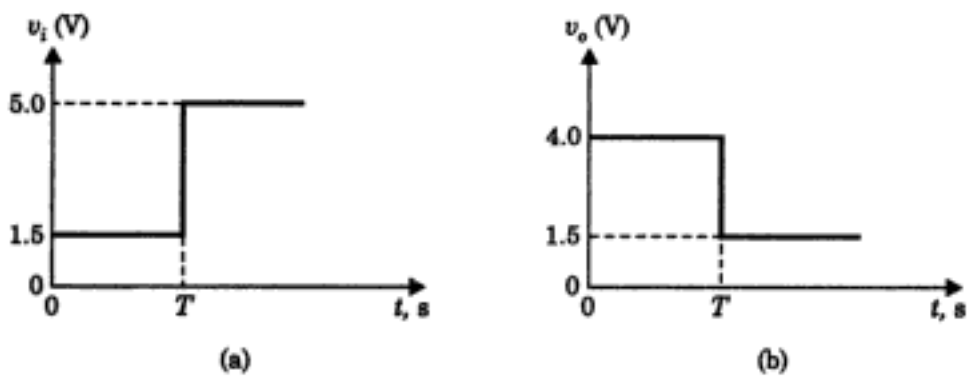


Fig. 8.22 (a) Input step voltage applied to inverter circuit of Fig. 8.20(a), (b) Output waveform.

SUMMARY

- An FET is a voltage controlled current source device compared to BJT which is a current controlled current source device.
- The three important parameters of an FET are: g_m (transconductance) r_d (drain resistance) and μ (amplification factor).

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- The low frequency small signal model of an FET/MOSFET contains a current source $g_m v_{gs}$ and drain resistance r_d connected between drain and source.
- The value of transconductance g_m is computed graphically from the transfer characteristics of FET using the definition:

$$g_m = \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_{V_{DSQ}}$$

- The transconductance g_m can be computed analytically from the relation:

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_p}\right)$$

where $$g_{mo} = g_m|_{V_{GS}=0} = \frac{2I_{DSS}}{|V_p|}$$

- The transconductance g_m for an enhancement MOSFET is given by the equation:

$$g_m = 2k(V_{GSQ} - V_T)$$

where k is determined from a typical operating point.

- The parameter r_d (drain/output resistance) can be computed from the drain characteristics using the definition:

$$r_d = \left.\frac{\Delta v_{DS}}{\Delta i_D}\right|_{V_{GSQ}}$$

- The product of g_m and r_d is equal to the amplification factor μ of FET ($\mu = g_m r_d$).
- The important quantities of interest in an FET amplifier are: input impedance R_i, output impedance R_0 and voltage gain A_V. The current gain in FET is of no significance as the input gate current is always zero due to the high input impedance of FET.
- An FET amplifier may be used in three configurations: common source (CS), common drain (CD) and common gate (CG).
- A CS FET amplifier provides high voltage gain and high input impedance.
- A CD FET amplifier (or source follower) has voltage gain less than unity, a high input impedance and low output impedance.
- A common gate (CG) FET amplifier has low input impedance, high output impedance and moderate voltage gain.
- A MOSFET can be used as a nonlinear resistance by connecting gate to drain terminal.
- A MOSFET inverter forms the basic building block to realize various digital circuits.
- A MOSFET inverter also works as a switch.

REVIEW QUESTIONS

8.1 Draw the small signal model of an FET and explain the significance of each element.

8.2 Define r_d, g_m and μ. Derive a relationship between them.

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P8.12 The circuit shown in Fig. 8.26 uses a depletion MOSFET. Given: I_{DSS} = 12 mA, V_p = –3.5 V and r_d = 25 kΩ. Determine R_i, R_o, A_v.

(***Ans.*** 10 MΩ, 1.68 kΩ, –9.07)

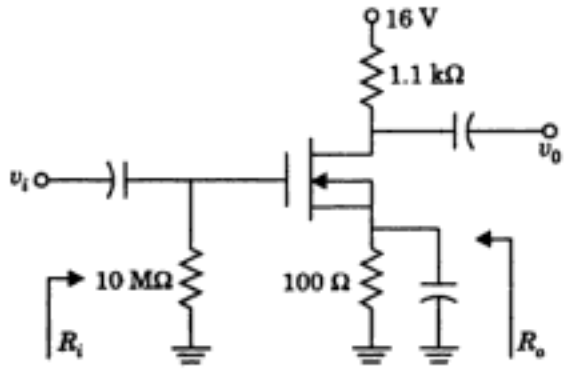


Fig. 8.26 Circuit for P8.12.

P8.13 Determine V_0 if V_i = 4 mV in the circuit shown in Fig. 8.27. Given: r_d = 30 kΩ, g_m = 6 mS.

(***Ans.*** –132.96 mV)

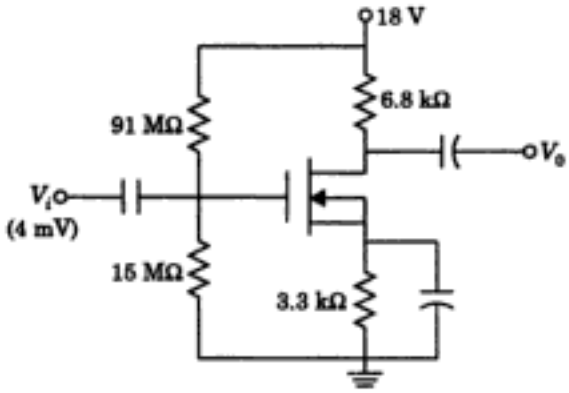


Fig. 8.27 Circuit for P8.13.

P8.14 An *n*-channel E-MOSFET is used in a CS amplifier with voltage divider biasing as shown in Fig. 8.28. The following data is given: r_d = 40 kΩ; k = 0.4 × 10^{-3}, V_{GSQ} = 8V, V_T = 3 V. Find v_o if v_i = 0.8 mV.

(***Ans.*** –9.7 mV)

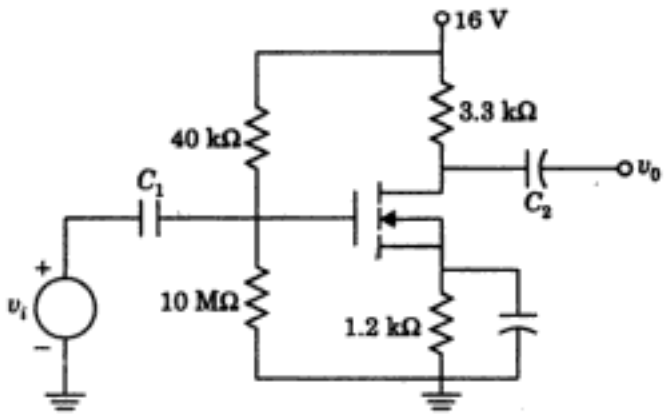


Fig. 8.28 Circuit for P8.14.

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CHAPTER 9 Multistage Amplifiers

9.1 INTRODUCTION

In most practical electronic circuits/systems, the amplification provided by a single stage of amplifier is not sufficient. As was seen, the voltage gain of a single stage amplifier depends upon its load resistance R_C which can not be increased beyond a limit due to constraints imposed by dc biasing. Thus, there is a limit to the voltage gain that can be obtained from a single stage amplifier. Besides this, the input and output impedances of a single stage amplifier may not be suitable for the electronic circuit where it is being used. These problems are taken care of by connecting two or more amplifier stages in cascade to achieve larger voltage or current gain or suitable input and output impedances. Thus, if it is desired to have a high voltage gain, then CE stages are cascaded. If high input impedance is required along with voltage gain, then first stage can be CC followed by CE stages. Such circuits are called **cascaded** or **multistage amplifiers.** Special cascaded circuits namely a darlington pair and cascode amplifier are also discussed. The device used can be BJT or FET. Here, more emphasis is on BJT circuits.

The output of the first stage is applied as input to the next stage usually through a coupling device. Various types of coupling methods are available, however, RC coupling is the most commonly used coupling method at audio range of frequencies and is discussed in detail. A differential amplifier, the basic building block of analog ICs (741 Op-amp) is a two-stage amplifier and has been discussed. The analysis can be done by using any of the three small signal transistor models. We have chosen hybrid-π model here as it is simple and more practical.

9.2 CASCADED BJT AMPLIFIERS AT LOW FREQUENCIES

Figure 9.1 shows a two-stage cascaded amplifier in which the output of the first stage is connected as input to the next stage. The output of the second (or last) stage is connected to the load resistance R_L. The analysis of cascaded amplifiers for finding the overall voltage gain, current gain and input and output impedances can be done in various ways. A very

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simple way of analysis is by taking the Thevenin's equivalent of the first stage at terminals 1-1′ as shown in Fig. 9.2.

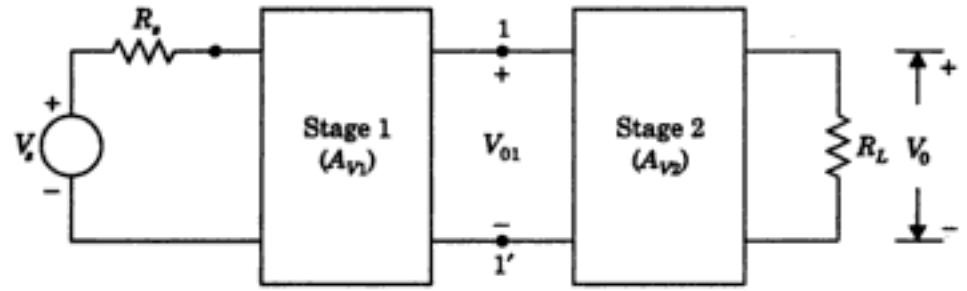


Fig. 9.1 A two-stage cascaded amplifier.

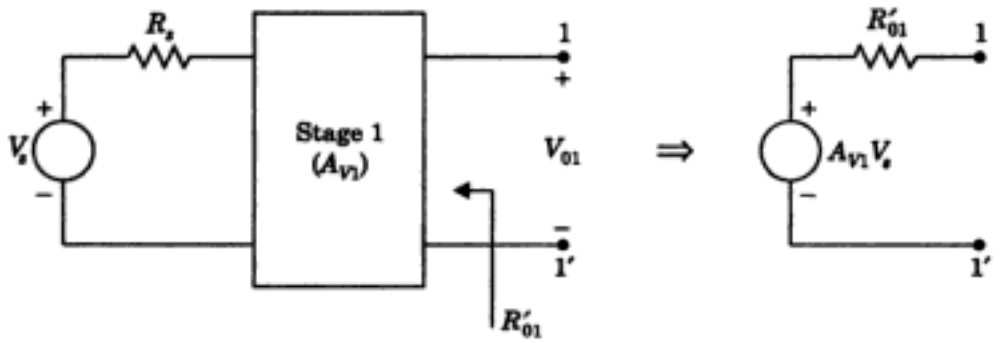


Fig. 9.2 Thevenin's equivalent of the 1st stage at 1-1′.

Thus, the first stage is represented by Thevenin's voltage source $A_{V1}V_s$ and output resistance R'_{01} at terminals 1 and 1′. The second stage is driven by the Thevenin's equivalent of the first stage as shown in Fig. 9.3. It can be seen that the source resistance of stage 2 is R'_{01}.

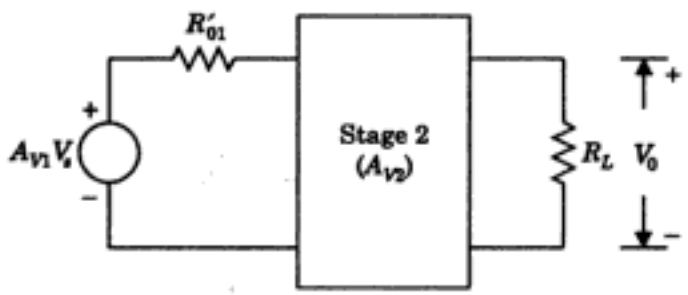


Fig. 9.3 Equivalent circuit representation of second stage.

The output voltage V_0 of the second stage from Fig. 9.3 is

$$V_0 = A_{V2} \times A_{V1} V_s \tag{9.1}$$

The overall voltage gain of the two-stage amplifier; therefore is

$$A_V = \frac{V_o}{V_s} = A_{V1} \times A_{V2}$$

The analysis is performed at the range of frequencies at which the various capacitors, that is coupling, by-pass and internal junction capacitances can be neglected.

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EXAMPLE 9.1

A two-stage amplifier shown in Fig. 9.4 is in CE–CC configuration. The transistor parameters are given as $\beta_0 = 100$ and $r_\pi = 0.5$ kΩ. Determine the overall voltage gain and current gain. Assume $r_0 = \infty$.

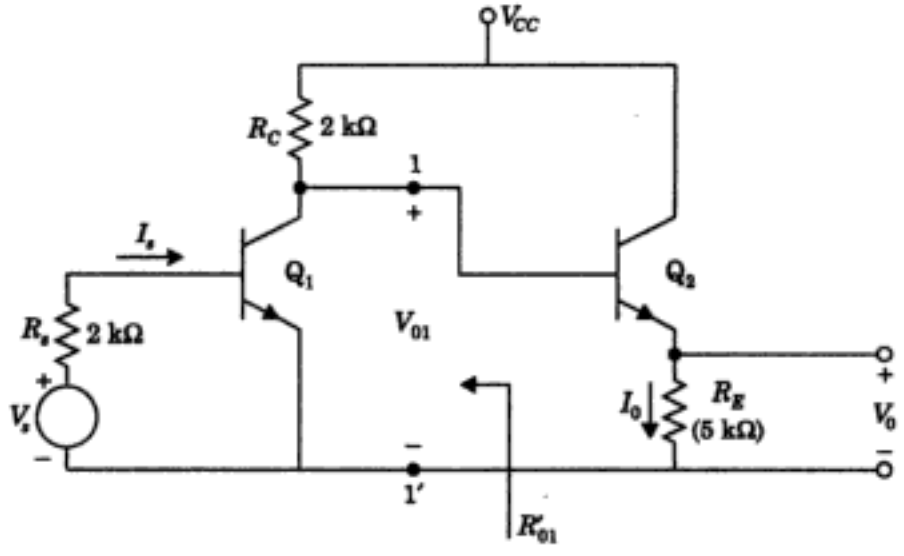


Fig. 9.4 Circuit for Example 9.1.

Solution: The Thevenin's equivalent of the unloaded first stage at terminals 1-1′ is shown in Fig. 9.5. As the first stage is a CE amplifier stage, its voltage gain A_{V1} is given as:

$$A_{V1} = \frac{V_{01}}{V_s} = \frac{-\beta_0 R_C}{R_s + r_\pi}$$

$$= \frac{-100 \times 2}{2 + 0.5}$$

$$= -80$$

The value of $R'_{01} = R_C = 2$ kΩ. Thus, the second stage can be shown as in Fig. 9.6. Note that R_s for the second stage is R'_{01} only. The second stage is a CC amplifier and its voltage gain is given as:

$$A_{V2} = \frac{(1 + \beta_0) R_E}{R_s + r_\pi + (1 + \beta_0) R_E}$$

$$= \frac{(1 + 100)\,5}{2 + 0.5 + (1 + 100)\,5}$$

$$= 0.995$$

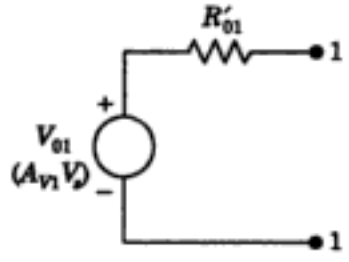


Fig. 9.5 Thevenin's equivalent of first stage at 1-1′.

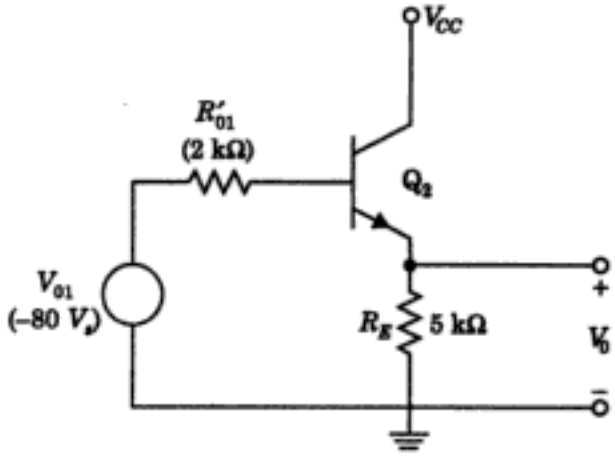


Fig. 9.6 Equivalent circuit representation of second stage.

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The overall voltage gain is:

$$A_V = A_{V1}A_{V2}$$
$$= (-80)(0.995) = -79.6$$

As, $$I_0 = \frac{V_0}{R_E}$$

and $$I_s = \frac{V_s}{R_s}$$

Therefore, the overall current gain is

$$A_I = \frac{I_o}{I_s} = \frac{R_s}{R_L} A_V$$
$$= \frac{2}{5}(-79.6) = -31.84$$

EXAMPLE 9.2

Calculate the overall voltage gain, current gain, input impedance and output impedance for the two-stage amplifier shown in Fig. 9.7. Assume $\beta_0 = 100$. All capacitors are high.

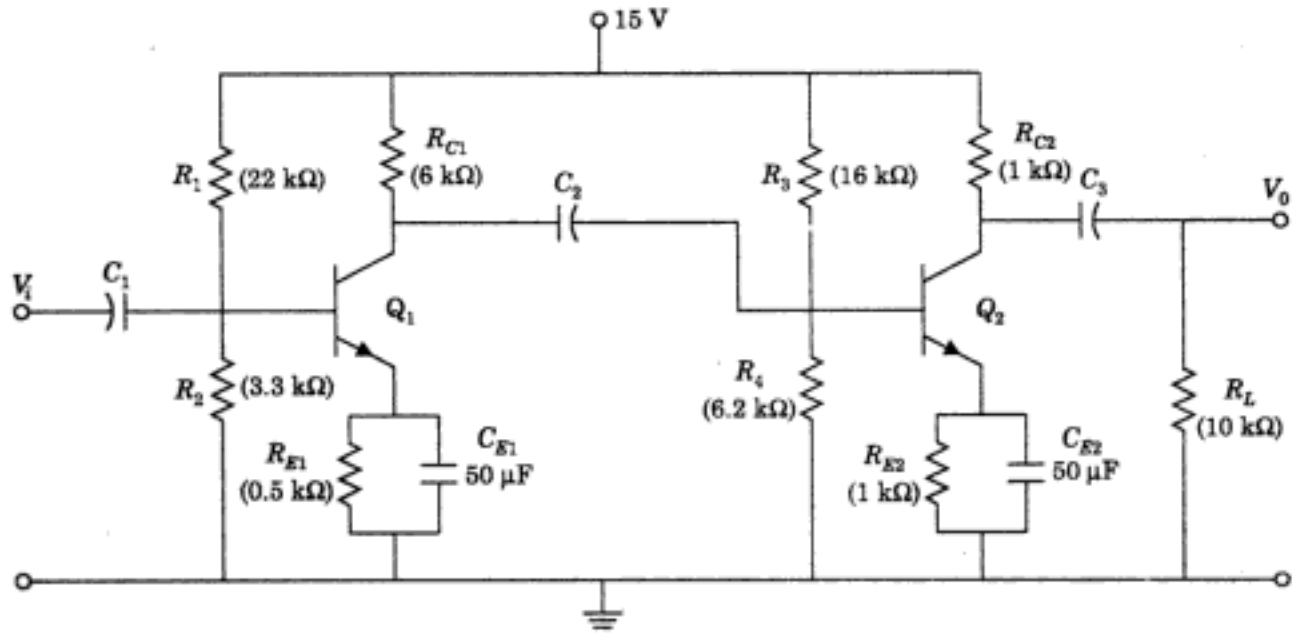


Fig. 9.7 Circuit diagram for Example 9.2.

Solution: It can be seen that the circuit is a two-stage CE-CE amplifier with self-bias arrangement. In the given data, the value of r_π for the transistors is not provided. So, as a first step, we perform the dc analysis to evaluate the quiescent currents I_{C1} and I_{C2} so as to find $r_{\pi 1}$ and $r_{\pi 2}$ respectively. It can be seen that the biasing for both the stages are different, therefore, $r_{\pi 1}$ and $r_{\pi 2}$ will also be different.

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DC analysis

Under dc conditions, all the capacitors are open circuited as their reactance given by $X_C = 1/\omega C$ will be infinite.

The simplified dc equivalent circuit for stage 1 is shown in Fig. 9.8(a), where

$$R_{B1} = R_1 \parallel R_2$$
$$= 22\ \text{k}\Omega \parallel 3.3\ \text{k}\Omega$$
$$= 2.86\ \text{k}\Omega$$

and
$$V_{BB1} = \frac{3.3 \times 15}{22 + 3.3}$$
$$= 1.95\ \text{V}$$

$$I_{B1} = \frac{V_{BB1} - V_{BE}}{R_{B1} + (1+\beta)R_{E1}}$$
$$= \frac{1.95 - 0.7}{2.86 + 101 \times 0.5}$$
$$= 0.023\ \text{mA}$$

Therefore,
$$I_{C1} = \beta I_{B1}$$
$$= 100 \times 0.023$$
$$= 2.3\ \text{mA}$$

and
$$g_{m1} = \frac{I_{C1}}{V_T}$$
$$= \frac{2.3}{25} = 0.092\ \text{℧} \qquad \text{(assuming } V_T = 25\ \text{mV)}$$

$$r_{\pi 1} = \frac{\beta}{g_{m1}}$$
$$= \frac{100}{0.092} = 1.08\ \text{k}\Omega$$

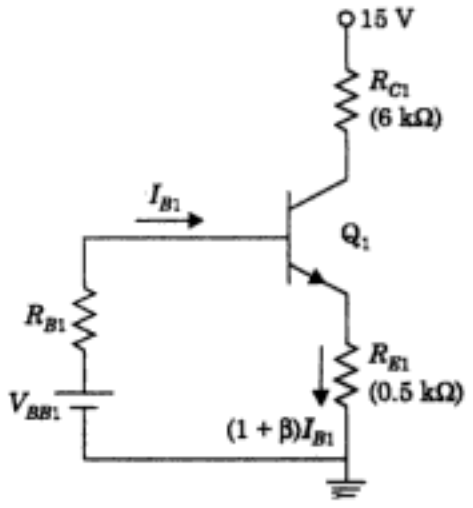


Fig. 9.8(a) Simplified dc equivalent circuit for stage 1.

The value of $r_{\pi 2}$ for stage 2 is obtained from the simplified dc equivalent circuit shown in Fig. 9.8(b).

Here,
$$R_{B2} = R_3 \| R_4$$
$$= 16\ \text{k}\Omega \| 6.2\ \text{k}\Omega$$
$$= 4.46\ \text{k}\Omega$$

and
$$V_{BB2} = \frac{6.2 \times 15}{16 + 6.2}$$
$$= 4.18\ \text{V}$$

$$I_{B2} = \frac{V_{BB2} - V_{BE}}{R_{B2} + (1+\beta)R_{E2}}$$

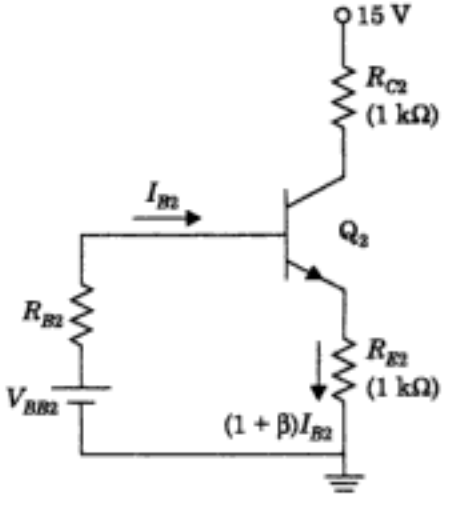


Fig. 9.8(b) Simplified dc equivalent circuit for 9.8(b).

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$$= \frac{4.18 - 0.7}{4.46 + 101 \times 1} = 0.032 \text{ mA}$$

$$I_{C2} = \beta I_{B2}$$

$$= 100 \times 0.032 = 3.2 \text{ mA}$$

$$g_{m2} = \frac{I_{C2}}{V_T} = \frac{3.2}{25} = 0.128 \text{ ℧}$$

$$r_{\pi 2} = \frac{\beta}{g_m} = \frac{100}{0.128} = 781.25 \, \Omega$$

AC analysis

Under ac conditions, all the capacitors are short circuit. The ac equivalent circuit is shown in Fig. 9.9.

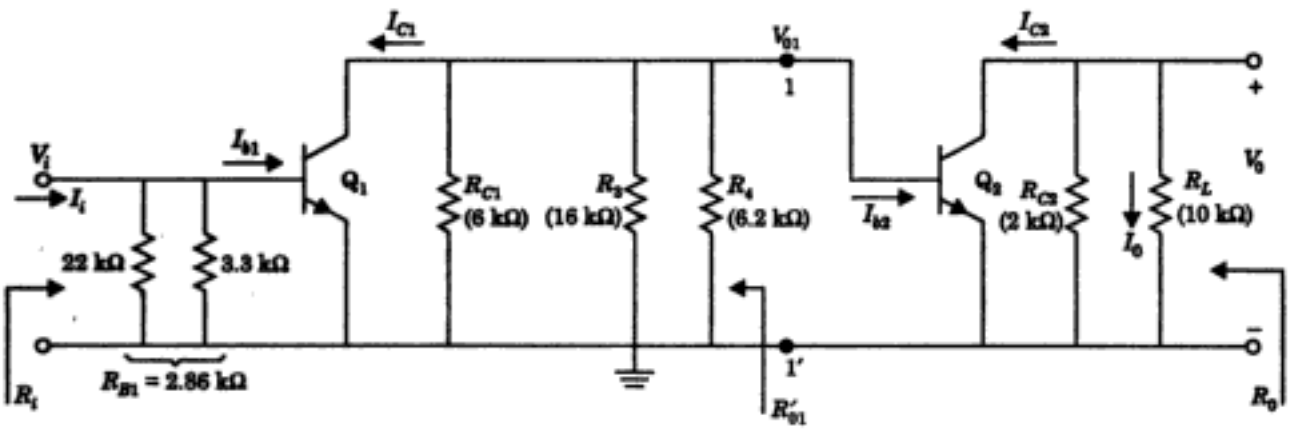


Fig. 9.9 ac equivalent circuit for the circuit shown in Fig. 9.7.

First obtain the Thevenin's equivalent of stage 1 at 1-1′, as shown in Fig. 9.10(a).

Effective load R_{L1} for first stage = $R_{C1} \parallel R_3 \parallel R_4$

So $R_{L1} = 6 \text{ k}\Omega \parallel 16 \text{ k}\Omega \parallel 6.2 \text{ k}\Omega$

$= 2.55 \text{ k}\Omega$

$$\therefore \quad A_{V1} = \frac{V_{01}}{V_i} = -\frac{\beta R_{L1}}{r_{\pi 1}} \qquad [\text{As } R_{S1} = 0]$$

$$= -\frac{100 \times 2.55}{1.08} = -236.1$$

and $R'_{o1} = R_{C1} \parallel R_3 \parallel R_4$

$= 2.55 \text{ k}\Omega$

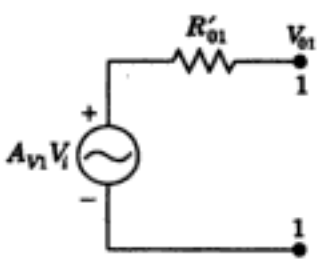


Fig. 9.10(a) Thevenin's equivalent of stage-1 at 1-1′.

Using the Thevenin's equivalent of first stage, the equivalent circuit of second stage is shown in Fig. 9.10(b).

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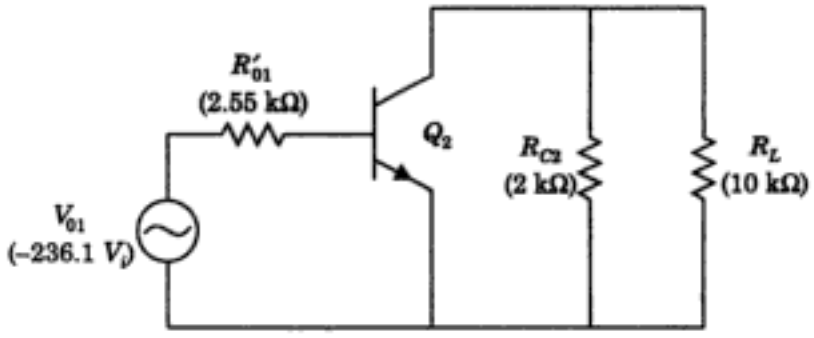


Fig. 9.10(b) Thevenin's equivalent of stage 2.

Now, the effective load for the second stage is:

$$R_{L2} = R_{C2} \| R_L$$
$$= 2\ \text{k}\Omega \| 10\ \text{k}\Omega$$
$$= 1.67\ \text{k}\Omega$$

Now
$$A_{V2} = \frac{-\beta_0 R_{L2}}{R_s + r_{\pi 2}}$$
$$= \frac{-100 \times 1.67\ \text{k}\Omega}{2.55\ \text{k}\Omega + 781.25\ \text{k}\Omega} = -50$$

Thus, the overall voltage gain is

$$A_V = \frac{V_0}{V_i} = \frac{V_0}{V_{01}} \times \frac{V_{01}}{V_i}$$
$$= A_{V1} A_{V2}$$
$$= (-236.1)(-50) = 11805$$

Note that the overall voltage gain is positive due to 180° phase shift provided by each of CE stages.

The overall current gain is:

$$A_I = \frac{I_0}{I_i}$$
$$= \frac{I_0}{I_{c2}} \times \frac{I_{c2}}{I_{b2}} \times \frac{I_{b2}}{I_{c1}} \times \frac{I_{c1}}{I_{b1}} \times \frac{I_{b1}}{I_i}$$

Here I_0/I_{c2} is obtained by the current divider rule and is given by

$$\frac{I_0}{I_{c2}} = -\frac{R_{C2}}{R_{C2} + R_L} = -\frac{2}{2+10} = -0.166$$

$$\frac{I_{c2}}{I_{b2}} = -\beta_0 = -100$$

and I_{b2}/I_{c1} is computed from the simplified diagram shown in Fig. 9.11.

$$\frac{I_{b2}}{I_{c1}} = -\frac{R_{L1}}{R_{L1} + r_{\pi 2}}$$

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Solution: Since $I_{CQ_1} = I_{CQ_2} = 100\,\mu A$, therefore,

$$g_m = \frac{I_{CQ}}{25} = \frac{100}{25} = 4\ \text{m℧}$$

$$r_o = \frac{V_A}{I_{CQ}} = \frac{130}{0.1} = 1.3\ \text{MΩ}$$

and

$$r_\pi = \frac{\beta}{g_m} = \frac{150}{4} = 37.5\ \text{kΩ}$$

The circuit is a CC-CE cascade. The ac equivalent circuit of the first CC stage using hybrid-π model is shown in Fig. 9.13(a) for calculating its voltage gain. Note that the load for the CC amplifier stage is r_{o1} = 1.3 MΩ. Thus, $R_E = r_{01}$ = 1.3 MΩ. The various formulae in the analysis have been taken from Table 6.6, Chapter 6.

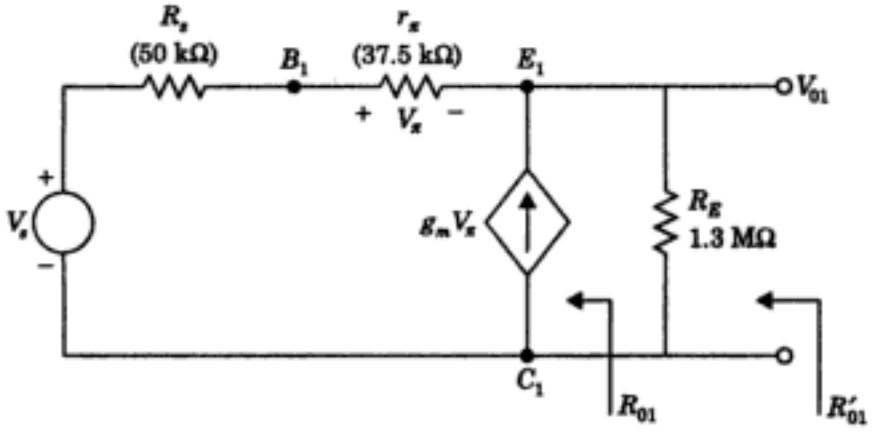


Fig. 9.13(a) ac equivalent circuit for CC stage using hybrid-π model.

The voltage gain of CC stage is:

$$A_{V1} = \frac{V_{01}}{V_s} = \frac{(1+\beta_0)R_E}{R_s + r_\pi + (1+\beta_0)R_E}$$

$$= \frac{(1+150)1300}{50 + 37.5 + (+150)1300}$$

$$= 0.999$$

and

$$R_{o1} = \frac{R_s + r_\pi}{1+\beta_0}$$

$$= \frac{50 + 37.5}{1+150}$$

$$= 0.579\ \text{kΩ}$$

So R'_{o1} = 1300 kΩ || 0.579 kΩ

= 0.579 kΩ

Thus, the second stage can be represented as shown in Fig. 9.13(b)

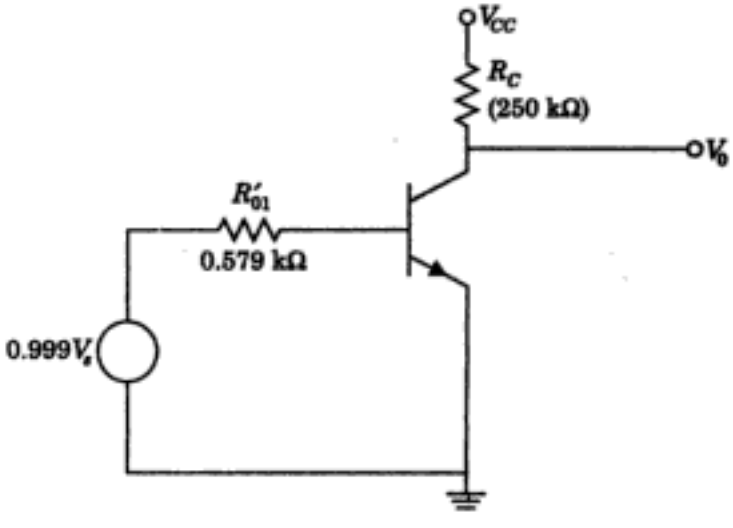


Fig. 9.13(b) Equivalent representation of stage 2 (CE amplifier).

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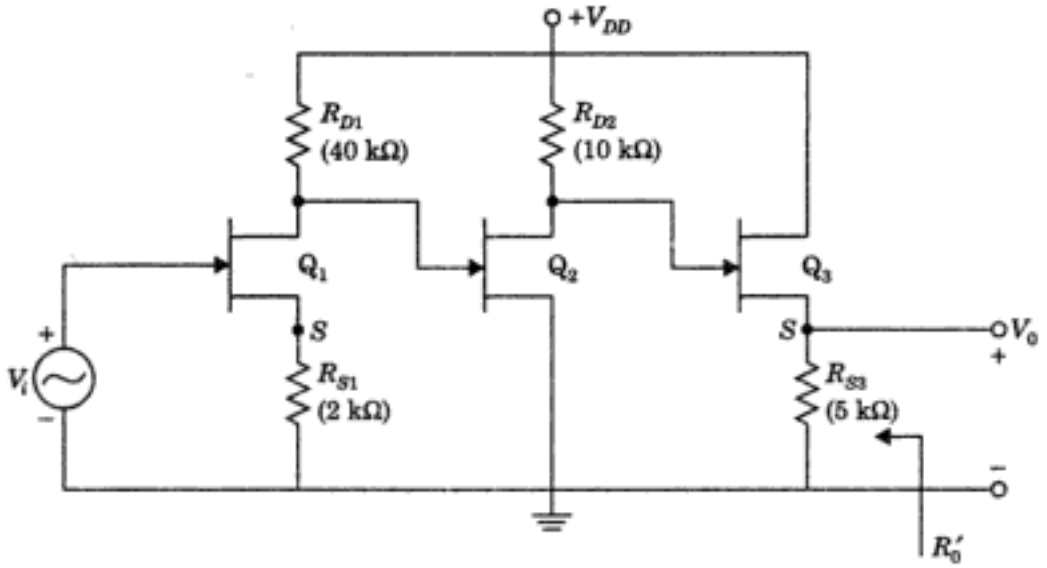


Fig. 9.14(b) Circuit diagram for Example 9.4.

Solution: The circuit is a three-stage amplifier where first stage is common source (CS) with R_S, second stage is CS and third stage is CD amplifier. Using the results derived in Chapter 8.

(i)
$$A_{V1} = \frac{-\mu R_{D1}}{r_d + R_{D1} + (1+\mu)R_{S1}} \quad \text{(CS amplifier with } R_{S1}\text{)}$$

$$= \frac{-40 \times 40}{40 + 40 + (1+40)\,2}$$

$$= -9.88$$

$$A_{V2} = \frac{-\mu R_{D2}}{r_d + R_{D2}} \quad \text{(CS amplifier stage)}$$

$$= \frac{-40 \times 10}{40 + 10} = -8$$

$$A_{V3} = \frac{\mu R_{S3}}{r_d + (1+\mu)R_{S3}} \quad \text{(CD amplifier stage)}$$

$$= \frac{40 \times 5}{40 + (1+40)\,5} = 0.816$$

Therefore,
$$A_{V(\text{overall})} = \frac{V_0}{V_i}$$

$$= A_{V1} \times A_{V2} \times A_{V3}$$

$$= (-9.88)(-8)(0.816)$$

$$= 64.5$$

(ii) The last stage is a CD amplifier and its output impedance R_0 without taking load resistance R_{S3} into account is given by

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Current gain

Since
$$I_0 = I_b + \beta_D I_b \tag{9.9}$$
$$= (1 + \beta_D) I_b$$

Therefore,
$$\frac{I_0}{I_b} = (1 + \beta_D) \tag{9.10}$$

and overall current gain is:

$$A_I = \frac{I_0}{I_i} = \frac{I_0}{I_b} \cdot \frac{I_b}{I_i} \tag{9.11}$$

where
$$\frac{I_b}{I_i} = \frac{R_B}{R_B + R_i} = \frac{R_B}{R_B + r_i + (1 + \beta_D) R_E} \tag{9.12}$$

So
$$A_I = \frac{(1 + \beta_D) R_B}{R_B + r_i + (1 + \beta_D) R_E} \tag{9.13}$$

$$\simeq \frac{\beta_0 R_B}{R_B + r_i + \beta_D R_E} \tag{9.14}$$

Voltage gain

$$V_0 = I_0 R_E \tag{9.15}$$
$$= (1 + \beta_D) I_b R_E$$
$$V_i = I_b r_i + (1 + \beta_D) I_b R_E \tag{9.16}$$
$$= I_b [r_i + (1 + \beta_D) R_E] \tag{9.17}$$

So
$$A_V = \frac{V_0}{V_i} = \frac{(1 + \beta_D) R_E}{r_i + (1 + \beta_D) R_E} \tag{9.18}$$

$$\simeq 1 \tag{9.19}$$

Output resistance

The output resistance, R_0 is determined by applying a test voltage V_0 at the output and determining the current I_0 (with input V_i set to zero) drawn by the circuit. Solving for I_0 gives

$$I_0 = \frac{V_0}{R_E} + \frac{V_0}{r_i} + \beta_D I_b \tag{9.20}$$

$$= \frac{V_0}{R_E} + \frac{V_0}{r_i} + \beta_D \left(\frac{V_0}{r_i} \right) \tag{9.21}$$

$$= \left(\frac{1}{R_E} + \frac{1}{r_i} + \frac{\beta_D}{r_i} \right) V_0 \tag{9.22}$$

Solving for R_0 gives

$$R_0 = \frac{V_0}{I_0} = \frac{1}{\frac{1}{R_E} + \frac{1}{r_i} + \frac{\beta_D}{r_i}} \tag{9.23}$$

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$$= R_E \| r_i \| \frac{r_i}{\beta_D} \tag{9.24}$$

$$\approx \frac{r_i}{\beta_D} \tag{9.25}$$

EXAMPLE 9.5

A Darlington emitter follower with $R_E = 500\ \Omega$ is driven by a 50 kΩ source. The transistor Q_1 is biased at 15 μA and Q_2 is biased at 1.0 mA. Find A_V, R_i and R_0. Assume: $V_A = 100$ V, $\beta_0 = 150$ for both the transistors.

Solution: The transistor parameters are computed as:

For Q_1:

$$g_{m1} = \frac{I_{c1}}{V_T} = \frac{15}{25} = 0.6\ \text{m℧}$$

$$r_{\pi 1} = \frac{\beta_0}{g_{m1}} = \frac{150}{0.6} = 250\ \text{k}\Omega$$

$$r_{01} = \frac{V_A}{I_{c1}} = \frac{100}{15} = 6.67\ \text{M}\Omega$$

For Q_2:

$$g_{m2} = \frac{I_{c2}}{V_T} = \frac{1}{25} = 4\ \text{m℧}$$

$$r_{\pi 2} = \frac{\beta_0}{g_{m2}} = \frac{150}{4} = 37.5\ \text{k}\Omega$$

$$r_{02} = \frac{V_A}{I_{c2}} = \frac{100}{1} = 1\ \text{M}\Omega$$

The ac equivalent circuit can be shown as in Fig. 9.17 where transistors have been replaced by their hybrid-π model. Note that the load for the first stage is the output resistance r_{01}.

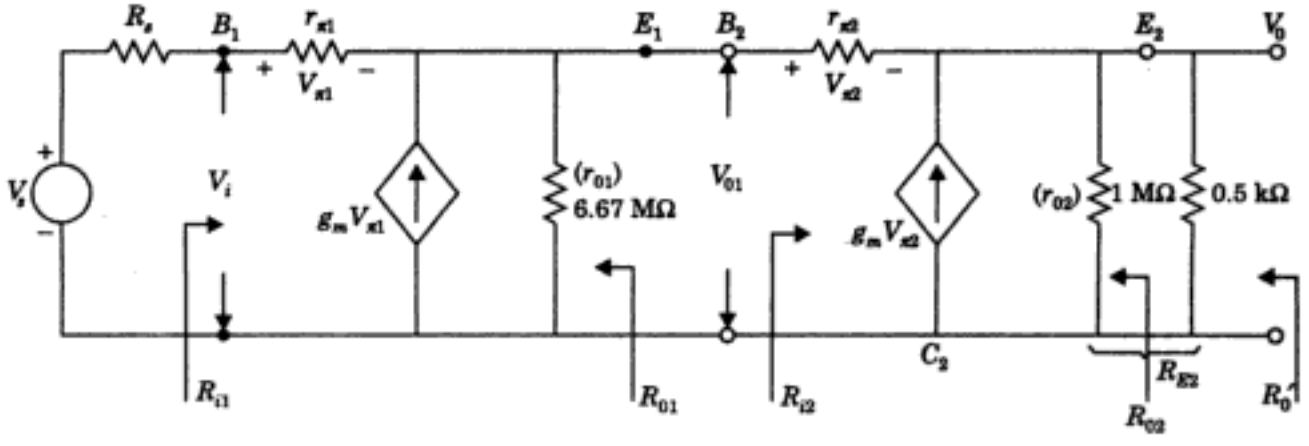


Fig. 9.17 ac equivalent circuit for Example 9.4.

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Effective load for stage Q_2 is:

$$R_{E2} = r_{02} \parallel R_E$$
$$= 1\ \text{M}\Omega \parallel 0.5\ \text{k}\Omega$$
$$= 0.5\ \text{k}\Omega$$

The input resistance for second stage is:

$$R_{i2} = r_{\pi 2} + (1 + \beta_0)R_{E2}$$
$$= 37.5 + (1 + 150)\ 0.5 = 113$$

The voltage gain of the second stage is:

$$A_{V2} = \frac{V_0}{V_{01}} = \frac{(1 + \beta_0)R_{E2}}{R_{i2}}$$
$$= \frac{(1+150)0.5}{113} = 0.668$$

Now, the effective load for the first stage is:

$$R_{E1} = r_{01} \parallel R_{i2}$$
$$= 6.67\ \text{M}\Omega \parallel 113\ \text{k}\Omega$$
$$= 113\ \text{k}\Omega$$

and

$$R_{i1} = r_{\pi 1} + (1 + \beta_0)R_{E1}$$
$$= 250 + (1 + 150)\ 113$$
$$= 17.3\ \text{M}\Omega$$

The voltage gain of the first stage is:

$$A_{V1} = \frac{V_{01}}{V_i} = \frac{(1 + \beta_0)R_{E1}}{R_{i1}}$$
$$= \frac{(1+150)113}{17.3} = 0.986$$

The overall voltage gain is:

$$A_{V_s} = \frac{V_0}{V_{01}} \times \frac{V_{01}}{V_i} \times \frac{V_i}{V_s}$$
$$= A_{V2} \times A_{V1} \times \frac{R_{i1}}{R_s + R_{i1}}$$
$$= (0.668) \times (0.986) \times \frac{17.3}{50 + 17.3}$$
$$= 0.658$$

The output resistance of the first stage is:

$$R_{01} = 6.7\ \text{M}\Omega \parallel \frac{50 + 250}{1 + 150}$$
$$= 1.99\ \text{k}\Omega$$

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$$R_{02} = r_{02} \| \frac{r_{\pi 2} + r_{01}}{1 + \beta_0}$$

$$= 1\,\text{M}\Omega \| \frac{37.5 + 1.99}{1 - 150} = 0.261\,\text{k}\Omega$$

9.2.3 Cascode Amplifier

A cascode configuration consists of a CE stage feeding a CB stage as shown in Fig. 9.18(a) where transistor Q_1 is npn and Q_2 is a pnp transistor. The circuit provides a high voltage gain over a wider range of frequencies and is, therefore, used in video amplifier circuits.

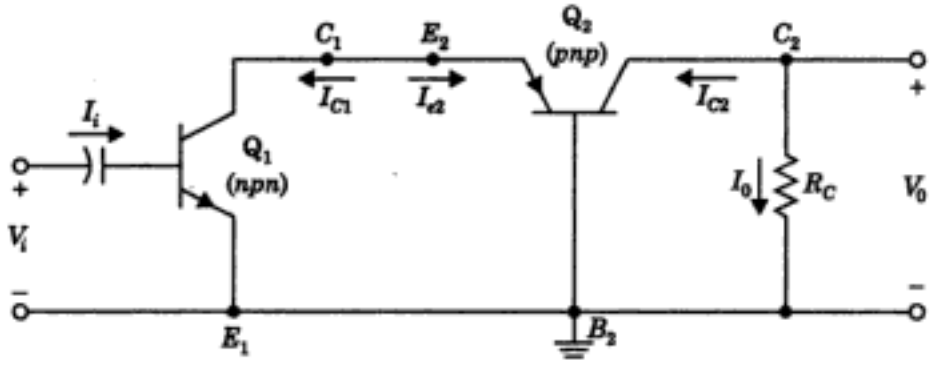


Fig. 9.18(a) Cascode amplifier.

For proper amplifier operation, it is desired that the two transistors be identical. The small signal hybrid-π model is drawn in Fig. 9.18(b), ignoring r_{01} and r_{02}, and assuming $r_{\pi 1} = r_{\pi 2} = r_\pi$ (identical transistors)

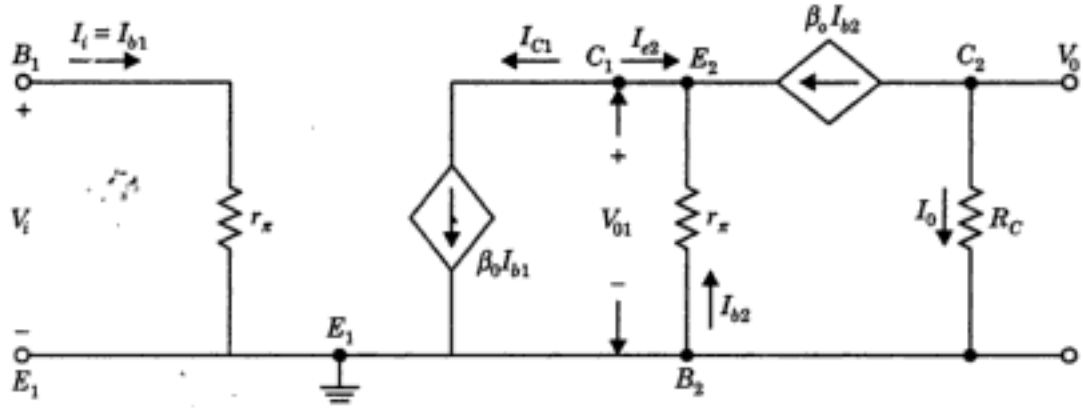


Fig. 9.18(b) ac equivalent circuit.

Current gain

$$A_I = \frac{I_0}{I_i} = \frac{I_0}{I_{c1}} \times \frac{I_{c1}}{I_{b1}} \tag{9.26}$$

Since $I_0 = -\beta_0 I_{b2}$

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and $$I_{c1} = -I_{e2} = -(1 + \beta_0) I_{b2} \tag{9.27}$$

Therefore, $$\frac{I_0}{I_{c1}} = +\frac{\beta_0}{1 + \beta_0} \tag{9.28}$$

Also $$I_{c1} = \beta_0 I_{b1}$$

Therefore, $$\frac{I_{c1}}{I_{b1}} = \beta_0 \tag{9.29}$$

Now, $$A_I = \frac{I_0}{I_i} = -\frac{\beta_0}{1 + \beta_0} \times \beta_0 \tag{9.30}$$

$$\simeq -\beta_0 \tag{9.31}$$

Voltage gain

$$A_V = \frac{V_0}{V_i} = \frac{V_0}{V_{01}} \times \frac{V_{01}}{V_i} \tag{9.32}$$

Since $$V_i = r_\pi I_{b1} \tag{9.33}$$

$$V_{01} = -r_\pi I_{b2} \tag{9.34}$$

Using Eqs. (9.27) and (9.29), we find

$$\frac{I_{b2}}{I_{b1}} = +\frac{\beta_0}{1 + \beta_0}$$

So, the voltage gain of CE stage

$$\frac{V_{01}}{V_i} = -\frac{I_{b2}}{I_{b1}} \simeq -1 \tag{9.35}$$

Note that the quantity V_{01}/V_i gives the voltage gain of the CE amplifier stage and is found to be close to unity. The reason for such a low voltage gain is that the load for the CE stage is the input resistance of the CB stage which is very small (a few tenths of ohms) whatever may be the value of load resistance R_C. This reduction of the effective load resistance of CE stage leads to improvement in the high frequency response of the cascode amplifier. It will be shown in the chapter on "frequency response" that the product (gain × bandwidth) for an amplifier is almost constant. Therefore, the reduction in the voltage gain of the CE stage results in increase of its bandwidth. Further, it may be seen,

$$V_o = I_0 R_C \tag{9.36}$$

$$= -\beta_0 I_{b2} R_C$$

$$= -\beta_0 R_C \left(\frac{-V_{01}}{r_\pi}\right) \quad [\because V_{01} = -r_\pi I_{b2}] \tag{9.37}$$

So $$\frac{V_0}{V_{01}} = \frac{\beta_0 R_C}{r_\pi} \tag{9.38}$$

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Now, the overall voltage gain is:

$$A_V = \frac{V_0}{V_{01}} \times \frac{V_{01}}{V_i} \tag{9.39}$$

$$= \frac{\beta_0 R_C}{r_\pi} \times (-1)$$

$$= -\frac{\beta_0 R_C}{r_\pi} \tag{9.40}$$

A practical cascode amplifier is shown in Fig. 9.19.

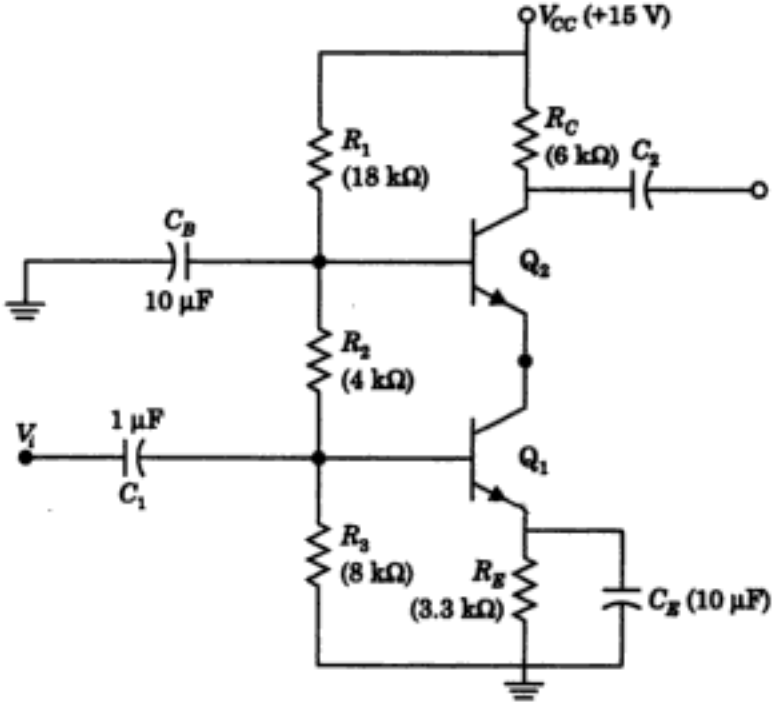


Fig. 9.19 A practical cascode amplifier. Capacitor C_B is large and establishes base of Q_2 at ground for ac signals.

EXAMPLE 9.6

For the component values given in Fig. 9.20, calculate the gain of the cascode circuit. dc analysis performed on the circuit gives $I_{C1} = I_{C2} \simeq 1$ mA and $\beta_0 = 120$.

Solution: The ac equivalent circuit is shown in Fig. 9.20.

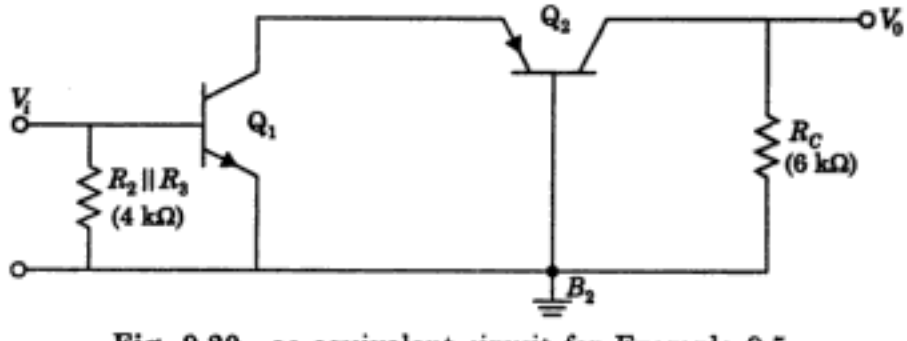


Fig. 9.20 ac equivalent circuit for Example 9.5.

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dc signal available across R_C is blocked and is not permitted to go to the next stage. This ensures that the dc biasing of the next stage is not disturbed by this type of coupling. Further, the value of C_C is usually chosen to be high so that it provides low reactance at the frequencies of interest. Thus, the coupling capacitor C_C blocks dc signals and allows ac signals only to be passed to the next stage. The capacitor C_C is also called a **blocking capacitor** as it blocks dc signals.

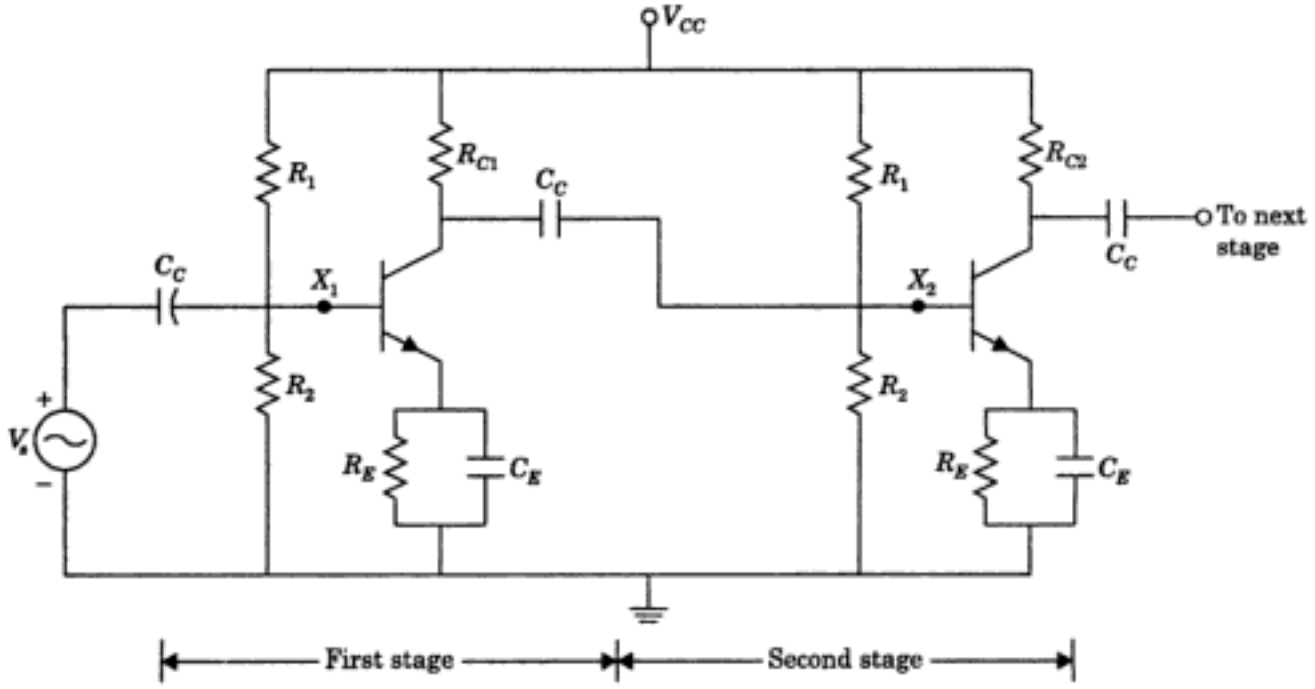


Fig. 9.21 A two-stage RC coupled amplifier.

The resistors R_1, R_2 and R_E provide the necessary biasing and stabilization of the Q-point. The capacitor C_E connected in parallel to R_E short circuits the resistance R_E for ac signals and thereby prevents any loss of ac signal. If C_E is not connected across R_E both, the dc and ac components of the current will flow through R_E. The Q-point will be stabilized, but at the same time the ac voltage gain will get reduced due to negative feedback. The capacitor C_E provides an alternate path for the ac current to flow and is called **bypass capacitor**. The signal source V_s is also connected through a coupling capacitor C_C to the base terminal of the first stage. This blocks any dc signal coming from the signal source and also prevents any dc current flowing through R_1 and R_2 towards the signal source.

Frequency response of the RC coupled amplifier: A very important criterion for comparing the performance of various amplifiers is to study their frequency response characteristics. That is, how the amplifier responds to signals of varying frequencies. For example, an amplifier may be used for amplifying speech signals such as in a public address system. A speech signal contains frequencies varying from 200 Hz to 3.2 kHz and ideally one desires that all the frequencies are equally amplified so that there is no distortion in speech after amplification.

Consider an input signal v_s applied to the input of the amplifier represented as:

$$v_s = V_m \sin(\omega t + \phi) \tag{9.41}$$

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If the voltage gain of the amplifier is of magnitude A and if the signal also goes through a phase shift (say lags by θ) then the output of the amplifier is given as:

$$v_0 = AV_m \sin(\omega t + \phi - \theta) \tag{9.42}$$

$$= AV_m \sin\left[\omega\left(t - \frac{\theta}{\omega}\right) + \phi\right] \tag{9.43}$$

If, we assume that the amplifier gain A is independent of frequency then according to Eq. (9.43), the amplitude of the output signal has got multiplied by A, frequency has remained same, but the signal has got shifted in time (delayed in this case) by an amount θ/ω. However, in practical amplifiers, both the amplification A and phase shift θ produced by the amplifier are functions of frequency due to the presence of frequency sensitive components such as coupling and by pass capacitors C_C, C_E and internal junction capacitances. Thus, different frequencies get multiplied by different values of gain and undergo varying phase shift. The amplitude response, therefore, is not uniform and time delay is also not constant introducing distortion in amplifiers. It is not usually necessary to specify both the amplitude and delay response as the two are related to each other. We shall emphasize more on the amplitude response characteristics.

The frequency response of an amplifier can be divided into three regions: The mid-frequency range is the one over which the amplification is reasonably constant and the delay or phase shift is also constant. In the low-frequency range, below the mid-band, the gain reduces with decreasing frequency and output approaches zero at dc ($f = 0$). In the high frequency range which is above the mid-frequency range, the amplifier gain decreases with increasing frequencies. The frequency response of amplifiers are usually plotted on semi log scale. The voltage gain is shown in dBs and frequency is plotted on the log scale. The reasons for taking logarithmic frequency scale are: (i) frequency range is usually large and (ii) ear response is logarithmic by nature. The frequency response of only one stage of R_C-coupled amplifier taking loading effects of the second stage will be analyzed. The effect of cascading on the frequency response will be dealt later.

Mid-frequency range. This is the range of frequencies at which external capacitors C_C and C_E are effectively short circuit and all the internal junction capacitors are open circuit. Thus, the circuit has no frequency sensitive component and the voltage gain is constant. Each CE stage provides a constant phase shift of 180°, so that the total phase shift provided by the two stage CE amplifier shown in Fig. 9.21 is 360° or 0°.

Low-frequency range. If the frequency is decreased from mid-frequency range, it is found that the voltage gain decreases. We will discuss the effect of the coupling capacitor C_C only and assume that the bypass capacitor C_E is large enough, so that is behaves as a short circuit even at low frequencies.

For analysis purpose, consider an intermediate stage from X_1 to X_2 in Fig. 9.21. The ac equivalent circuit using the approximate low frequency hybrid-π model is shown in Fig. 9.22(a) and its simplified circuit using Thevenin's equivalent is shown in Fig. 9.22(b).

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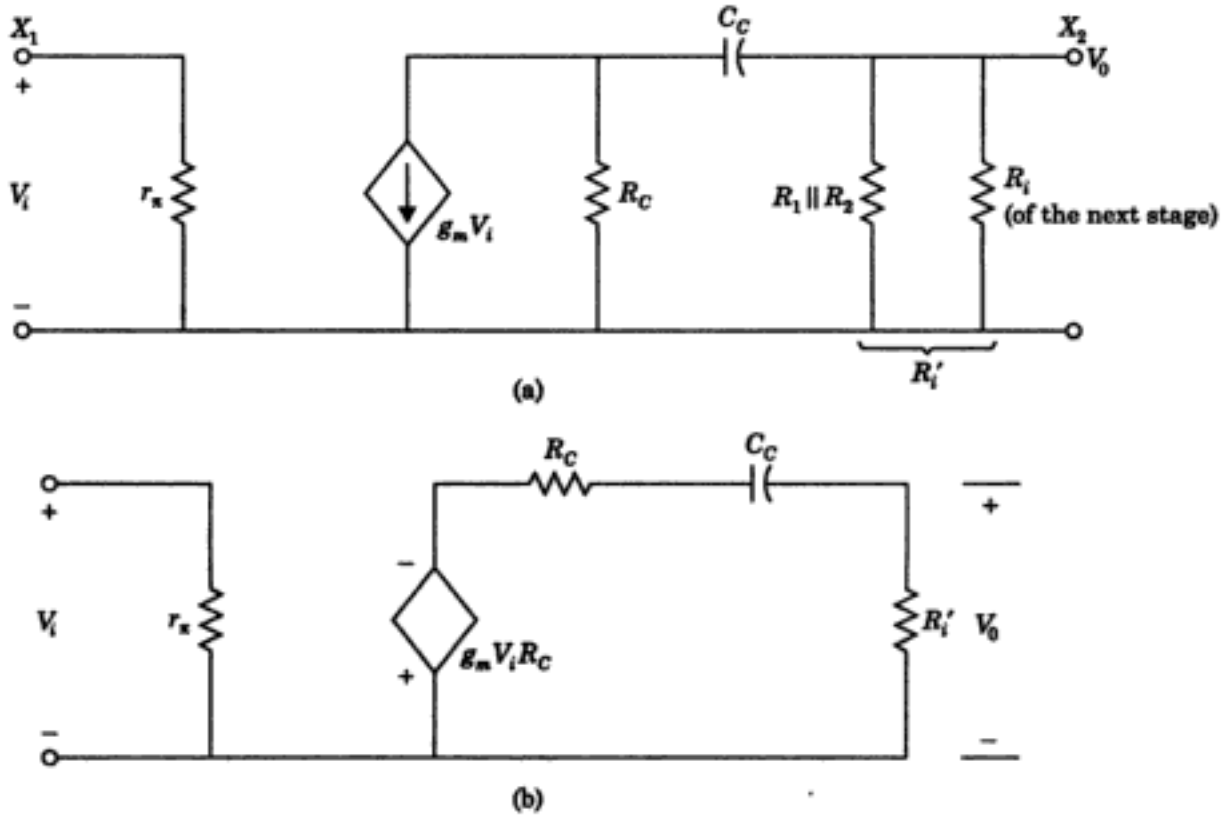


Fig. 9.22 (a) ac equivalent circuit, (b) Simplified circuit.

In Fig. 9.22(b),

$$V_0 = \frac{-g_m V_i R_C R_i'}{R_C + R_i' + 1/s\,C_C} \tag{9.44}$$

The voltage gain at low frequencies is:

$$A_{low} = \frac{V_0}{V_i} = \frac{-g_m R_C R_i'}{R_C + R_i' + 1/s\,C_C} \tag{9.45}$$

$$= \frac{-g_m R_C R_i'/(R_C + R_i')}{1 + 1/sC_C(R_C + R_i')} \tag{9.46}$$

$$= \frac{A_{mid}}{1 - jf_L/f} \tag{9.47}$$

where

$$A_{mid} = \frac{-g_m R_C R_i'}{R_C + R_i'} = -g_m(R_c \| R_i') \tag{9.48}$$

and

$$f_L = \frac{1}{2\pi C_C(R_C + R_i')} \tag{9.49}$$

The magnitude of the voltage gain at low frequencies is given as:

$$|A_{low}| = \frac{|A_{mid}|}{\sqrt{1 + (f_L/f)^2}} \tag{9.50}$$

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and the phase shift θ is:

$$\theta = \tan^{-1}(f_L/f) \tag{9.51}$$

The total phase shift at low frequencies is:

$$\theta_L = 180° + \tan^{-1}(f_L/f) \tag{9.52}$$

At $f = f_L$, $\theta_L = 180° + 45° = 225°$

The magnitude response of an amplifier is usually plotted on a semilog scale. The normalized voltage gain $\left|\frac{A_{low}}{A_{mid}}\right|$ in dBs w.r.t. normalized frequency f/f_L on log scale is shown in Fig. 9.23. The response approximated by piecewise linear curves is shown by solid lines and is referred to as Bode plot.

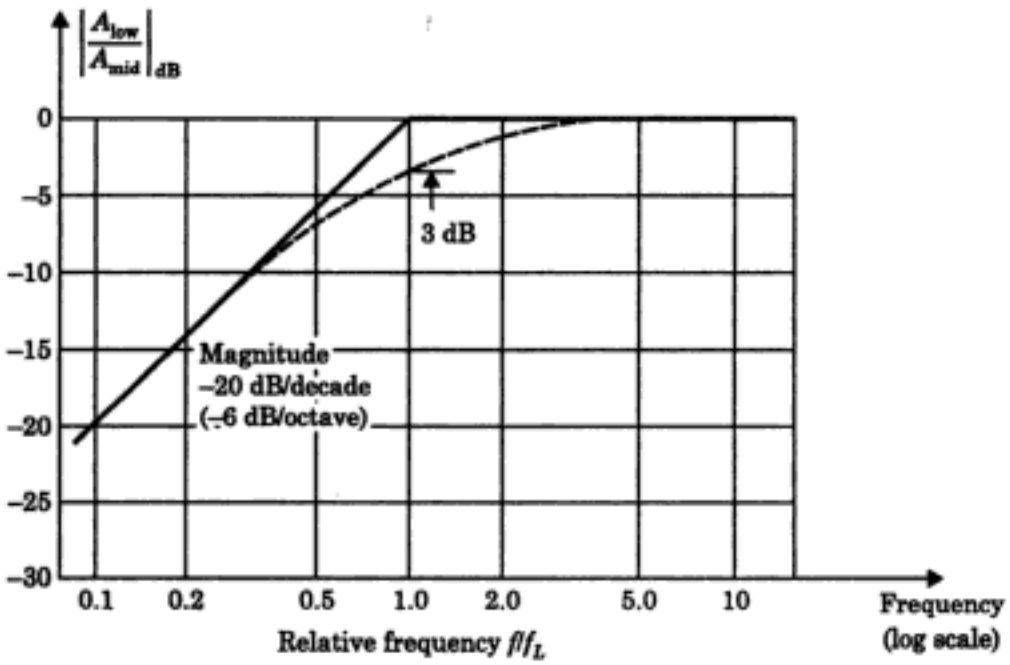


Fig. 9.23 Normalized response of a single stage RC-coupled amplifier at low frequencies.

It can be seen from Eq. (9.50), that

(i) for $f >> f_L$, (i.e. $f_L/f << 1$)

$$\left|\frac{A_{low}}{A_{mid}}\right| = 1 \tag{9.53}$$

or

$$\left|\frac{A_{low}}{A_{mid}}\right|_{dB} = 20 \log_{10}^{1} = 0 \text{ dB} \tag{9.54}$$

Thus, the response is a straight line at 0 dB in Fig. 9.23.

(ii) for $f = f_L$,

$$\left|\frac{A_{low}}{A_{mid}}\right| = \frac{1}{\sqrt{2}} = 0.707 \tag{9.55}$$

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or
$$\left|\frac{A_{low}}{A_{mid}}\right|_{dB} = -20 \log_{10} 0.707$$
$$\cong -3 \text{ dB} \tag{9.56}$$

The voltage gain at frequency f_L falls below by 3 dB from its value at mid band frequency. The frequency f_L is, therefore, referred to as lower 3-dB frequency. In terms of power, it can be seen from Eq. (9.55) that the power delivered at this frequency will be half the power delivered to load as mid-range of frequencies. Thus, the frequency f_L is also called **lower half power frequency**.

(iii) for $f << f_L$,

$$|A_{low}| = \frac{|A_{mid}|}{f_L/f} \tag{9.57}$$

or
$$\left|\frac{A_{low}}{A_{mid}}\right|_{dB} = 20 \log f - 20 \log f_L \tag{9.58}$$

The response is a straight line with a slope of 6 dB/octave (20 log 2 = 6 dB) or 20 dB/decade (20 log 10 = 20 dB) as shown in Fig. 9.23. The two straight lines intersect at $f = f_L$ and, therefore, frequency f_L is also called the **corner frequency**. The actual response will be asymptotic to these two approximated straight lines as shown by the dashed curve.

High frequency range. At high frequencies, the reactance of the coupling capacitor C_C is very small and can be assumed to be a short circuit. Thus, the capacitor C_C has no role at high frequencies. However, the effect of junction capacitances C_π (base to emitter), C_μ (base to collector) can not be neglected at high frequencies. These junction capacitances are always present, however at low and mid range of frequencies, their reactances are so large that these behave as open circuit. The ac equivalent circuit of the intermediate stage from X_1 to X_2 of Fig. 9.2 is shown in Fig. 9.24(a). The loading effect of second stage on the 1st stage has been represented by capacitance C_S and resistance R_i. Here the C_S represents the total capacitance $[C_\pi + C_\mu(1 + g_m R_L)]$ between base to emitter of transistor Q_2 where C_μ has been replaced by its Miller capacitance. The effect of junction capacitances at high frequencies has been discussed in Chapter 10 as well.

The simplified circuit using Thevenin's equivalent is shown in Fig. 9.24(b), from which we may write,

$$V_0 = -\frac{g_m V_i (R_C \,||\, R_i') \dfrac{1}{j\omega C_S}}{(R_C \,||\, R_i') + \dfrac{1}{j\omega C_S}} \qquad (R_i' = R_b \,||\, R_i) \tag{9.59}$$

Simplifying, we get

$$V_o = -\frac{g_m V_i \dfrac{R_C R_i'}{R_C + R_i'} \times \dfrac{1}{j\omega C_S}}{\dfrac{R_C R_i'}{R_C + R_i'} + \dfrac{1}{j\omega C_S}} \tag{9.60}$$

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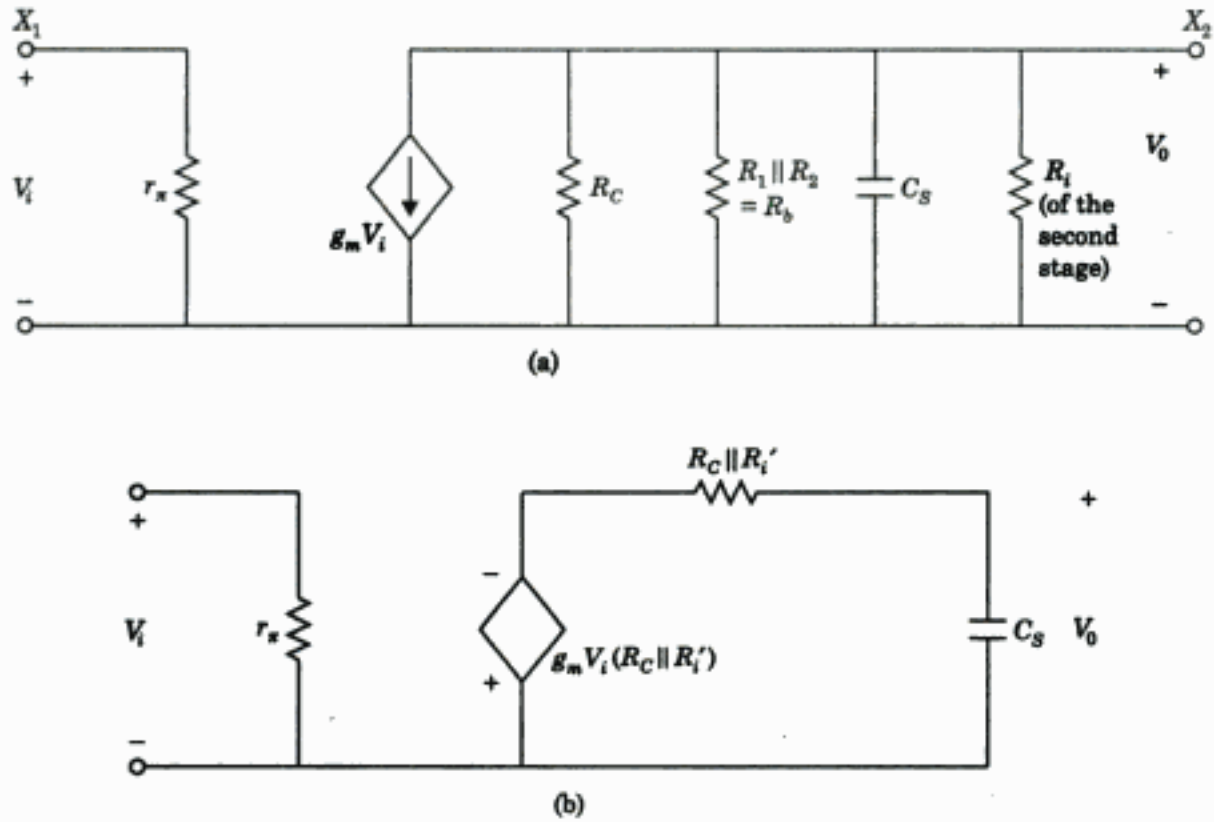


Fig. 9.24 (a) ac equivalent circuit at high frequencies where $C_S = [C_\pi + C_\mu(1 + g_m R_L)]$ where $R_i' = R_b \| R_i$, (b) Thevenin's equivalent of 9.24(a).

The voltage **gain A_{high} at high frequencies** is obtained as:

$$A_{high} = \frac{V_o}{V_i} = \frac{-g_m R_C R_i'/R_C + R_i'}{1 + j\omega C_S (R_C \| R_i')} \tag{9.61}$$

$$= \frac{A_{mid}}{1 + jf/f_H} \tag{9.62}$$

where $$f_H = \frac{1}{2\pi C_S (R_C \| R_i')} \tag{9.63}$$

Thus, the **magnitude response is given by**

$$|A_{high}| = \frac{|A_{mid}|}{\sqrt{1 + (f/f_H)^2}} \tag{9.64}$$

and phase shift θ is:

$$\theta = -\tan^{-1} f/f_H \tag{9.65}$$

The total phase shift **at high frequencies is:**

$$\theta_H = 180° - \tan^{-1} f/f_H \quad [180° \text{ due to } A_{mid}] \tag{9.66}$$

At $f = f_H$, $\tan^{-1}1 = 45°$

So $\theta_H = 180° - 45° = 135°$

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Total frequency response: We have analyzed one stage of the RC coupled amplifier at different frequency ranges. From these, the complete frequency response of the RC coupled amplifier can be plotted which is shown in Fig. 9.26. The response shown here has not been normalised.

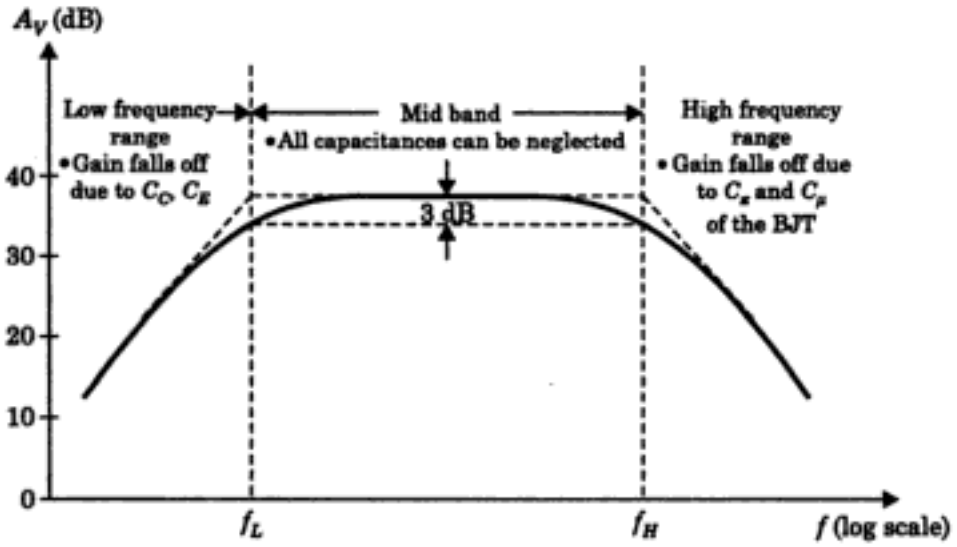


Fig. 9.26 Complete frequency response of single stage of RC-coupled amplifier.

A very important quantity of interest for the amplifier is its 3 dB bandwidth (BW) defined as:

$$BW = f_H - f_L$$

that is the bandwidth of an amplifier is the difference of upper cut-off frequency f_H and lower cut-off frequency f_L. Bandwidth is taken as a measure for comparing the performance of amplifiers. An amplifier with high BW need not necessarily be good. It should have high gain too. Suppose we have two amplifiers with the following values:

	Gain	BW
Amplifier 1	400	20 kHZ
Amplifier 2	100	50 kHZ

So, which of the two amplifiers will be considered better. One with high voltage gain or the one with high bandwidth. The amplifier which provides high gain bandwidth is considered to be better. Thus, a more important criterion which gives the figure of merit of various amplifiers is gain bandwidth product (GBW). Higher the value of GBW product, better is the amplifier.

Phase shift characteristics: The complete phase shift characteristics of the RC coupled amplifier is shown in Fig. 9.27. The phase shift θ be summarized as

Mid-band frequency: $\theta = 180°$ (9.71)

Low frequency range: $\theta_L = 180° + \tan^{-1} f_L/f$ (9.72)

High frequency range: $\theta_H = 180° - \tan^{-1} f/f_H$ (9.73)

Loading effects in RC coupled amplifier: There is one drawback of RC coupling in multistage BJT amplifiers. The input resistance r_π (or h_{ie}) of a BJT is quite low (of the order of 1 kΩ) and it comes in parallel to the load resistance R_C of the previous stage in cascaded amplifiers. This reduces the effective load of each stage and hence the voltage gain of the

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stage gets reduced due to this loading effect. Because of this the overall gain of the cascaded amplifier is less than the product of the voltage gain of the individual stages (without loading).

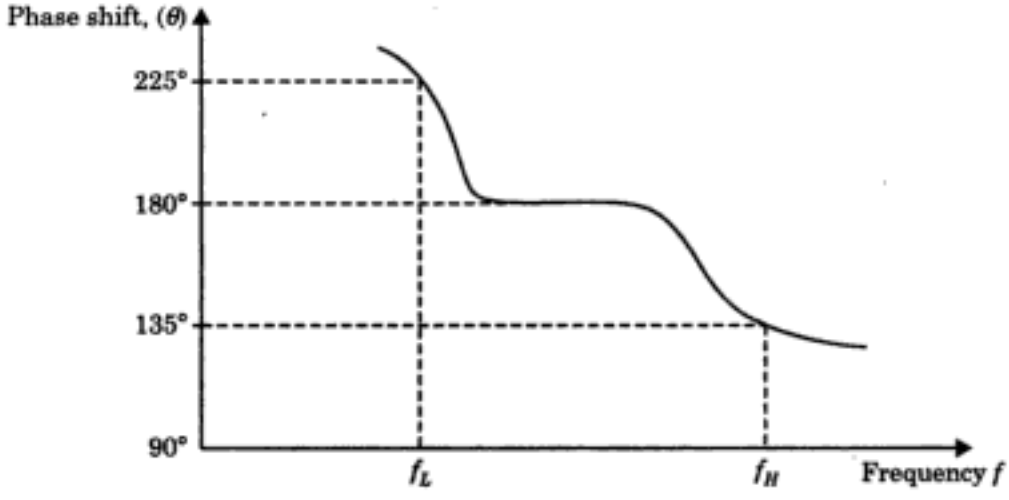


Fig. 9.27 Phase shift characteristics of an RC coupled amplifier.

9.3.2 Transformer Coupled Amplifier

The loading effect can be reduced by replacing the resistance R_C with a transformer. The primary winding of the transformer is connected between collector and dc supply and the secondary winding is connected to the load. By proper selection of the turns ratio of the transformer, impedance matching between the low input impedance of a stage (or load) with the output impedance of the previous stage can be achieved. The frequency response of a transformer coupled amplifier is shown in Fig. 9.28. It is seen that the response is flat at

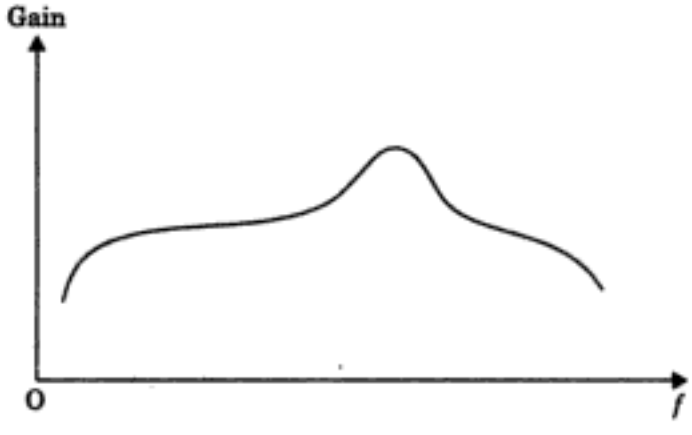


Fig. 9.28 Frequency response of a transformer coupled amplifier.

low frequencies and exhibits resonance at a high frequency where voltage gain becomes high. The transformer coupling is rarely used at audio range of frequencies as the size of the transformer becomes very bulky at low frequencies and the cost is also very high. And when used at high frequencies, the inductance and interwinding capacitance gives rise to

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resonance phenomenon. With proper design, this type of coupling is used for amplifying radio frequency signals (> 20 kHz). However, the most important application of transformer coupling is in the last stage of a system to provide impedance matching. For example, in a public address system or a transistorised radio, the load is a loudspeaker with a low resistance (4-15 Ω) value, so the transformer coupling provides excellent impedance matching.

9.3.3 Direct Coupled Amplifiers

The output of the first stage is directly connected as input to the next stage without any coupling device. Thus, very low frequency signals (<10 Hz) and even dc signals can be amplified. These amplifiers are very useful for low frequency applications. As an example, consider the use of a thermocouple for measuring the temperature of a furnace. The output voltage of the thermocouple will be very low (in μV) and, therefore, needs to be amplified. It will also be slowly varying as the temperature of the furnace varies slowly. In such applications, one can use a direct-coupled multistage amplifier. The frequency response of a direct-coupled amplifier is shown in Fig. 9.29. The response is flat up to the upper cut-off frequency f_H. One major drawback of this type of coupling is that as dc signals are not blocked, the dc current from one stage also goes to the next stage thereby disturbing the quiescent conditions of the next stage. Further any variations in the dc voltages and currents due to temperature variations or change of device are passed on to the next stage. The temperature stability of such amplifiers is poor, although it can be improved to a certain extent by using negative feedback in the circuit.

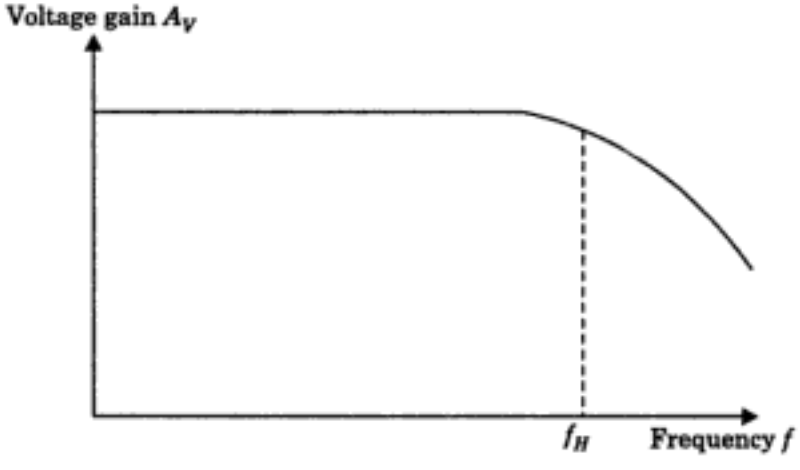


Fig. 9.29 Frequency response of a direct coupled amplifier.

The direct coupling, however is very useful in differential amplifiers which form the basic building block of an operational amplifiers.

9.4 DIFFERENTIAL AMPLIFIER

A cascaded direct coupled amplifier can provide high gain down to zero frequency (see Fig. 9.29) as it has no coupling capacitor. However, such an amplifier suffers from the major problem of drift of the operating point due to temperature dependency of I_{CO}, V_{BE} and h_{FE} of the transistor. This problem can be eliminated by using a balanced or differential amplifier as

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shown in Fig. 9.30. It may be seen that it is essentially an emitter-coupled differential amplifier. The main advantage of a differential amplifier is that these are less sensitive to noise and interference. A differential amplifier amplifies only the difference of the signals applied to the two bases B_1 and B_2 and any signal such as noise or interference which is common to the two bases is rejected.

A differential amplifier of the type shown in Fig. 9.30 can be used in four different configurations depending upon the number of input signals used and the way output is taken. These four configurations are:

(i) Differential-input, differential-output or dual-input balanced-output
(ii) Differential-input, single ended-output
(iii) Single-input, differential-output
(iv) Single-input, single ended-output

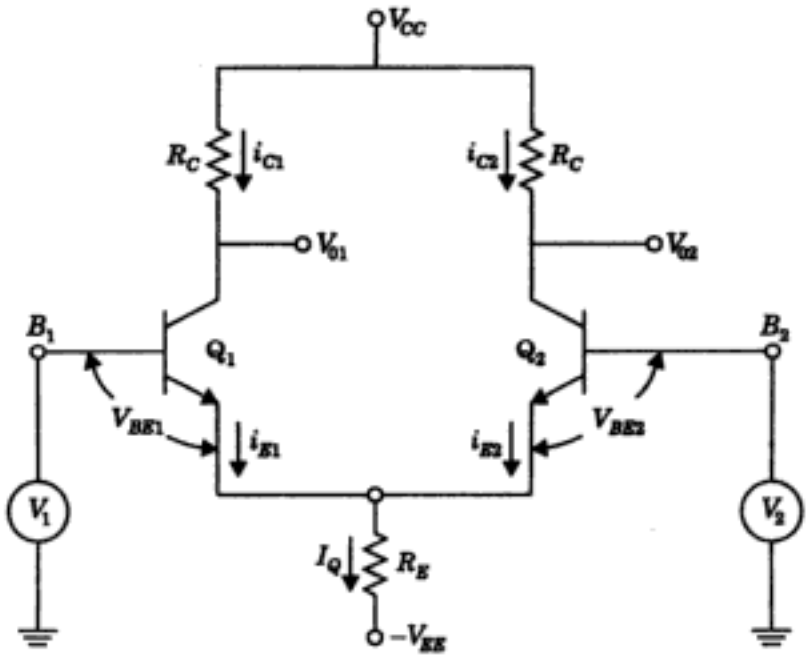


Fig. 9.30 The basic differential amplifier.

If the signal is applied to both the inputs then it is differential input or dual input and the difference of signals applied to the two inputs gets amplified. In many applications, a single input is only used. Similarly, if the output voltage is measured between two collectors then it is differential output. This is also referred to as a balanced output, as both collectors are at the same dc potential w.r.t. ground.

Low frequency small signal analysis of differential amplifier: An ideal dual-input balanced output DA as shown in Fig. 9.30 should amplify only the differential signal at the two inputs and reject the signal common to these inputs. As transistors Q_1 and Q_2 are a matched pair of transistors, thus any unwanted signal, such as noise or hum pick up which is common to both the inputs would get rejected. However in a practical case transistors Q_1 and Q_2 are not equally matched and output does appear even when same voltage is applied to the two input terminals. In this section, we will discuss how to compute the small signal differential mode gain A_{DM} and common-mode gain A_{CM}. These expressions help in finding the figure of merit CMRR that is, common mode rejection ratio of the differential amplifier.

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The ac analysis of the differential amplifier can be performed either by using hybrid-π model or h-parameter model. Both the approaches have been dealt with.

Differential-mode gain A_{DM}: In Fig. 9.31, for $V_1 = V_2$, the current I_Q divides equally into the two transistors Q_1 and Q_2 because of the symmetry of the circuit. However, if V_1 is now increased by an incremental voltage (small signal) $v_d/2$ and V_2 is decreased by $v_d/2$ as shown in Fig. 9.31, it can be seen that the differential amplifier is being fed by differential small signal v_d. The common mode small signal is naturally zero. The collector current i_{C1} will now increase by an incremental current i_c and i_{C2} will decrease by an equal amount. The sum of total currents in transistors Q_1 and Q_2 however remains constant as constrained by the constant current I_Q. As there is no change of current through R_E, the voltage V_E at the common emitter point E remains constant. Thus, for small signal analysis, the common emitter point E can be considered to be at ground potential as shown in Fig. 9.31.

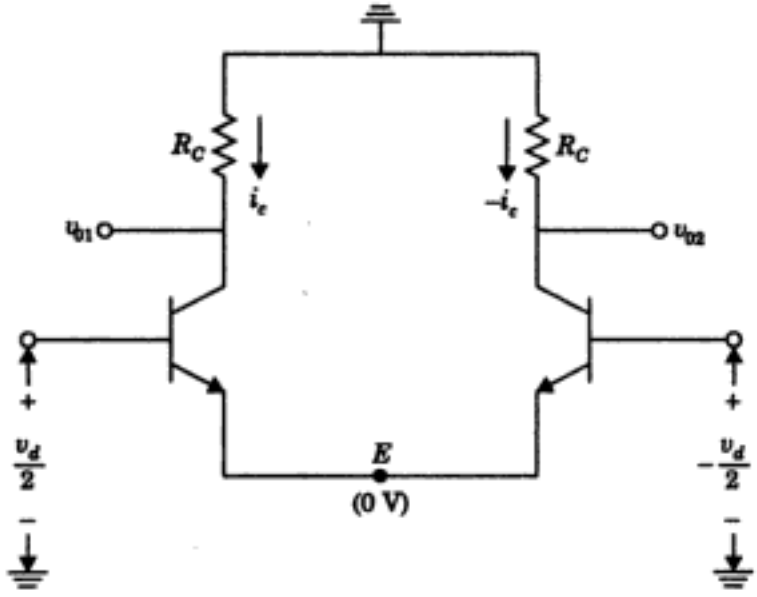


Fig. 9.31 Differential amplifier when different input signal applied.

Analysis:

Using hybrid-π model. Since the performance of two sides of the differential amplifier is identical, we need to analyze only one side of the differential amplifier called **differential-half circuit**. Figure 9.32(a) shows a single stage CE transistor amplifier fed by a small signal voltage $v_d/2$ and its ac equivalent circuit using hybrid-π model is shown in Fig. 9.32(b). From Fig. 9.32(b),

$$v_\pi = \frac{v_d}{2}; \quad v_{01} = -g_m v_\pi R_C \tag{9.74}$$

Therefore,

$$\frac{v_{01}}{v_d} = -\frac{1}{2} g_m R_C \tag{9.75}$$

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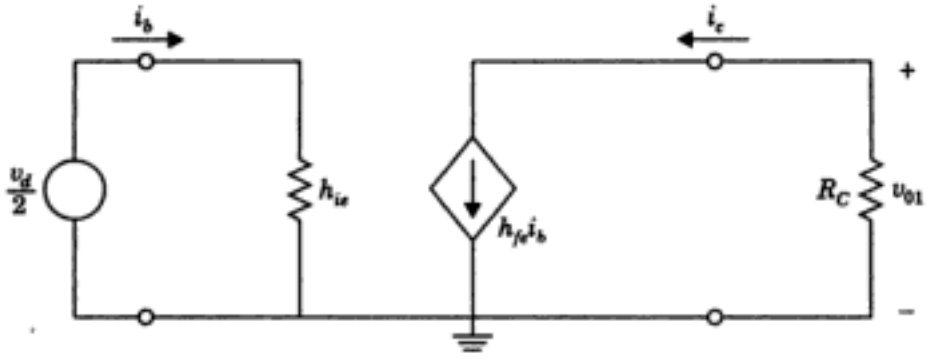


Fig. 9.33 Small signal equivalent circuit of differential half circuit using h-parameter model.

Therefore, the differential mode gain A_{DM} is given by

$$A_{DM} = \frac{v_{01}}{v_d} = -\frac{1}{2}\frac{h_{fe}}{h_{ie}}R_C \qquad \text{(Single-ended output)} \tag{9.83}$$

Similarly, we may write

$$A_{DM} = \frac{v_{02}}{v_d} = \frac{1}{2}\frac{h_{fe}R_C}{h_{ie}} \qquad \text{(Single-ended output)} \tag{9.84}$$

If the output is taken differentially between the two collectors then

$$A_{DM} = \frac{v_{01} - v_{02}}{v_d} = -\frac{h_{fe}R_C}{h_{ie}} \qquad \text{(differential-output)} \tag{9.85}$$

In the analysis, the source resistance R_S has not been taken into account.

Common-mode gain A_{CM}: Now, consider the case when V_1 and V_2 both are increased by an incremental voltage v_c. The differential signal v_d now is zero and common-mode signal is v_c. Both the collector currents i_{C1} and i_{C2} will increase by an incremental current i_c. The current through R_E now increases by $2i_c$. The voltage V_E at the emitter node is $2i_cR_E$ and no longer constant. In order to draw the common mode half circuit, replace resistance R_E by $2R_E$ as shown in Fig. 9.34(a). The common-mode gain A_{CM} is calculated from the small-signal hybrid-π equivalent model shown in Fig. 9.34(b). It can be seen

$$A_{CM} = \frac{v_{01}}{v_c} = \frac{v_{02}}{v_c} = \frac{-\beta_0 R_C}{r_\pi + 2(1+\beta_0)R_E} \tag{9.86}$$

For $\beta_0 >> 1$,

$$A_{CM} = \frac{-g_m R_C}{1 + 2g_m R_E} \cong -\frac{R_C}{2R_E} \tag{9.87}$$

It can be seen that, if the output is taken differentially, then the output voltage $v_{01} - v_{02}$ will be zero and the common-mode gain will be zero. However, if the output is taken single ended, the common-mode gain will be finite and given by Eqs. (9.86) and (9.87).

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The common mode gain A_{CM} using h-parameter model can be easily computed as:

$$A_{CM} = \frac{v_{01}}{v_c} = \frac{-h_{fe}R_C}{h_{ie} + (1 + h_{fe})2R_E} \tag{9.88}$$

Common-mode rejection ratio (CMRR): The common-mode rejection ratio (CMRR) is defined as:

$$\text{CMRR} = \left| \frac{A_{DM}}{A_{CM}} \right| \tag{9.89}$$

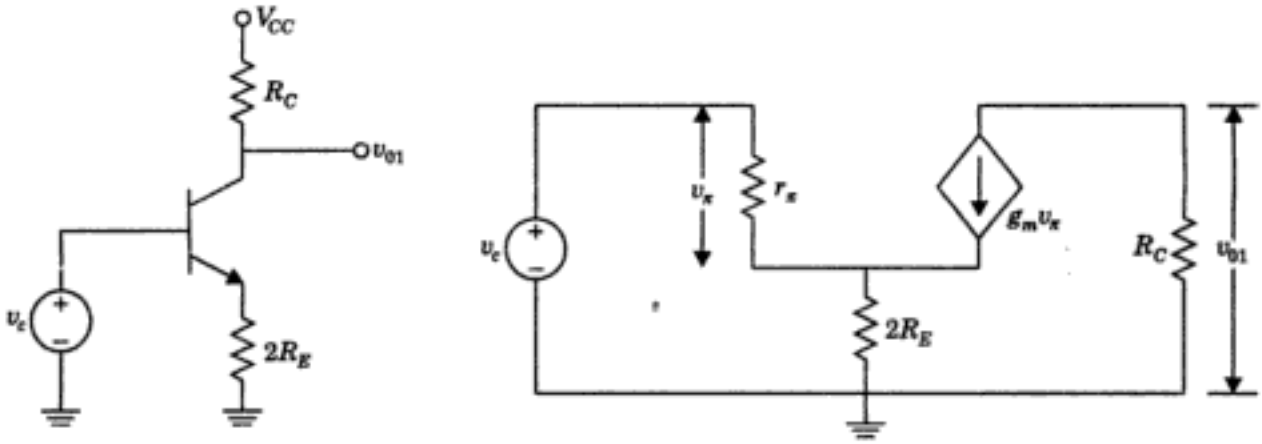


Fig. 9.34 (a) Common-mode half circuit (b) ac equivalent circuit using hybrid-π model.

For differential-input, differential-output, using Eqs. (9.77) and (9.86), we obtain

$$\text{CMRR} \cong \frac{g_m R_C(1 + 2g_m R_E)}{g_m R_C} \tag{9.90}$$

$$= 1 + 2g_m R_E$$

$$\cong 2g_m R_E \tag{9.91}$$

CMRR is normally expressed in dB, so

$$\text{CMRR} = 20 \log \frac{|A_{DM}|}{|A_{CM}|} \tag{9.92}$$

SUMMARY

- Amplifier stages are cascaded to obtain desired values of voltage gain, current gain, input and output impedances.
- The overall voltage gain of a multi-stage amplifier is less than the product of gains of individual stages due to loading effects.
- A Darlington pair consists of two transistors in CC–CC cascade and provides very high current gain, very high input impedance, voltage gain unity (slightly less than a single CC stage) and low output impedance.

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9.6 Draw the frequency response of an *RC* coupled amplifier and explain why gain falls at low and high frequencies.

9.7 Define upper cut-off and lower cut-off frequencies of a *RC* coupled amplifier. What is the significance of these frequencies?

9.8 Show that the gain bandwidth product of an *RC* coupled amplifier is constant.

9.9 Explain why the frequency response of amplifiers is plotted on a semilog scale.

9.10 Explain the advantages and disadvantages of (i) transformer coupling (ii) direct coupling.

9.11 Explain "overall voltage gain of a multistage amplifier is less than the product of individual stages".

9.12 Discuss one application of direct coupled multistage amplifier.

9.13 Explain how drift of operating point is overcome in direct coupled stages.

9.14 Draw the circuit of an emitter coupled differential amplifier and explain its working.

9.15 Explain and derive the expression for differential mode gain A_{DM} and common-mode gain A_{CM} of a differential amplifier.

9.16 Define and explain the significance of CMRR.

NUMERICAL PROBLEMS

P9.1 Calculate the overall voltage gain for the BJT cascade shown in Fig. 9.38. The value of β for both the transistors is given as $\beta = 150$.

***(Ans.* 23642)**

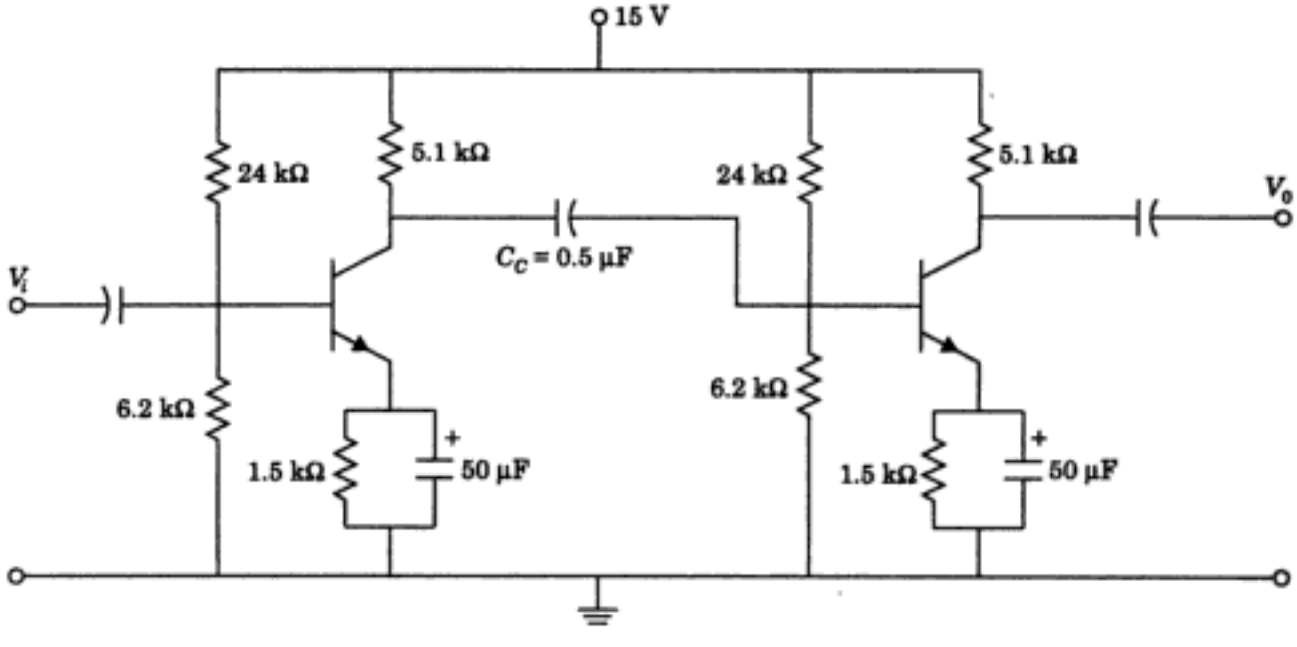


Fig. 9.38 Circuit for P9.1.

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P9.4 A two-stage FET RC coupled amplifier has the following parameters: g_m = 10 mA/V, r_d = 6 kΩ, R_D = 10 kΩ, R_G = 1 MΩ for each stage. Find the overall mid-band gain.

(***Ans.*** 1406.2)

P9.5 A three-stage *RC* coupled amplifier uses FETs with the parameters: g_m = 2.6 mA/V, r_d = 10 kΩ, R_D = 10 kΩ, R_G = 0.1 MΩ. Evaluate overall mid-band gain.

(***Ans.*** –27,000)

P9.6 It is desired that the voltage gain of a BJT *RC* coupled amplifier at 60 Hz should be ten percent of its mid-band value. Show that the coupling capacitor C_C must at least be equal to $5.5/[(r_\pi || R_B) + R_C]$ where $R_B = R_1 || R_2$.

P9.7 Calculate the amplifier voltage gain for the circuit shown in Fig. 9.41. Given β_D = 6000, r_i = 5 kΩ.

(***Ans.*** 0.998)

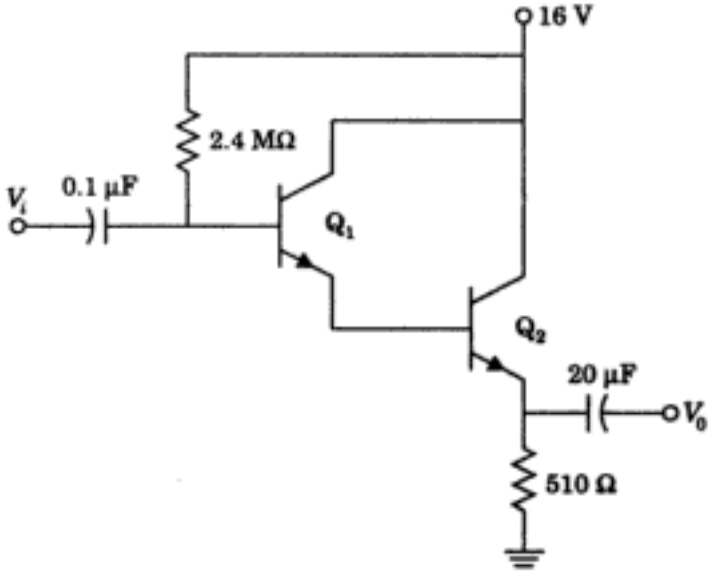


Fig. 9.41 Circuit for P9.6.

P9.8 A two-stage CE–CE amplifier uses transistors biased at I_{CQ} = 1 mA, and having parameters as: β_0 = 125. Also given that R_S = 0.6 kΩ, $R_{C1} = R_{C2}$ = 1.2 kΩ. Determine (i) r_π (ii) overall voltage gain.

(***Ans.*** 3.125 K; 1396)

P9.9 A cascade configuration shown in Fig. 9.42 uses transistors from Q_1 to Q_N with same β. Assume $r_\pi = 0$. Find the input resistance R_i.

(***Ans.*** $R_i = R_E(1 + h_{fe})^N$)

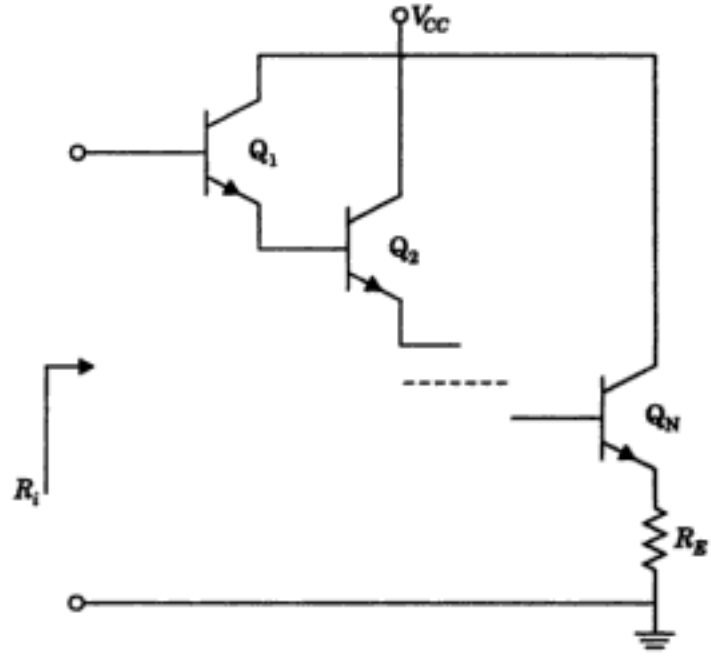


Fig. 9.42 Circuit for P9.9.

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P9.10 For the circuit shown in Fig. 9.43 verify that

(a) $A_{V1} = \dfrac{V_{01}}{V_i} = \dfrac{g_{m1}\beta_0 R_S}{1 + g_{m1}\beta_0 R_S}$

(b) $A_{V2} = \dfrac{V_{02}}{V_i} = \dfrac{g_{m1}\beta_0 (R_S + R_C)}{1 + g_m \beta_0 R_S}$

Assume: $R_D >> r_\pi$, $r_d >> r_\pi$, $\beta_0 >> 1$ and $\mu >> 1$.

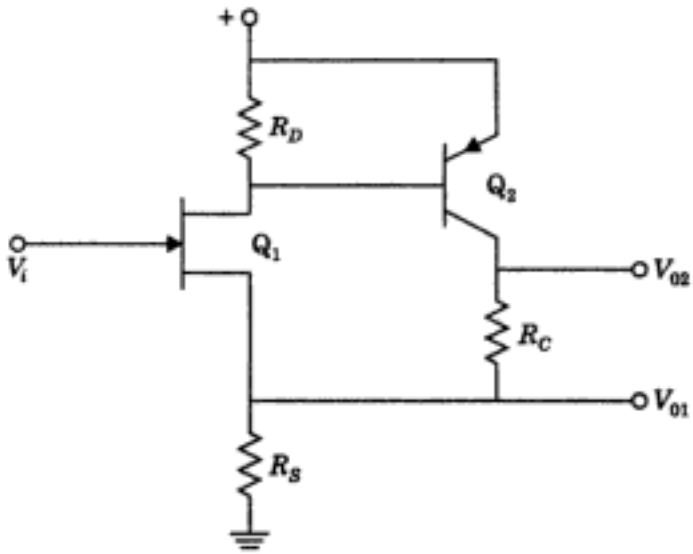


Fig. 9.43 Circuit for P9.10.

P9.11 A differential amplifier uses a transistor with $\beta = 200$ and biased with $I_Q = 100$ μA. Determine R_C and R_E so that $|A_{DM}| = 500$ and CMRR = 80 dB.

(***Ans.*** 125 kΩ, 1.25 MΩ)

P9.12 For the differential amplifier shown in Fig. 9.44, it is given that β for both the transistors is 200. Find

(a) For $v_1 = v_2 = 0$, determine the bias currents I_{CQ} and I_{BQ}.

(b) Find v_{01} and v_{02} for the conditions in (a).

(c) Find A_{DM}, A_{CM} and CMRR.

(***Ans.*** (a) 0.495 μA, 2.48 μA, (b) $v_{01} = v_{02} = 10.0$ V, (c) –198, –0.347, 55.1 dB)

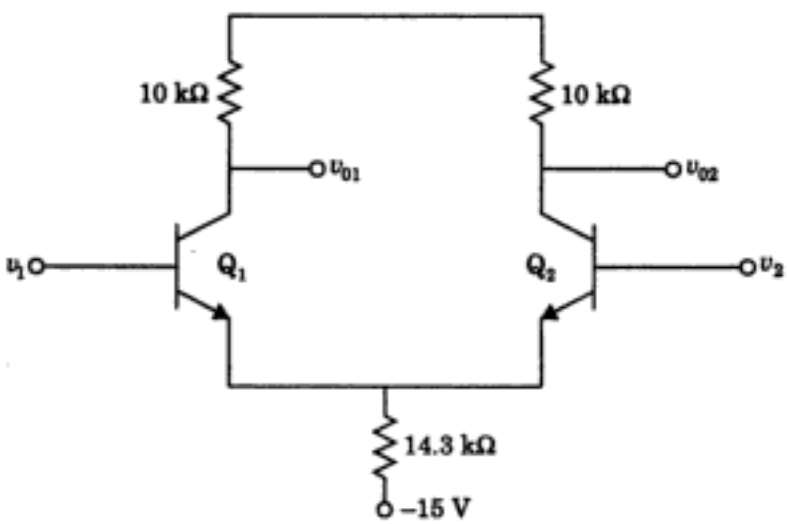


Fig. 9.44 Circuit for P9.12.

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P9.13 Calculate (i) g_m (ii) V_0 in the circuit shown in Fig. 9.45. Given $\beta_0 = 200$.

(***Ans.*** 6.84 mA/V, 492.4 mV)

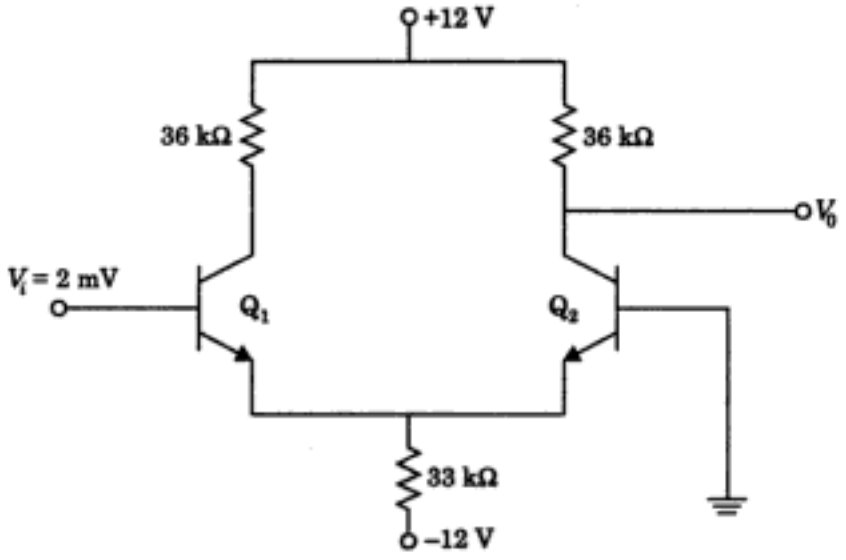


Fig. 9.45 Circuit for P9.13.

P9.14 For the Darlington follower shown in Fig. 9.46, transistor Q_1 has a $\beta = 20$ and transistor Q_2 has a $\beta = 200$. Assume $V_{BE} = 0.7$ V and neglect the effect of r_0.

(a) Find the dc emitter currents I_{E1}, I_{E2} and dc voltages V_{B1} and V_{B2}.

(b) Find input resistance R_i.

(c) Find the overall voltage gain V_0/V_s.

(***Ans.*** (a) 30 μA, 2 mA, 3.79 V, 3.09 V, (b) 448 kΩ, (c) 0.805)

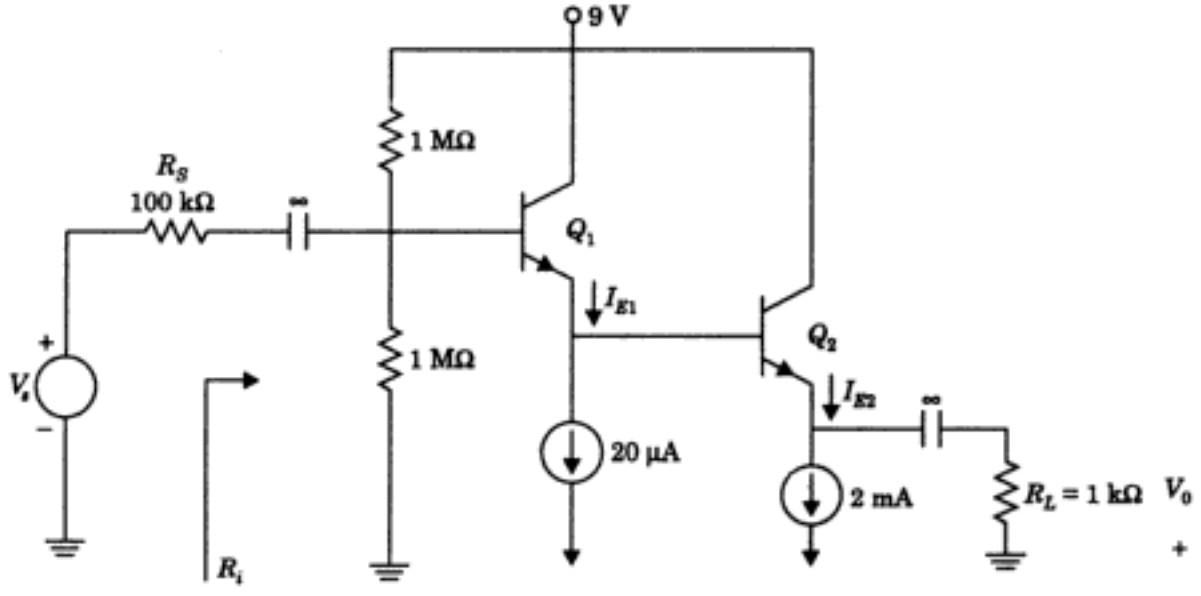


Fig. 9.46 Circuit diagram for P9.14.

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P9.15 The circuit in Fig. 9.47, shows an amplifier using a *pnp* and *npn* transistor in parallel. Assume transistors have identical characteristics. Derive an expression for the voltage gain and input impedance.

$$\left(A_V = \frac{2(1+h_{fe})R_E}{h_{ie}+2(1+h_{fe})R_E},\ R_i = \frac{h_{ie}}{2}+(1+h_{fe})R_E \right)$$

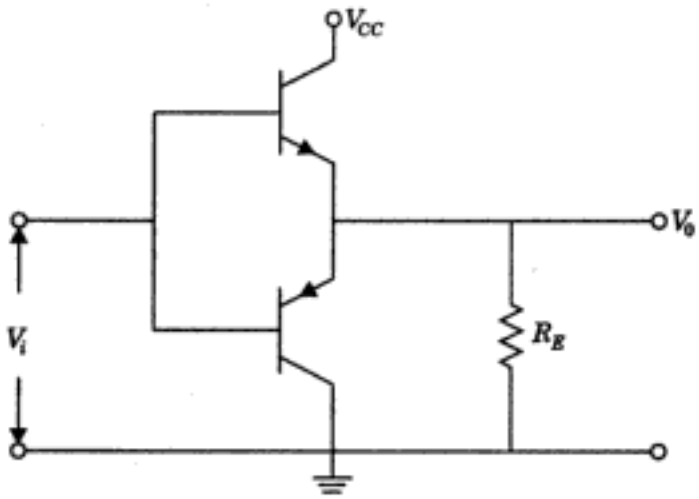


Fig. 9.47 Circuit for P9.15.

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CHAPTER 10

Frequency Response of Amplifiers

10.1 INTRODUCTION

In practice, a useful signal is made up of a number of frequencies. It is rare that we deal with a signal of only one frequency except in some communication systems. A signal of a single frequency is usually obtained from oscillators. Such single frequency oscillations can easily be amplified though some special devices might be required when the frequency is in the range of Gigahertz (1 GHz = 10^9 Hz). However, when we deal with a signal containing a number of frequencies, its amplification poses many problems if we aim at faithful reproduction of the amplified version from the low amplitude input signal. The voltage or current gain of an amplifier is a function of device parameters, such as r_π (i.e., h_{ie}), C_π (i.e., diffusion capacitance C_D due to forward conduction of base-emitter diode) and C_μ (i.e., depletion capacitance C_T due to reverse biasing of the base-collector diode) for the case of BJTs; and the capacitances C_{gs} (between the gate and source), C_{gd} (between the gate and drain), C_{ds} (between the drain and source) in the case of FETs. Besides these capacitances, the coupling capacitances, the bypass and the blocking capacitors also appear in the calculation of voltage and current gains.

The signals utilized in many electronic systems have to be amplified with a minimum distortion. Thus, for this purpose, the active devices involved must operate linearly, i.e., the small-signal conditions must apply.

When the amplifiers are required to operate over a broad frequency range, the internal capacitances of the active device and the coupling capacitances' effect must be taken into account. The low frequency edge of the signal may be DC or a few hertz, the high frequency may go upto tens of gigahertz. The square pulses, in general, and particularly in television, radar and sonar etc. require wideband amplifiers. The various capacitances appearing in the amplifiers have frequency-dependant reactances ($\because X_C = 1/j\omega C$). Hence, the amplifier gain depends on the frequency content of the input signal. If the amplifier has not constant gain for all the frequencies of interest, the output signals would have frequency distortion. The aim is to have the minimum possible distortion in the amplification process.

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In this chapter, we shall study how a low-level or a weak signal containing frequencies from DC to a few megahertz can be amplified with a minimum distortion. We shall first determine the frequency response of single-stage BJT and FET amplifiers. Thereafter we shall extend this treatment to multi-stage amplifiers. As the rigorous analysis becomes quite involved when an amplifier (single or multistage) consists of many capacitors in the equivalent circuit, an approximate method for evaluating the frequency response may be usefully adopted. Such approximation methods are also developed in this chapter.

It may be noted that the integrated-circuit amplifiers are, in general, direct-coupled (i.e., do not use the coupling capacitors). Their performance at low frequencies is, therefore, highly satisfactory. However, their performance deteriorates at high frequencies due to the internal capacitances of the transistors (C_π, C_μ, C_{gs}, C_{gd}, C_{ds} etc.). On the other hand, the discrete-component stages invariably use coupling and bypass capacitors, and, therefore, their performance deteriorates at low frequencies. It is useful to study the behaviour of single and multistage amplifiers at high frequencies first and then discuss their performance at low frequencies.

In this chapter, we shall discuss the following topics:

- Frequency-response characteristics
- Asymptotic Bode's diagram
- High frequency response of amplifiers
- Low frequency response of amplifiers
- Total (high and low frequency) response
- Bandwidth—(3 dB bandwidth)
- Parameters to determine the response to a square wave input signal (tilt and sag)
- Common emitter short circuit current gain (and parameter f_T)
- The generalised gain function (and dominent pole approximation)
- High-frequency response of a common emitter stage
- An important result (useful for the analysis)
- CE configuration analysis by unilateral hybrid-π model
- The gain–bandwidth product
- Common source (CS) stage at high frequency
- Emitter and Source followers at high frequencies
- The Source follower analysis
- The time constant method of obtaining the response
- The frequency response of cascaded stages
- The cascode (CE–CB) amplifier
- The effect of coupling and bypass capacitors

10.2 FREQUENCY-RESPONSE CHARACTERISTICS

If the input, low-level, signal is sinusoidal, the output (amplified) signal is also sinusoidal. However, if the input signal contains a number of frequencies, and each frequency has different amplifications then the gain may be written as:

$$\bar{A} = A\angle\theta$$

where $\bar{A}$ is a vector, A and θ are the amplitude and phase responses, respectively. In general, A and θ are functions of frequency f. The frequency-response characteristic of an amplifier is the plot of gain and phase versus frequency. Bode diagram is used to display the frequency response. The asymptotic Bode diagram is a convenient approximation of this

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sinusoids (sine or cosine waves) used in electronic circuits are of wide range. For example, the signals in audio systems are in the range of 3 Hz to 30 KHz. It is, therefore, necessary to determine the response of the network transfer function, usually denoted by $G(s)$, at each frequency. The response contains the information of magnitude response $G(j\omega)$ and phase response $\angle G(j\omega)$, ploted versus the frequency ω (though $\omega = 2\pi f$, but ω is also called frequency, in radian/sec). The function $G(s)$ is the Laplace transform of time signal $g(t)$.

$$\therefore \qquad G(s) = \int_0^\infty g(t)\, e^{-st} dt \tag{10.6}$$

where $G(s)$ is the system response, i.e., the circuit's transfer function.

Here, s is the Laplace parameter. If we replace s by $j\omega$ then we obtain a complex function denoted by $\bar{G}(j\omega)$ which is a vector quantity. Some authors prefer $s = j\Omega$ where Ω has the same effect as ω. $\bar{G}(j\omega)$ is system's frequency response. The bar on $\bar{G}(j\omega)$ indicates that $\bar{G}(j\omega)$ is a vector quantity having phase and magnitude. We can write

$$\begin{aligned} \bar{G}(j\omega) &= |\bar{G}(j\omega)|\, \angle \bar{G}(j\omega) \\ &= G(j\omega)\ .\ \angle\theta(\omega) \end{aligned} \tag{10.7}$$

where $|\bar{G}(j\omega)|$ is mod of $\bar{G}(j\omega)$ and is denoted by $G(j\omega)$ being a scalar quantity, and $\angle\bar{G}(j\omega)$ is phase angle of $\bar{G}(j\omega)$, it is sometimes denoted by $\theta(\omega)$. It is customary to express $G(j\omega)$ in **decibels (dB)**, i.e.,

$$G(j\omega) \text{ in dB} = 20 \log G(j\omega) \tag{10.8}$$

(Note that '*d*' implies deci and B (always capital letter) refers to Grahm Bell).

A plot (graph) drawn with $G(j\omega)$ in dB along y-axis and log ω along x-axis together with $\theta(\omega)$ (i.e. the phase response) along y-axis and log ω along x-axis is called the **BODE diagram.** Bode diagram gives information of behaviour (i.e. response) of the circuit for different frequencies in the input signal when the input signal contains a large range of frequencies. By chosing log ω on x-axis we can represent the large range of frequencies much more conveniently than if we took ω along the x-axis (and not log ω). Note that the Bode diagram gives approximate frequency-response characteristic which is adequate for many applications. However, the nature of Bode diagrams leads to simply drawn approximate characteristics, called **asymptotic Bode diagram.**

The network function of any system has a generic form given by

$$G(s) = \left(\sum_{i=0}^{m} a_i s^i\right) \Big/ \left(\sum_{i=0}^{n} b_i s^i\right) = \frac{N(s)}{D(s)} \tag{10.9}$$

which may by written as:

$$G(s) = K\, \frac{1 + a_1 s + a_2 s^2 + \cdots + a_m s^m}{1 + b_1 s + b_2 s^2 + \cdots + b_n s^n} \tag{10.10}$$

where $K = a_0/b_0$ and the a_i, b_i in Eq. (10.10) are some other constants and not the same as a_i, b_i of Eq. (10.9). The numerator polynomial and the denominator polynomial in Eq. (10.10) can be factorized and Eq. (10.10) may be expressed as:

$$G(s) = K\, \frac{(1 + s/Z_1)(1 + s/Z_2) \cdots (1 + s/Z_m)}{(1 + s/p_1)(1 + s/p_2) \cdots (1 + s/p_n)} \tag{10.11}$$

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Here, $-Z_1$, $-Z_2$, ..., etc. are the roots of the numerator polynomial and $-p_1$, $-p_2$, ..., etc. are the roots of the denominator polynomial. Note that $-Z_i$ indicates zeros of Eq. (10.11), i.e., at $s = -Z_1$, $s = -Z_2$, $s = -Z_m$, $G(s)$ becomes zero. Hence $-Z_i$ are called **zeros of G(s).** Similarly, $s = -p_i$ are called **poles of G(s)** since at $s = -p_1$, $s = -p_2$, ..., $s = -p_n$ the system function $G(s)$ assumes a value of infinity. For determining the frequency response, we replace s by $j\omega$ in Eq. (10.11). This yields

$$\bar{G}(j\omega) = K \frac{(1 + j\omega/Z_1)(1 + j\omega/Z_2)\cdots(1 + j\omega/Z_m)}{(1 + j\omega/p_1)(1 + j\omega/p_2)\cdots(1 + j\omega/p_n)} \tag{10.12}$$

The expression for $\bar{G}(j\omega)$ is a product of a constant K and a group of terms of the form $(1 + j\omega/Z_l)$ or $1/(1 + j\omega/p_m)$. Each of these terms can be thought of individual vector (also called **phasor**). Hence the resultant $\bar{G}(j\omega)$ has a **magnitude** which is the product of the magnitudes of individual term; and the resultant $\bar{G}(j\omega)$ has an angle which is the algebraic sum of angles of individual angles.

As mentioned earlier, we use decibel form of the magnitude for the Bode diagram. Note that

$$\begin{aligned} &20 \log [(1 + j\omega/Z_1)(1 + j\omega/Z_2) \ldots (1 + j\omega/Z_m)] \\ &= (1 + j\omega/Z_1)_{dB} + (1 + j\omega/Z_2)_{dB} + \cdots + (1 + j\omega/Z_m)_{dB} \end{aligned} \tag{10.13}$$

Thus, the product terms become sum terms when expressed on dB. Similarly,

$$20 \log \frac{(1 + j\omega/Z_1)}{(1 + j\omega/p_1)} = (1 + j\omega/Z_1)_{dB} - (1 + j\omega/p_1)_{dB} \tag{10.14}$$

Let us define two simple functions:

$$\bar{G}_1(j\omega) = (1 + j\omega/\omega_0); \quad \bar{G}_2(j\omega) = \frac{1}{(1 + j\omega/\omega_0)} \tag{10.15}$$

It will be readily seen from Eq. (10.15) that for $\frac{\omega}{\omega_0} << 1$,

$$|\bar{G}_1(j\omega)| = |\bar{G}_2(j\omega)| = 1$$

Hence
$$G_1(j\omega)_{dB} = G_2(j\omega)_{dB} = 20 \log 1 = 0 \tag{10.16}$$

At very high frequencies ω, we can assume $\omega/\omega_0 >> 1$, and, therefore, Eqs. (10.15) yields (neglecting 1 w.r.t. ω/ω_0)

$$|\bar{G}_1(j\omega)| = \frac{\omega}{\omega_0} \quad \text{and} \quad |\bar{G}_2(j\omega)| = \frac{\omega_0}{\omega}$$

Hence
$$G_1(j\omega)_{dB} = 20 \log \frac{\omega}{\omega_0} \tag{10.17a}$$

$$G_2(j\omega) = -20 \log \frac{\omega}{\omega_0} \tag{10.17b}$$

We have used the notation $|\bar{G}_1(j\omega)| = G_1(j\omega)$ and $|\bar{G}_2(j\omega)| = G_2(j\omega)$ in Eq. (10.17a) and (10.17b).

Equations (10.16) and (10.17) show that at low frequencies ($\omega << \omega_0$ or $\omega/\omega_0 << 1$), the magnitudes G_1, G_2 in dB are zero (and $G_1 = G_2 = 1$ here).

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At $\omega = \omega_0$, $G_1(j\omega)_{dB} = G_2(j\omega)_{dB} = 0$ (10.18a)

At $\omega = 10\omega_0$, $G_1(j\omega)_{dB} = 20$ dB; $G_2(j\omega)_{dB} = -20$ dB (10.18b)

At $\omega = 100\omega_0$, $G_1(j\omega)_{dB} = 40$ dB; $G_2(j\omega)_{dB} = -40$ dB (10.18c)

It is seen that the values of G_1, G_2 in dB increase/decrease by 20 dB for each factor of 10 (decade). The factor of 10 times is linear on logarithmic frequency scale, hence Eqs. (10.18a), (10.18b) and (10.18c) will be straight lines on logarithmic graph, i.e., the Bode plots of Eq. (10.17a) and Eq. (10.17b) will be straight lines with their slopes +20 dB/decade for G_1 and –20dB/decade for G_2. It is also customary to express the slopes of the straight lines in units of dB/octave. Octave means 2 times in frequency. Thus, for $\omega = 2\omega_0$, the values of G_1 and G_2 from Eqs. (10.17a) and (10.17b) will be +6 dB/octave and –6 dB/octave, respectively (Note that 20 log 2 = 6). It may be noted that a slope of 20 dB/decade = a slope of 6 dB/octave and –20 dB/decade = –6 dB/octave.

The phase angles represented by $\bar{G}_1(j\omega)$ and $\bar{G}_2(j\omega)$ are as follows [from Eq. (10.15)]:

$$\angle\bar{G}_1(j\omega) = \tan^{-1}\frac{\omega}{\omega_0} \quad \text{or} \quad \theta_1(\omega) = \tan^{-1}\frac{\omega}{\omega_0} \tag{10.19a}$$

$$\angle\bar{G}_2(j\omega) = -\tan^{-1}\frac{\omega}{\omega_0} \quad \text{or} \quad \theta_2(\omega) = -\tan^{-1}\frac{\omega}{\omega_0} \tag{10.19b}$$

At $\omega = 0$, $\theta_1(\omega) = 0$, $\theta_2(\omega) = 0$ (10.20a)

At $\omega = \omega_0$, $\theta_1(\omega) = 45°$, $\theta_2(\omega) = -45°$ (10.20b)

At $\omega >> \omega_0$, $\theta_1(\omega) = 90°$, $\theta_2(\omega) = -90°$ (10.20c)

In practice, to draw Bode graph (asymptotic diagram), instead of $\omega = 0$, $\omega = 0.1\omega_0$ is taken to draw $\theta_1(\omega) = \theta_2(\omega) = 0$. Rigorously,

$$\tan^{-1}\frac{\omega}{\omega_0} = \tan^{-1}\frac{0.1\omega_0}{\omega_0} = \tan^{-1} 0.1 = 5.7°$$

but we assume $\tan^{-1} 0.1 \approx$ zero. This is a small error in approximation. Similarly, instead of $\omega >> \omega_0$, if we take $\omega = 10\omega_0$ instead of $\omega >> \omega_0$, we take $\theta_1(\omega)$ equal to –90°. Rigorously, when $\omega = 10\omega_0$, we have

$$\tan^{-1}\frac{\omega}{\omega_0} = \tan^{-1}\frac{10\omega_0}{\omega_0} = \tan^{-1} 10 = 84.3°$$

but we assume $\tan^{-1} 10 \approx 90°$ for the plot. This is a small approximation error in phase response. Hence the maximum error in phase characteristic is 5.7°, i.e., at break frequency ($\omega = \omega_0$), the phase error is zero; and at $\omega = 0.1\omega_0$ or $\omega = 10\omega_0$, the phase error is 5.7°.

Various curves in Fig. 10.1 indicate amplitudes and phase responses of $\bar{G}_1$ and $\bar{G}_2$ discussed earlier.

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Phase response curves

$$At\ \omega = 0, \quad \theta(\omega) = \text{Arg}\left.\frac{1 + j\omega/10}{1 + j\omega/50}\right|_{\omega=0} = 0°$$

$$At\ \omega = 10, \quad \theta(\omega) = \text{Arg}\left(\frac{1 + j10/10}{1 + j10/50}\right) = 45° - \tan^{-1}\frac{1}{5} = 45° - 11.3° = 33.7°$$

$$At\ \omega = 50, \quad \theta(\omega) = \text{Arg}\left(\frac{1 + j50/10}{1 + j50/50}\right) = \tan^{-1} 5 - 45° = 78.7 - 45° = 33.7°$$

$$At\ \omega = \infty, \quad \theta(\omega) = \text{Arg}\left(\frac{1 + j\omega/10}{1 + j\omega/50}\right)\Bigg|_{\omega=\infty} = 0 \text{ (by inspection)}$$

As
$$\theta(\omega) = \text{Arg}\left[\frac{(1 + j\omega/10)}{1 + j\omega/50}\right]$$
$$= \text{Arg}\ (1 + j\omega/10) - \text{Arg}\ (1 + j\omega/50)$$
$$= \theta_1(\omega) = \theta_2(\omega)$$

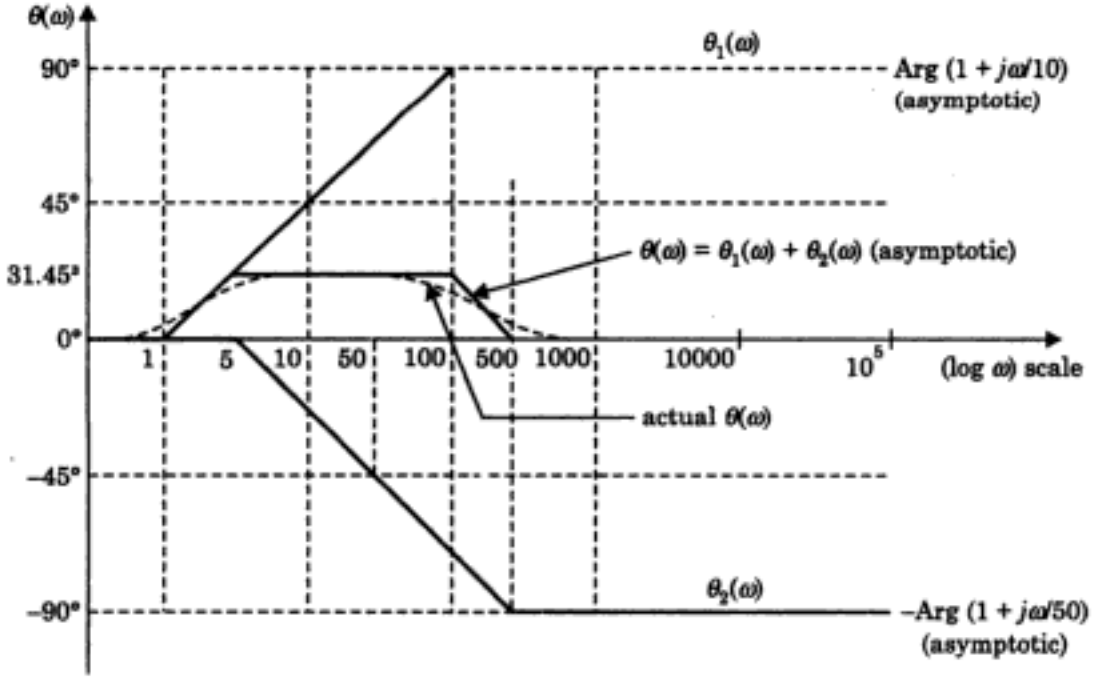


Fig. 10.3 Curves showing phase angles $\theta_1(\omega)$ and $\theta_1(\omega) + \theta_2(\omega)$, Ex. 10.1.

where
$$\theta_1(\omega) = \text{Arg}\ (1 + j\omega/10) \quad = 0, \quad \omega = 0$$
$$= 45°, \quad \omega = 10$$
$$= 90°, \quad \omega = \infty$$
$$\theta_2(\omega) = -\text{Arg}\ (1 + j\omega/50) \quad = 0°, \quad \omega = 0$$
$$= -45°, \quad \omega = 0$$
$$= -90°, \quad \omega = \infty$$

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where $A = 20 \log 100 = 40$ dB constant for all frequencies

$$B = 20 \log \omega \quad \left.\begin{array}{l} at\ \omega = 1,\ \text{gain} = 0\ \text{dB} \\ at\ \omega = 10,\ \text{gain} = 20\ \text{dB} \end{array}\right\}$$

$\therefore$ 20 dB/decade starting from $\omega = 1$, curve B is drawn in Fig. 10.4(a).

$$C = 10 \log \left[1 + \left(\frac{\omega}{20}\right)^2\right] \quad \left.\begin{array}{l} \text{at } \omega = 0,\ \text{gain} = 0\ \text{dB} \\ \text{at } \omega = 20,\ \text{gain} = 3\ \text{dB} \end{array}\right\}$$

Assume gain 0 dB upto $\omega = 20$ for curve C

Now $$C \approx 20 \log \frac{\omega}{20} \text{ for } \omega >> 20$$

$\therefore$ 20 dB/decade starting from $\omega = 20$ for curve C (see Fig. 10.4a)

Now $$D = -10 \log \left(1 + \left(\frac{\omega}{1000}\right)^2\right) \quad \left.\begin{array}{l} at\ \omega = 0, \quad \text{gain} = 0\ \text{dB} \\ at\ \omega = 1000,\ \text{gain} = -3\ \text{dB} \end{array}\right\}$$

(Assume gain 0 dB upto $\omega = 1000$ for curve D)

Now $$D \approx -20 \log \left(\frac{\omega}{1000}\right)^2 \text{ for } \omega >> 1000$$

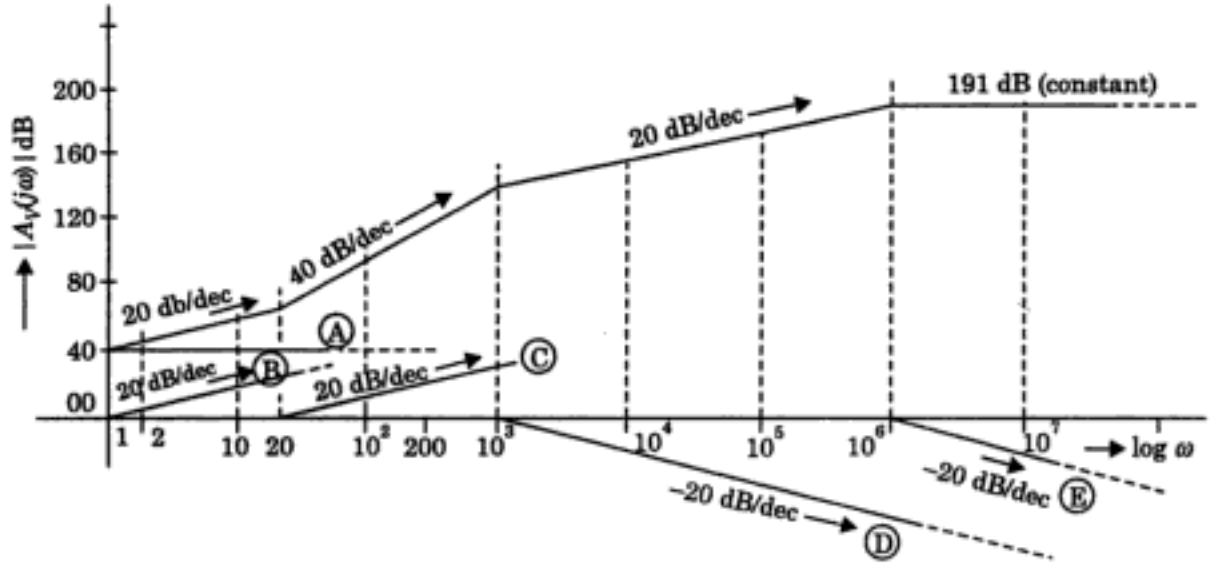
$\therefore$ –20 dB/decade starting from $\omega = 1000$ for curve D (see Fig. 10.4a)

Now$E$ $$= -10 \log \left[1 + \left(\frac{\omega}{10^6}\right)\right]^2 \quad \left.\begin{array}{l} \text{at } \omega = 0,\ \text{gain} = 0\ \text{dB} \\ \text{at } \omega = 10^6,\ \text{gain} = -3\text{dB} \end{array}\right\}$$

(Assume gain 0 dB upto $\omega = 10^6$ for curve E)

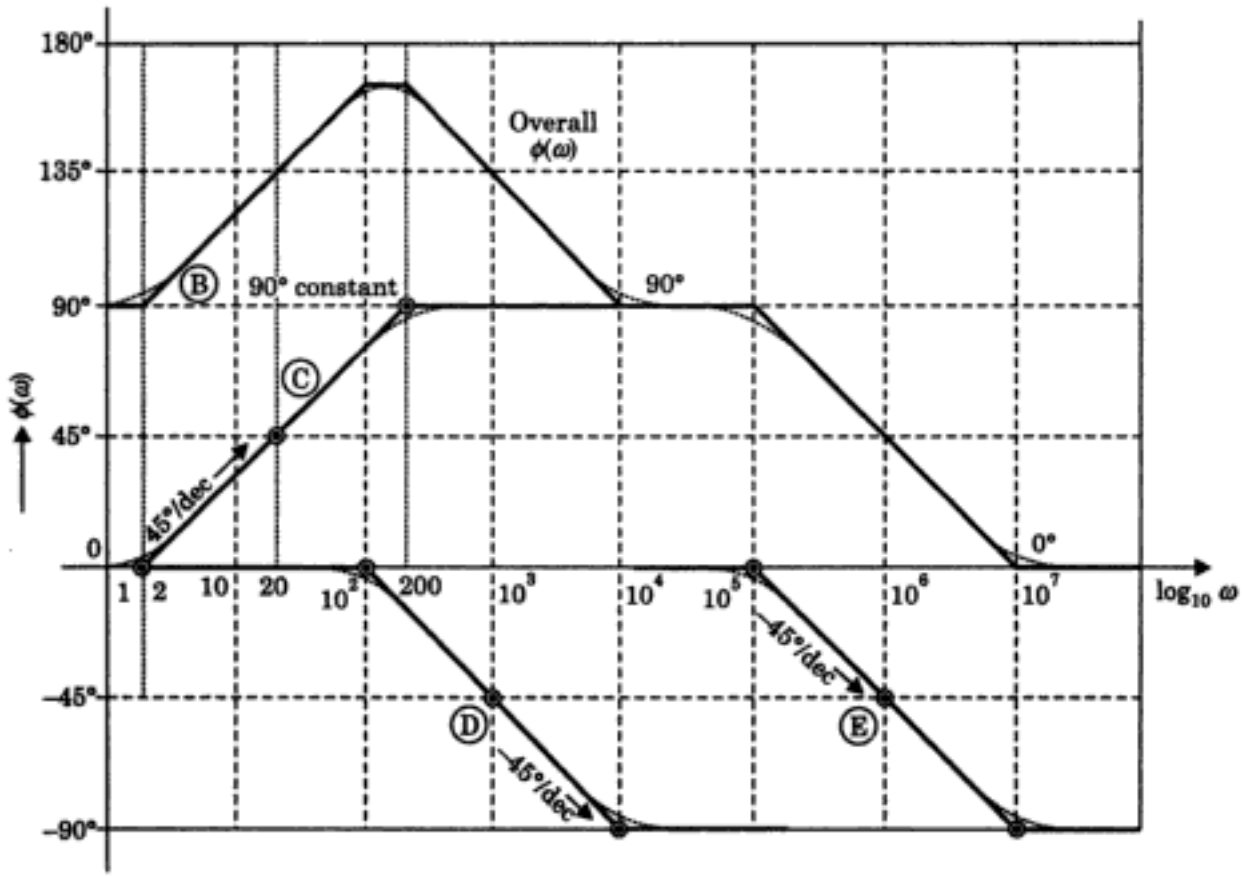
Now $$E = -20 \log \frac{\omega}{10^6}, \omega >> 10^6$$

$\therefore$ –20 dB/decade starting from $\omega = 10^6$, for curve E (see Fig 10.4a)



(a) Amplitude (Gain) $|A_v(j\omega)|$ in dB.

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(b) Phase $\Phi(\omega)$ in degrees.

(B): $\theta_B(\omega) = \tan^{-1}\dfrac{\omega}{0} = 90°$ (constant); (C): $\theta_C(\omega) = \tan^{-1}\dfrac{\omega}{20} \rightarrow 45°$/decade ($\omega$ = 2 to 200)

(D): $\theta_D(\omega) = -\tan^{-1}\dfrac{\omega}{10^3} \rightarrow -45°$/decade ($\omega = 10^2$ to 10^4)

(E): $\theta_E(\omega) = -\tan^{-1}\dfrac{\omega}{10^6} \rightarrow -45°$/decade ($\omega = 10^5$ to 10^7)

Fig. 10.4 (a) Amplitude plot, (b) Phase plot for Ex. 10.2.

10.4 HIGH FREQUENCY RESPONSE (of Lowpass BJT Circuit)

We, now consider the frequency response of the amplifiers for various cases. First we take up the high frequency behaviour of a given circuit with input capacitance.

Consider the equivalent circuit of a typical BJT shown in Fig. 10.5. C_M is the internal capacitance of the amplifying device (e.g. C_π and C_μ for the BJT; C_{gs} and C_{gd} for the FET). R_i is the input impedance of the amplifier. A hybrid-π model will be more useful in the analysis that follows. We aim at determining the value of voltage gain $A_V = V_0/V_1$ at various frequencies.

As
$$C_M \parallel R_i = \frac{(1/sC_M)\,R_i}{(1/sC_M) + R_i} = \frac{R_i}{1 + sR_iC_M} = Z \text{ (say)}$$

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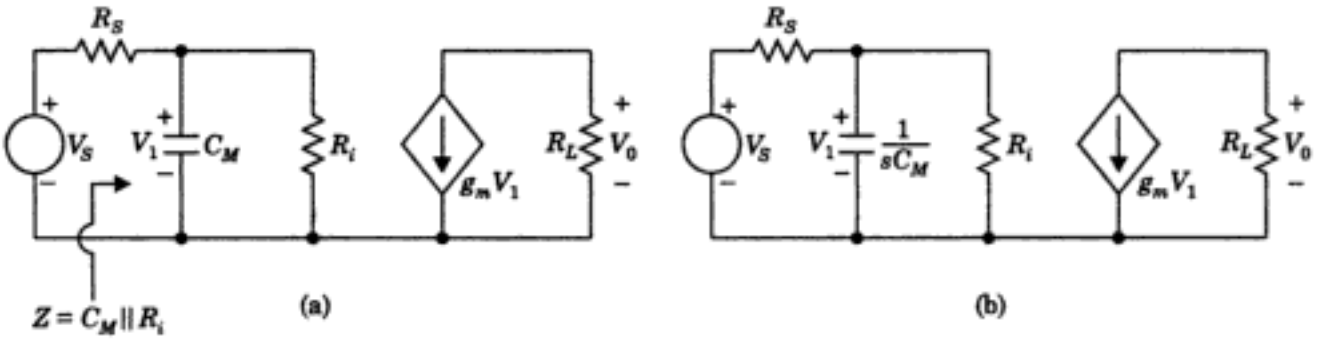


Fig. 10.5 (a) Low-pass circuit of a BJT, (b) The frequency domain (s-plane) representation of circuit in (a).

$$V_1 = V_S \frac{Z}{R_S + Z} = V_S \cdot \frac{R_i /(1 + sC_M R_i)}{R_S + \dfrac{R_i}{1 + sC_M R_i}}$$

i.e.
$$V_1 = \frac{R_i}{(R_S + R_i) + sC_M R_i R_S} V_S \tag{10.21}$$

$$V_0 = -(g_m V_1) R_L$$

$\therefore$
$$\frac{V_0}{V_1} = \frac{-g_m R_i R_L}{(R_S + R_i) + sC_M R_i R_S} \qquad (\because V_1 = V_S) \tag{10.22}$$

Hence
$$A_{VH}(s) = \frac{V_0}{V_1} = \frac{-g_m R_i R_L /(R_S + R_i)}{1 + sC_M \cdot \dfrac{R_i R_S}{R_i + R_S}} = \frac{A_{V0}}{1 + s/\omega_H} \tag{10.23}$$

where A_{V0} is the gain of the circuit at $s = j\omega = 0$, i.e., the DC gain. Clearly,

$$A_{V0} = -g_m R_L R_i/(R_S + R_i)$$

Note: If $R_i = r_\pi$ then $A_{V0} = -\beta R_L/(R_S + r_\pi)$ as for CE mode of a BJT for low frequencies model.

Now,
$$\omega_H = \frac{1}{C_M (R_S \| R_i)}$$

As
$$A_{VH}(s) = \frac{A_{V0}}{1 + s/\omega_H} \tag{10.24}$$

$\therefore$
$$A_{VH}(j\omega) = \frac{A_{V0}}{1 + j\omega/\omega_H} \qquad \text{(putting } s = j\omega\text{)}$$

$$|A_{VH}(j\omega)| = \frac{A_{V0}}{\sqrt{1 + (f/f_H)^2}}\ ;\ A_{V0} = \frac{-g_m R_L R_i}{R_S + R_i} \tag{10.25a}$$

$$\theta_H = -\tan^{-1}\frac{f}{f_H} \tag{10.25b}$$

$$\omega_H = \frac{1}{(R_S \| R_i) C_M} \quad \text{the half power frequency for lowpass BJT circuit} \tag{10.25c}$$

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Note: 1: The input resistance seen by C_M is $R_S \| R_i$. (see Fig. 10.6)

i.e. $$Z' = \frac{R_S R_i}{R_S + R_i}$$

2: $$A_{VH}\Big|_{f \to \infty} = 0$$

3: $$\theta_H\Big|_{f \to \infty} = -\frac{\pi}{2}$$

4: $$\theta_H\Big|_{f = f_H} = -\frac{\pi}{4}$$

5: $$A_{VH}\Big|_{f = f_H} = \frac{1}{\sqrt{2}} A_{V0}$$ (i.e. at $f = f_H$, A_{VH} is 3 dB down)

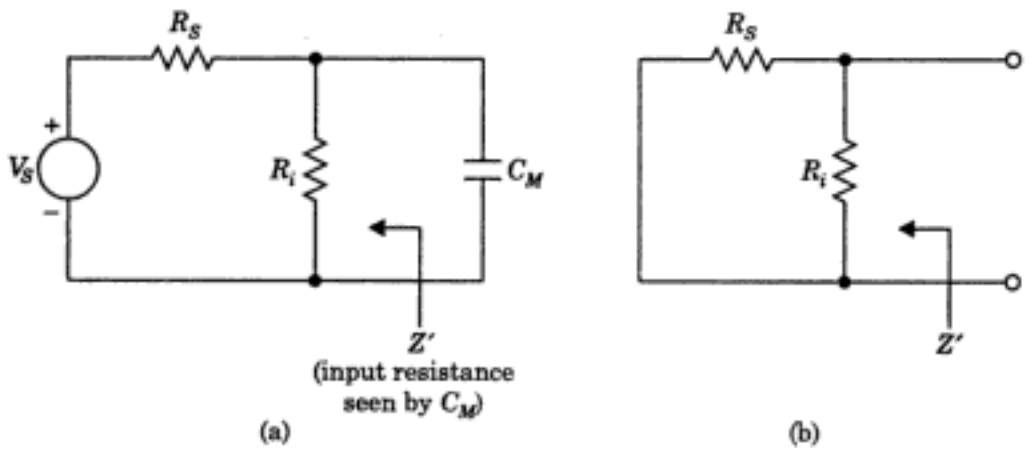


Fig. 10.6 To find resistance seen by C_M. (a) Actual circuit, (b) To get Z', we make $V_S = 0$.

In Bode's diagram, we take

$$\theta_H = -90° \text{ for } \frac{f}{f_H} = 10$$

$$\theta_H = -45° \text{ for } \frac{f}{f_H} = 1$$

$$\theta_H = 0° \text{ for } \frac{f}{f_H} = 0.1$$

Exactly	*For Bode's diagram*
$\tan^{-1} 0.1 = 5.7°$	but we assume 0.0°
$\tan^{-1} 1.0 = 45°$	we take 45° exact
$\tan^{-1} 10.0 = 84.3°$	but we assume 90°

Since, at $f = f_H$, the gain A_{VH} is $1/\sqrt{2}\, A_{V0}$, i.e., $0.707 A_{V0}$ hence, the power (i.e. gain^2) or the decibel reduction of the gain is:

$$20 \log_{10} \frac{A_{VH}}{A_{V0}} = 20 \log_{10} 0.707 = 20 \times -\frac{0.3}{2} = -3 \text{ dB}$$

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Then, f_H is referred to high or upper (3 dB down frequency) *3 dB frequency* or also called upper (high) **half-power frequency.**

In the Bode's diagram, as shown in Fig. 10.7, the asymptotic curves are drawn for relative gain A_{VH}/A_{V0} versus relative frequency f/f_H. Note that as $f \to \infty$, i.e., $s \to \infty$,

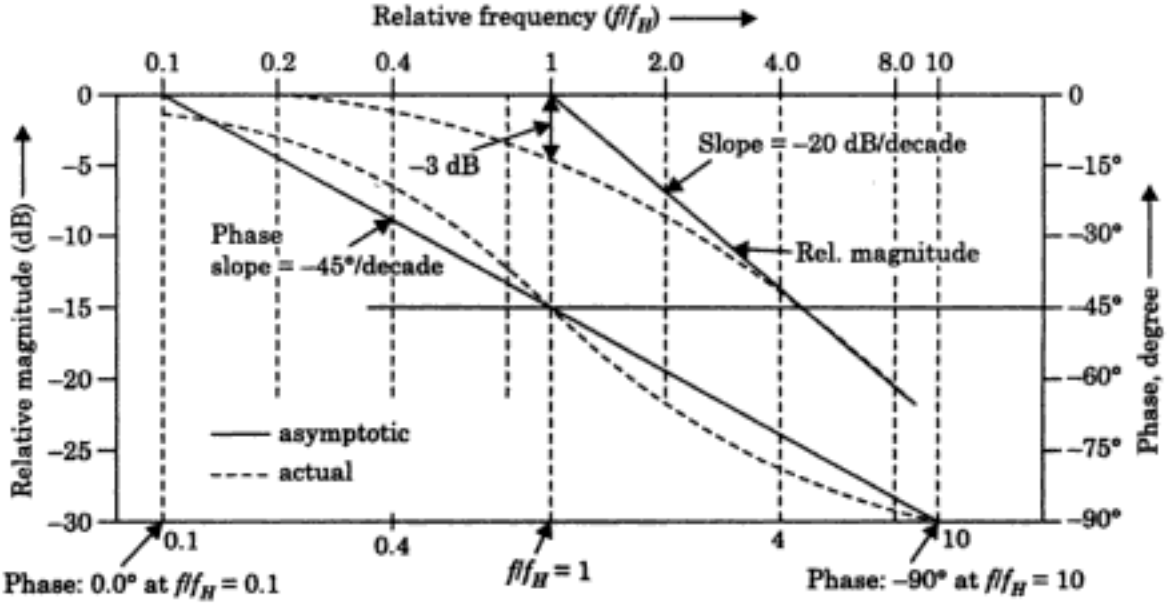


Fig. 10.7 Normalized Bode diagram of the transfer function, given by $A_{VH}(s) = A_{V0}/(1 + s/\omega_H)$ (a low pass filter). *X*-axis is log of normalized frequency given by log (f/f_H)

$$\left.\frac{A_{VH}(s)}{A_{V0}}\right|_{\substack{s\to\infty \\ \therefore \omega\to\infty}} \approx \frac{1}{s/\omega_H} = \frac{\omega_H}{j\omega}$$

$$\therefore \quad \left|\frac{A_{VH}(s)}{A_{V0}}\right|_{\omega\to\infty} = \frac{\omega_H}{\omega}$$

i.e., slope at $\omega \to \infty$ is found as follows:

To find slope of A_{VH}/A_{V0} at asymptote for $\omega \to \infty$

As $$\left.\frac{A_{VH}}{A_{V0}}\right|_{s\to\infty} = \frac{\omega_H}{s} = \frac{\omega_H}{j\omega}$$

$$20 \log_{10} \left|\frac{A_{VH}}{A_{V0}}\right|_{\omega\to\infty} = 20 \log \frac{\omega_H}{\omega}$$

$$= (20 \log_{10} \omega_H - 20 \log_{10} \omega) \text{ dB}$$

Here slope is –20 dB/decade, i.e., as ω increases to 10 times, 20 $\log_{10}$ $|A_{VH}/A_{V0}|$ decreases by 2 dB.

The circuit of Fig. 10.5 is a low-pass filter since at $\omega = 0$, the gain is the highest ($= A_{V0}$) and the gain decreases as ω increases. For example, if

$$C_M = 100 \text{ pF}, R_i = R_S = 1 \text{ k}\Omega$$

$$\therefore \quad R_i || R_S = 0.5 \text{ k}\Omega = 500 \ \Omega$$

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$$\triangleq \frac{A_{V0}}{(1+\omega_L/s)} = \frac{(A_{V0}\, s/\omega_L)}{(1+s/\omega_L)}$$

i.e.,
$$A_{VL}(s) = \frac{V_0}{V_s} = \frac{A_{V0}\dfrac{s}{\omega_L}}{1+\dfrac{s}{\omega_L}} = \frac{A_{V0}}{1+\dfrac{\omega_L}{s}} \tag{10.27a}$$

where
$$\omega_L = \frac{1}{(R_S + R_i)C_C} \quad \text{the half power frequency of highpass BJT circuit} \tag{10.27b}$$

and
$$A_{V0} = -\frac{g_m R_L R_i}{(R_S + R_i)} \tag{10.27c}$$

(A_{V0} is the same as in the high frequency response model see Eq. 10.25a)

Also,
$$|A_{VL}(j\omega)| = \frac{A_{V0}}{\sqrt{1+(f_L/f)^2}}, \quad \theta_L = \tan^{-1}\frac{f_L}{f} \tag{10.28}$$

$$\therefore \quad Arg\,[A_{VL}(j\omega)] = -\tan^{-1}\left(-\frac{\omega_L}{\omega}\right) = \tan^{-1}\left(\frac{f_L}{f}\right)$$

Clearly, $A_{VL} \to 0$ as $f \to 0$ and A_{VL} is maximum at $f \to \infty$.

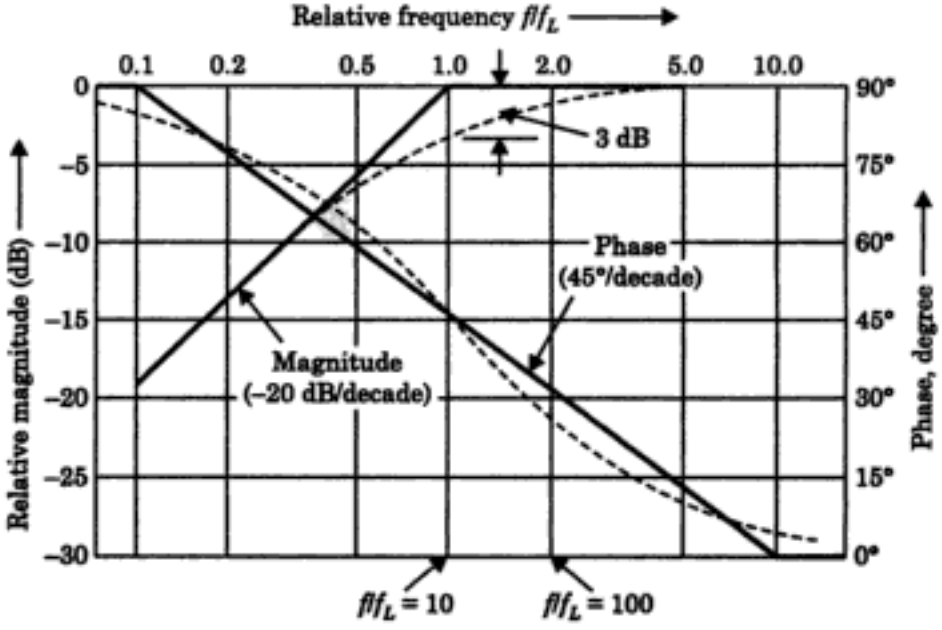


Fig. 10.9 Normalized Bode diagram of the transfer function of the circuit in Fig. 10.8 (high-pass filter). $A_{VH}(s) = A_{V0}/(1 + \omega_L/s)$. X-axis is log of normalized frequency given by log (f/f_L)

This is a high pass filter, therefore for $C_C = 1\ \mu F$, $R_S = R_i = 1\ k\Omega$,

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$$\omega_L = \frac{1}{1\times10^{-6}\times2\times10^{3}} = 500$$

or $$f_L \approx 80 \text{ Hz}$$

The behaviour of this circuit (Fig. 10.8) as a high pass filter is obvious, since at high/higher frequencies the reactance of C_C is quite low and it permits the signal to be fed to the amplifier's input terminal. As $\omega \to 0$, $1/\omega C_C \to \infty$ and here the input signal is completely blocked and $V_0 \to$ zero.

The Bode diagram for the transfer function Eq. (10.27a) is shown in Fig. 10.9. Note that from (10.27a) we have

$$A_{VL}\big|_{s=0} \to 0$$

$$A_{VL}(s)\big|_{s=\infty} = A_{V0}$$

$$A_{VL}(s)\big|_{s=j\omega_L} = \frac{1}{\sqrt{2}} A_{V0} \quad \text{(i.e., half power point)}$$

$$\theta_L\big|_{\omega=\infty} = 0$$

$$\theta_L\big|_{\omega=\omega_L} = 45^\circ$$

$$\theta_L\big|_{\omega=0} = 90^\circ$$

In Bode diagram: $\left(\theta_L = \tan^{-1}\dfrac{\omega_L}{\omega}\right)$, *take*

$\theta_L = 45^\circ$ at $\omega/\omega_L = 1$

$\theta_L = 0^\circ$ at $\omega/\omega_L = 10$

$\theta_L = 90^\circ$ at $\omega/\omega_L = 0.1$

The dotted lines are the actual curves and the asymptotic graph is in continuous/solid lines.

Having determined the behaviour of the amplifier at low and high frequencies, due to C_M and C_C, it is possible to determine the frequency response due to the presence of both C_M and C_C. This is clarified in the next section.

EXAMPLE 10.3

The amplifier shown in Fig. 10.10 is biased at I_D = 1 mA, g_m = 1 m℧. Find the value of C_S that places the corresponding pole at 10 Hz. What is the frequency of the transfer functions zero introduced by C_S?

Solution: C_S causes low frequency gain lower due to reactance of $C_S \to$ high at low frequency

$$\omega_L = \frac{1}{C_S \text{ (Impedance seen by } C_S)}$$

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In IC's, which are invariably direct coupled (i.e. C_C is not there), the low frequency response extends upto $\omega = 0$ i.e. dc and the bandwidth (BW) is simply f_H. Therefore, only the high frequency limitations to amplifiers (for IC cases) response exist, at low frequencies IC do not pose any serious problem.

10.8 PARAMETERS TO DETERMINE RESPONSE TO SQUARE WAVE SIGNALS

In this section, we discuss the step response, rise time, tilt or sag in the response and suggest a methodology for determining the performance of an amplifier. These parameters are very important to judge the response of the amplifiers for square wave type input waveforms. Amplification of given square wave inputs are practically needed in a large number of practical situations.

10.8.1 Step Response of an Amplifier

An alternative criteria of amplifier's fidelity is the response of the amplifier to a particular waveform preferably a step voltage. Once the step input response is known then the response to any arbitrary waveform can be written in terms of step response (by superposition/ convolution integral). Moreover, the step response easily high-lights even small distortions clearly. Also, square-wave generators and step (pulse) generators are commercially readily available, this enables us ready signal required for determining the performance of the amplifier. Note that the voltage gain for an amplifier, represented by a single pole is of the form (see Fig. 10.5)

$$A_V(s) = \frac{A_{V0}}{1 + s/\omega_H} \qquad \text{(From 10.23)}$$

For input step of $V_{in}(s)$,

$$V_0(s) = V_{in}(s) \times A_V(s) \qquad \text{(Recollect: } Y(s) = X(s) \,.\, H(s)\text{)}$$

here

$$\left.\frac{V_0}{V_{in}}\right|_{s=0} = A_V(0) = A_{V0}$$

$$\frac{V_0}{A_{V0} V_{in}} = 1 \quad \text{at } \omega = 0 \quad \text{or} \quad \text{at } t = \infty$$

An amplifier with transfer function $A_V(s)$ having a single pole (and no zero except at $s = \infty$) has the output waveform for the step input as shown in Fig. 10.14. Let us consider

Step input: $V_{in}(t) = Au(t) \Rightarrow A\frac{1}{s}$ (Laplace transform)

System with $H(s) = B \,.\, \frac{1}{s + k}$ (a low pass filter as given by $A_{VH}(s)$)

$\therefore$ Output, $V_{out}(s) = V_{in}(s) \,.\, H(s)$

$\therefore$ $$V_{out}(s) = \frac{AB}{s(s + k)} = \frac{AB}{k}\left[\frac{1}{s} - \frac{1}{s + k}\right]$$

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$$V_0(t) = K_1(1 - e^{-kt})\, u(t) \tag{10.29}$$

where K_1 is a constant equalling AB/k here.

Thus, the output is of the form shown in Fig. 10.14.

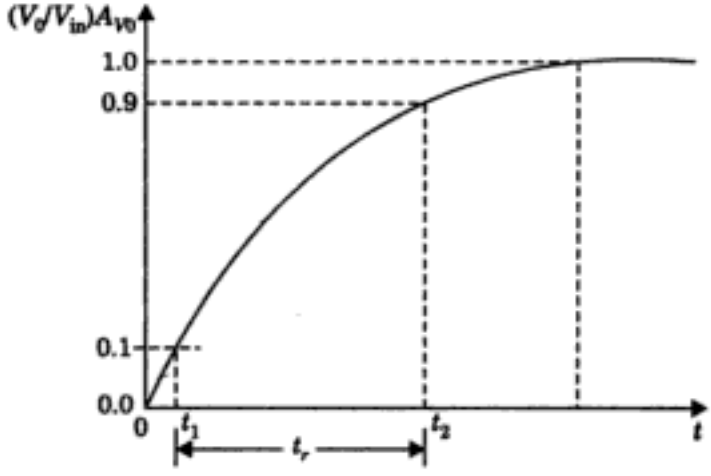


Fig. 10.14 Numerical step response of the circuit of Fig. 10.5.

There continues to be an *intimate relationship* between the *distortion of the leading edge of the step and the high-frequency response*. Similarly, there is a *close relationship* between the *low-frequency response* and the *distortion of the flat portion* of the step. Since an input step is a combination of the most abrupt voltage possible (the leading edge) and the slowest possible voltage variation (the flat portion), thus the step response is an excellent measure of fidelity of the amplifier. Note that the sharp rise of the unit step function $u(t)$ at $t = 0$ amounts to inclusion of all frequencies 0 to ∞ (theoretically, by Fourier transform). Similarly, the $u(t)$ has a constant value equalling unity for $t > 0$. This part of $u(t)$ represents DC. Hence $u(t)$ contains all the frequencies which any practical signal can have.

10.8.2 Rise Time

Let the input $V_{in}(t) = u(t)$, i.e.,

$$V_{in}(s) = \frac{1}{s} \quad \text{(by Laplace transform)}$$

Let the Amplifier's system function be

$$H(s) = A_V(s) = \frac{A_{V0}}{1 + (s/\omega_H)} \quad \text{(From 10.23)}$$

$$\therefore \quad \text{Output } V_0(s) = V_{in}(s) \,.\, A_V(s) = \frac{A_{V0}}{s(1 + s/\omega_H)}$$

or $$V_0(t) = A_{V0}(1 - e^{-\omega_H t})u(t) \quad \text{(as in Eq. 10.29)}$$

where $\omega_H = 1/C_M\,(R_i \| R_S)$ (From Eq. 10.25c)

A_{V0} = Gain at $\omega = 0$ (i.e. for $t = \infty$)

V_S = voltage level of the input = 1 V here (say)

t_1 = Time to reach 0.1 times the final output

t_2 = Time to reach 0.9 times the final output

$$\therefore \quad 1 - e^{-\omega_H t_1} = 0.1 \quad \text{or} \quad e^{-\omega_H t_1} = 0.9 \quad \text{or} \quad \omega_H t_1 = 0.1$$

and $$1 - e^{-\omega_H t_2} = 0.9 \quad \text{or} \quad e^{-\omega_H t_2} = 0.1 \quad \text{or} \quad \omega_H t_2 = 2.3$$

Thus, $$(t_2 - t_1)\omega_H = 2.3 - 0.1 = 2.2$$

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$$\text{Rise time } t_r = \frac{2.2}{\omega_H} = \frac{2.2}{2\pi f_H} = \frac{0.35}{f_H} \tag{10.30}$$

where we have defined the Rise time t_r as follows: (see Fig. 10.15)

Rise time t_r = time for the output to reach from 0.1 to 0.9 times the final value.

Thus, the rise time is inversely proportional to the upper 3-dB frequency (i.e. f_H). Typical value for 1 MHz f_H, $t_r = 0.35$ μs.

For a single-pole circuit, $t_r = 0.35/f_H$ is exact upto three significant figures. For a multiple circuit, the expression $t_r = 0.35/f_H$ is correct within 3 or 4%.

A thumb rule: For a pulse width T_p, we choose an amplifier with high frequency (3 dB) f_H, given by

$$f_H \approx \frac{1}{T_p} \tag{10.31a}$$

Such an amplifier would give a fairly good output and an acceptable level of distortion in the input pulse.

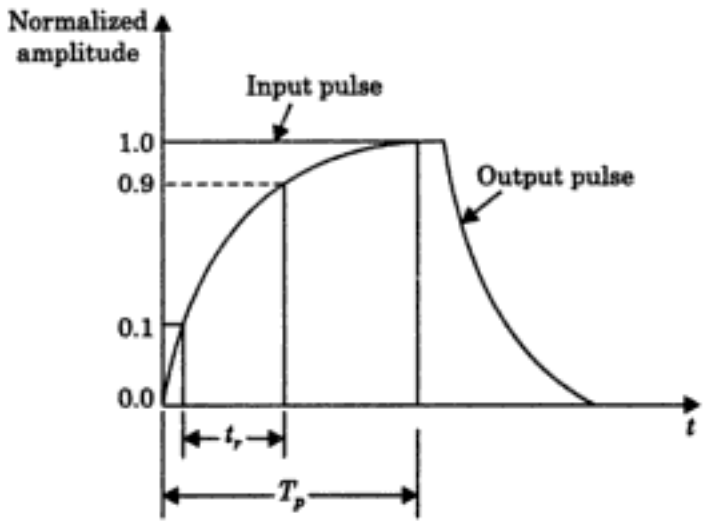


Fig. 10.15 Typical response of a low-pass circuit to a pulse. Rise time to t_r is shown. Note that $t_r = 0.35T_p$.

For radars and sonars where the leading edge is important, since it contains the range (distance) information of the echo, we choose amplifiers with even more broadband, such as

$$f_H = \frac{2}{T_p} \tag{10.31b}$$

This enables us to have

$$t_r \approx \frac{0.175}{(f_H/2)} = 0.175T_p \quad \text{(instead of } 0.35T_p \text{ as in the earlier case)}$$

10.8.3 Tilt or Sag

Consider a high pass filter with Transfer function (TF) (see Fig. 10.8)

$$H(s) = A_{V0}\frac{s/\omega_L}{1 + s/\omega_L} \quad \text{(From Eq. (10.27a))}$$

where $$\omega_L = \frac{1}{(R_S + R_i)C_C} \quad \text{(From Eq. (10.27b))}$$

For input,

$$v_s(t) = V_s u(t) \equiv \frac{V_s}{s} \quad \text{(Laplace transform of } v_s(t))$$

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and $$\omega_L = \frac{1}{100 \times 10^{-3}} = 10 \text{ rads/s}$$

with the input wave time period $T = 0.4 \times 10^{-6}$ s

and $$f = \frac{1}{T}$$

$$= \frac{1}{0.4 \times 10^{-6}} = 2.5 \times 10^{+6}$$

From Eq. (10.35d), we have

$$\%\text{age tilt} \quad P = \frac{\pi f_L}{f} \times 100 = \frac{\omega_L}{2f} \times 100 = \frac{10}{2 \times 2.5 \times 10^6} \times 100 = 0$$

The given amplifier would show no tilt (or almost zero tilt).
From Eq. (10.30),

$$\text{Rise time } t_r = \frac{2.2}{\omega_H} = \frac{2.2}{10 \times 10^6} = 0.22 \times 10^{-6}$$

As t_r is comparable to T, the rising/leading edge of the input would be rounded. There is a need to decrease rise time t_r. If T of the input pulse is 20 μs, however, then for this case, we have

Then $$f = \frac{1}{T} = 50 \text{ Hz}$$

Here, $$\text{Tilt } P = \frac{\omega_L}{2f} \times 100 = \frac{10}{2 \times 50} \times 100 = 10\% \quad \text{(visible on the oscilloscope)}$$

As $t_r = 0.22 \times 10^{-6}$ is much smaller than T, the leading edge would not be distorted.

The frequency characteristics are, in general, *more useful* since:

1. Analysis/synthesis results in frequency domain are much more known.
2. By knowing steady state response, the circuit behaviour can be qualitatively understood.
3. Compensation against oscillations is accomplished in frequency domain, so the analysis in frequency domain indicates where the compensation is needed.
4. In general, the requirements/specifications of an amplifier are defined in frequency domain. The commercial data also gives specifications in terms of frequency response.

With the computers and a number of useful softwares available, it is also possible to perform more rigorous analysis of the given circuit/amplifier. Facilities available in PSPICE and MATLAB may also be gainfully exploited for determining the frequency response of the gadget/amplifier under test.

In the following few sections, we determine the high frequency response of BJT and FET amplifiers in various configurations. It will be appropriate to discuss the common emitter configuration first. Note that we have preferred hybrid-π model. Here $h_{ie} = r_\pi$ and $h_{fe} = \beta_0$.

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$$= \frac{\beta_0(1 - sC_\mu / g_m)}{1 + sr_\pi(C_\pi + C_\mu)}$$

Put $$r_\pi(C_\pi + C_\mu) = \frac{1}{\omega_\beta}$$

and $$\frac{C_\mu}{g_m} = \frac{1}{\omega_Z}$$

$$\therefore \quad \beta(s) = \beta_0 \frac{1 - s/\omega_Z}{1 + s/\omega_\beta} \tag{10.40a}$$

where, zero frequency $$\omega_Z = \frac{g_m}{C_\mu} \tag{10.40b}$$

bandwidth $$\omega_\beta = \frac{1}{r_\pi(C_\pi + C_\mu)} \tag{10.40c}$$

$$\beta_o = g_m r_\pi \tag{10.40d}$$

ω_Z is called the **zero frequency**. If $s = \omega_Z$ then $\beta(s) = 0$. Thus, the generic current gain, $\beta(s)$ is a function of frequencies.

Note: We can find $\omega_Z = g_m/C_\mu$ directly from Fig. 10.18. If $\beta(s) = 0$ then $I_0 = 0$ and

$\therefore$ $$I_\mu = g_m V_\pi$$

i.e., $$sC_\mu V_\pi = g_m V_\pi$$

i.e., $$s = \frac{g_m}{C_\mu}$$

Thus, at $s = g_m/C_\mu$, $\beta(s) = 0$, i.e., $s = g_m/C_\mu = \omega_Z$ gives a zero of $\beta(s)$.

10.9.1 The Parameter f_T (Terminal Frequency)

We define a frequency f_T such that the short circuit current gain $|\beta(2\pi f_T)|$ is unity. The asymptotic characteristics in Bode's graph give highly accurate result for the unity gain frequency f_T because of the wide separation of ω_β and ω_Z in general. (Note that at $s = \omega_Z$, $\beta(s) = 0$ and at $s = j\omega = \omega_\beta$, the short circuit current gain $|\beta(j\omega)|$ has a value equalling $\beta_0/\sqrt{2}$).

In general, for the amplifier to have gain ≥ 1, the frequency ω must be much less than ω_T. If $\omega << \omega_Z, \omega_T$ then the equation

$$\beta(s) = \frac{\beta_0(1 - s/\omega_Z)}{1 + s/\omega_\beta} \qquad \text{[Eq. (10.40a)]}$$

reduces to $$\beta(s) \approx \frac{\beta_0}{1 + s/\omega_\beta} \qquad (\text{if } \omega << \omega_T \text{ or } \omega << \omega_Z) \tag{10.41}$$

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The assumption $s/\omega_Z << 1$ implies $|s| << \omega_Z$

i.e. $$s << \frac{g_m}{C_\mu} \qquad \left(\because \omega_Z = \frac{g_m}{C_\mu}, \text{ from Eq. (10.40b)}\right)$$

$$\therefore \quad g_m >> sC_\mu$$

or $$g_m V_\pi >> sC_\mu V_\pi$$

or $$g_m V_\pi >> I_\mu \qquad (\because \; sC_\mu V_\pi = I_\mu \text{ see Fig. 10.18})$$

If $I_\mu << g_m V_\pi$, the asymptotic Bode diagram for the Eq. (10.40a) is identical to that of Eq. (10.41). Thus, to find f_T, at which the *CE* short circuit current gain has unit magnitude, Eq. (10.41) can be used. We calculate ω_T (= $2\pi f_T$) as follows:

As $$\beta(s) = \frac{\beta_0}{1 + s/\omega_\beta}$$

If $\beta(j\omega_T)$ is unity then we have

$$\therefore \quad |\beta(j\omega_T)| = 1 = \frac{\beta_0}{\sqrt{1 + (\omega_T/\omega_\beta)^2}}$$

or $$1 + (\omega_T/\omega_B)^2 = \beta_0^2$$

$$\therefore \quad \omega_T = \beta_0 \omega_\beta \quad \text{for } \beta_0 >> 1 \text{ (as is usual)}$$

Hence $$\omega_T = \beta_0 \omega_\beta \qquad (10.42)$$

or $$f_T = \beta_0 f_\beta$$

where β_0 is dc gain and f_β is 3 dB bandwidth

Now, $$\omega_\beta = \frac{1}{r_\pi (C_\pi + C_\mu)}$$

$$\therefore \quad f_T = \frac{\beta_0}{2\pi r_\pi (C_\pi + C_\mu)} = \frac{g_m}{2\pi (C_\pi + C_\mu)} \qquad (\because \; \beta_0/r_\pi = g_m)$$

Unit gain frequency: $\omega_T = \dfrac{g_m}{(C_\pi + C_\mu)}$; $f_T = \omega_T / 2\pi$ (10.43a)

For $C_\mu << C_\pi$, $\omega_T \approx \dfrac{g_m}{C_\pi}$ (10.43b)

Thus, the parameter ω_T (and, therefore, f_T) in BJT depends on the operating conditions of the device since $g_m \approx \dfrac{I_{CQ}}{V_T}$. Typically, f_T varies with quiescent collector current as shown in Fig. 10.19. However, for higher currents I_{CQ}, the terminal frequency f_T decreases.

It may be seen that $\beta(0) = \beta_0$ from Eq. (10.41) and also $|\beta(j\omega_\beta)| = \beta_0/\sqrt{2}$, i.e., the low frequency 3 dB bandwidth, is 0 to ω_β radians, or f_β = 3 dB Bandwidth in Hz.

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Given $\beta(0) = \beta_0 = 160$

Assuming $\omega_Z >> \omega_\beta$, which is usually valid, we can write

$$|\beta(j\omega)|^2 = \frac{\beta_0^2}{1 + \omega^2/\omega_\beta^2}$$

or
$$(8)^2 = \frac{160^2}{1 + (2\pi \times 50 \times 10^6)^2 / \omega_\beta^2}$$

($\because$ at $\omega = 2\pi \times 50 \times 10^6$, gain = 8, given)

or
$$1 + \frac{100^2 \times 10^{12}\, \pi^2}{\omega_\beta^2} = \frac{160^2}{64} = 400$$

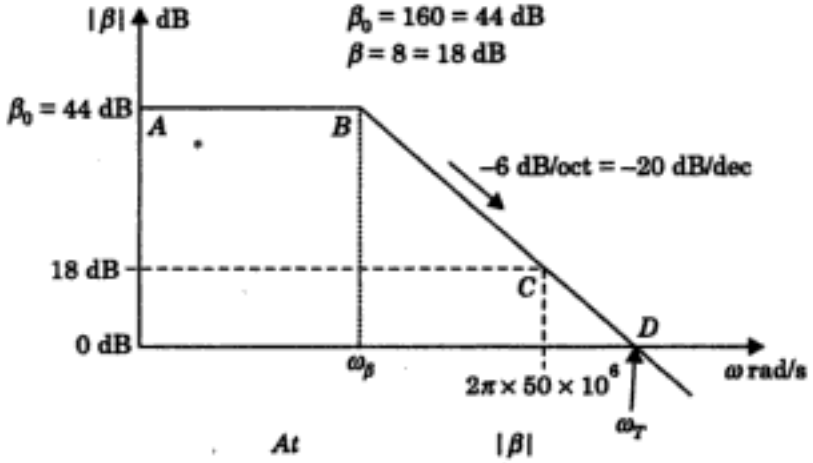
or
$$2\pi \times 50 \times \frac{10^6}{\omega_\beta} = \sqrt{400 - 1} = 19.9749$$

or
$$\omega_\beta = \frac{2\pi \times 50 \times 10^6}{19.9749} = (2\pi \times 2.5) \times 10^6$$

or
$$f_\beta = \frac{\omega_\beta}{2\pi} = 2.5 \text{ MHz} \quad \textbf{Ans.}$$

$$f_T = \beta_0 f_\beta = 160 \times 2.5 = 400 \text{ MHz} \quad \textbf{Ans.}$$

Determination of ω_T by Bode diagram is also possible as shown in Fig. 10.20.



At	|β|
$\omega = 2\pi \times 50$;	18 dB
$\omega = 2\pi \times 100$;	12 dB
$\omega = 2\pi \times 200$;	6 dB
$\omega = 2\pi \times 400$;	0 dB

Fig. 10.20 Bode diagram, used to compute ω_T for Ex. 10.4

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Theorem: The number of poles in a transfer function is equal to the number of independent energy-storing elements in the network.

In electronic amplifiers, the storing elements are almost exclusively capacitors. *An independent capacitor* is one to which we can assign an arbitrary voltage, independent of all other capacitor voltages. Note that:

(i) two capacitors in parallel (see Fig. 10.21) are not independent, as the voltage across the first capacitor C_1 must be the same as that across the second capacitor C_2, i.e., $V_{C1} = V_{C2} = V$. In fact, C_1 parallel to $C_2 = C_1 + C_2$ (only one capacitor).

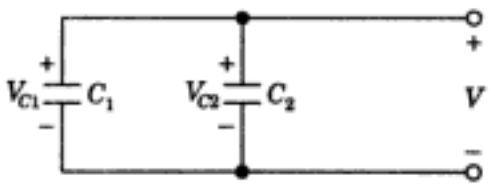


Fig. 10.21 Capacitors in parallel. C_1 and C_2 are not independent.

(ii) two capacitors in series (see Fig. 10.22) are not independent because the charge Q stored is the same in each capacitor.

$$\left(\because \text{ for two capacitors in series } i = \frac{dQ_1}{dt} = \frac{dQ_2}{dt} \therefore Q_1 = Q_2\right)$$

In fact C_1 series $C_2 = \dfrac{C_1 . C_2}{(C_1 + C_2)}$, i.e., only one capacitor.

(iii) If a network loop can be traversed by passing only through capacitors (see Fig. 10.23) then not all of these capacitors are independent, because the sum of the voltages around the closed path must be zero. In Fig. 10.23, the effect of three capacitors will be that of the capacitors which contribute to poles and zeros.

If a function $A(s)$ is such that $A(s)\big|_{s\to\infty} = \dfrac{k}{s^{n-m}}$, $n > m$, then $A(s)$ has n-m zeros at $s = \infty$, i.e., $A(s)$ has $(n - m)$ zeros which are not finite. The voltage across a capacitor is zero at $s \to \infty$ $\left(\because \dfrac{1}{sC} \to 0 \text{ at } s \to \infty\right)$.

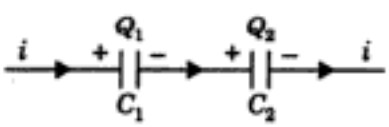


Fig. 10.22 Capacitors in series are not independent $i = \dfrac{dQ_1}{dt} = \dfrac{dQ_2}{dt}$, $\therefore Q_1 = Q_2$.

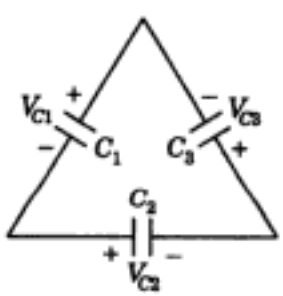


Fig. 10.23 Three capacitors in a mesh are not all independent $\because V_{C3} = -(V_{C1} + V_{C2})$ here.

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$$p_1 \approx \frac{1}{a_1}$$

$$p_2 \approx \frac{a_1}{a_2}$$

$$p_3 \approx \frac{a_2}{a_3}$$

$$\vdots \quad \vdots \qquad \text{if } p_1 \text{ is the dominant pole}$$

$$p_k \approx \frac{a_{k-1}}{a_k} \qquad \text{(i.e. recursive form)} \tag{10.51}$$

The importance of Eq. (10.51) is that we can easily approximate the pole locations by knowing the coefficients a_i in $A_H(s)$. Moreover, the dominant, pole approximation gives the 3 dB frequency f_H as:

$$f_H \approx f_{p1} = \frac{1/a_1}{2\pi} = \frac{1}{2\pi a_1} \tag{10.52}$$

Equation (10.51), i.e., $p_k = a_{k-1}/a_k$, applies to any transfer function of n real poles. In practice, we are interested only in $p_1(= 1/a_1)$ and $p_2(= a_1/a_2)$. The pole p_1 determines the approximate values of f_H (as $f_H \approx p_1/2\pi$) and the separation between p_1 and p_2 indicates the degree to which the dominant-pole approximation is valid.

If, for example, p_2/p_1** ≥ 8, the dominant-pole approximation yields f_H within 10% and p_1 within 20% of their actual values. Note that the dominant-pole approximation *always* results the values of f_H and p_1 that are less than the actual values.

By using 'constant-time response' method, the coefficients a_i can be determined, which in turn permit the circuit designer to correlate the overall response with the particular components (stages) which produce the response.

**suppose $p_1 = 1$ and $p_2 = 8p_1 = 8$. Then if we use only p_1 (and ignore p_2),

$$A_{v1}^2 = \frac{1}{1+1} = \frac{1}{2} \text{ at } s = p_1, \text{ i.e., } A_{V1} = 1/\sqrt{2}$$

Taking both poles gives us, for $s = p_1$

$$A_{V2} = \left(\frac{1}{(1+1)(1+(1/8)^2)}\right)^{1/2} = 0.7016$$

Hence error $\approx \dfrac{1/\sqrt{2} - 0.7016}{1/\sqrt{2}} = 0.08$, i.e., 8% only.

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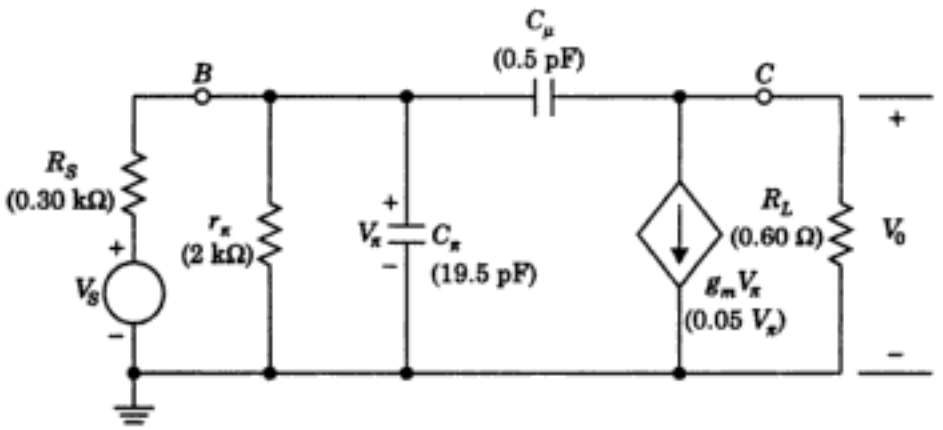


Fig. 10.24 The high-frequency circuit of the basic *CE* stage with load R_L. The hybrid-π model has been used (same as Fig. 10.18) with typical values shown in brackets.

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$$V_\pi\left(\frac{1}{R_S}+\frac{1}{r_\pi}+sC_\pi+sC_\mu\right)-sC_\mu V_0=\frac{V_S}{R_S} \tag{10.53}$$

$$V_\pi(g_m-sC_\mu)+V_0\left(\frac{1}{R_L}+sC_\mu\right)=0 \tag{10.54}$$

To eliminate V_π from Eqs. (10.53) and (10.54)
From Eq. (10.54),

$$V_\pi=-\frac{V_0}{g_m-sC_\mu}\left(\frac{1}{R_L}+sC_\mu\right)$$

Using this value of V_π in Eq. (10.53), we get

$$-\frac{V_0}{g_m-sC_\mu}\left(\frac{1}{R_L}+sC_\mu\right)\underbrace{\left(\frac{1}{R_S}+\frac{1}{r_\pi}\right)}_{=1/R_\pi^0}+sC_\pi+sC_\mu\Big)-sC_\mu V_0=\frac{V_S}{R_S}$$

$$\therefore\quad -V_0\left[\left(\frac{1}{R_L}+sC_\mu\right)\left(\frac{1}{R_\pi^0}+sC_\pi+sC_\mu\right)+sC_\mu(g_m-sC_\mu)\right]=(g_m-sC_\mu)\frac{V_S}{R_S}$$

$$\text{or}\quad -\frac{V_0}{V_S}\cdot\frac{R_S}{g_m}\left[\frac{1}{R_L}\cdot\frac{1}{R_\pi^0}+s\left\{\frac{C_\pi+C_\mu}{R_L}+\frac{C_\mu}{R_\pi^0}+C_\mu g_m\right\}+s^2\{C_\mu(C_\mu+C_\pi)-C_\mu^2\}\right]=\left(1-\frac{sC_\mu}{g_m}\right)$$

$$\therefore\quad -\frac{V_0}{V_S}\left[\frac{R_S}{g_m R_L R_\pi^0}+\frac{R_S}{g_m}s\left\{\frac{R_\pi^0(C_\pi+C_\mu)+R_L C_\mu+R_L R_\pi^0 C_\pi g_m}{R_L R_\pi^0}\right\}+\frac{R_S}{g_m}s^2C_\mu C_\pi\right]$$

$$=\left(1-\frac{sC_\mu}{g_m}\right) \tag{10.54a}$$

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$$R_\pi^0(1+g_mR_L)C_\mu = 0.26\times10^3\times31\times0.5\times10^{-12} = 4.03\times10^{-9}$$

$$R_LC_\mu = 0.6\times10^3\times0.5\times10^{-12} = 0.3\times10^{-9}$$

$$\frac{C_\mu}{g_m} = \frac{0.5\times10^{-12}}{0.05} = 10^{-11}$$

$\therefore$ $$a_1 = R_\pi^0C_\pi + R_\pi^0(1+g_mR_L)C_\mu + R_LC_\mu$$

$$= (5.086 + 4.03 + 0.3)\times10^{-9} = 9.416\times10^{-9} \text{ seconds}$$

$$a_2 = R_\pi^0R_LC_\pi C_\mu$$

$$= 0.26\times10^3\times0.6\times10^3\times19.5\times10^{-12}\times0.5\times10^{-12}$$

$$= 1.521\times10^{-18}\ s^2.$$

If we approximate by dominant pole method then

$$A_{VH}(s) = \frac{A_{V0}(1-10^{-11}s)}{1+(9.416\times10^{-9})s+(1.521\times10^{-18})s^2}$$

$\therefore$ $\frac{1}{\omega_{Z1}} = 10^{-11}$, $a_1 = 9.416\times10^{-9}$, $a_2 = 1.521\times10^{-18}$, and we get

$$p_1 \approx \frac{1}{a_1} = \frac{10^9}{9.416} = 10.6\times10^7 \text{ rad/s}$$

$$p_2 \cong \frac{a_1}{a_2} = \frac{9.416\times10^{-9}}{1.521\times10^{-18}} = 6.19\times10^9 \text{ rad/s}$$

Separation $\frac{p_2}{p_1} = \frac{6.19\times10^9}{(10.6\times10^7)} = 58.4$ (which is greater than 8)

Therefore, the dominant-pole approximation would hold well. The zero, $Z_1 = \frac{1}{10^{-11}} = 10^{11}$ rad/s and is even farther than p_2. Thus, the dominant pole is p_1 and the overall $BW \approx f_H = \frac{p_1}{2\pi}$

$= \frac{10.6\times10^7}{2\pi} = 16.87\times10^6$ Hz $\approx$ 16.9 MHz.

It may be mentioned that the determination of the poles in the denominator of $A_{VH}(s)$ by solving the quadratic equation in the denominator in (10.55) gives $p_1 = 10.7\times10^7$, $p_2 = 6.06\times10^9$ rad/s and f_H is calculated from the T.F. Eq. (10.55) gives $f_H = 17.1$ MHz. These results demonstrate the validity of the dominant-pole method.

The dominant-pole method, in general, is very simple to adopt though there is an error of about 10%. Even the discrete components (R and C) used in the circuit have a tolerance of 10%. Hence an error of ±10% is acceptable in practice.

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$$\therefore \quad V = IR_1 + (I + g_m V_\pi)R_L$$
$$= IR_1 + IR_L + g_m(IR_1)R_L \qquad (\because\ v_\pi = IR_1)$$
$$= I[R_1 + (1 + g_m R_1)R_L]$$

$$\therefore \quad R_\mu^0 = \frac{V}{I} = R_1 + (1 + g_m R_1)R_L = R_L + (1 + g_m R_L)R_1$$

$$\therefore \quad \boxed{\begin{aligned} R_\mu^0 &= (1 + g_m R_L)R_\pi^0 + R_L \\ &= R_\pi^0 + R_L + g_m R_\pi^0 R_L \end{aligned}} \qquad (10.58)$$

The results of Equations (10.57) and (10.58) will prove very handy in analysis.

Notation: R_x^0 (or R_{xx}^0) means impedance seen by capacitor C_x by open circuiting all other capacitors in the circuit.

Also, R_x^y means impedance seen by C_x with capacitance C_y short circuited, and the remaining capacitors (i.e. other than C_x, C_y) open circuited.

EXAMPLE 10.6

(a) Determine the high-frequency output impedance $Z_0(s)$ of a common-emitter stage. Assume $r_0 \to \infty$, but use the hybrid π model, (b) Repeat (a) for $r_0 < \infty$.

Solution: (a) Assuming $r_0 \to \infty$,

$$R_L = R_C \| r_0 = R_C$$

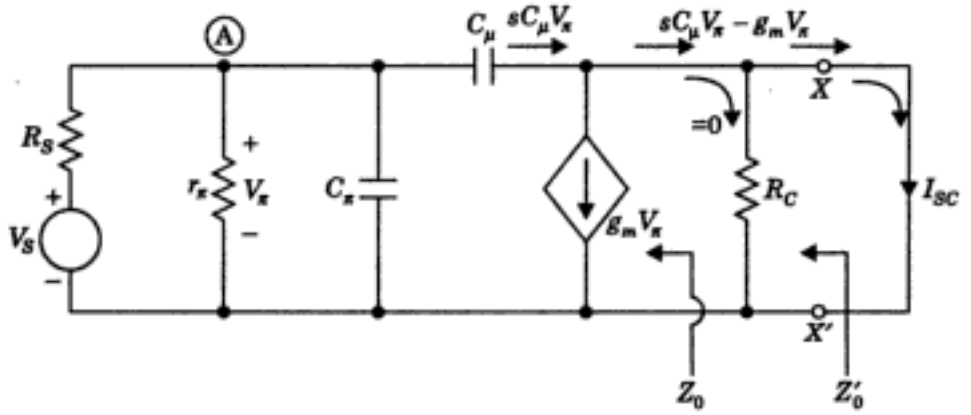


Fig. 10.28 The high-frequency, hybrid π-model of a *CE* stage (see also Fig. 10.24). Ex. 10.6.

Substituting $R_L = R_C$ in Eq. (10.55), we get

$$A_{VH}(s) = \frac{V_0}{V_S} = \frac{[-\beta_0 R_C/(R_S + r_\pi)](1 - sC_\mu/g_m)}{1 + s[R_\pi^0 C_\pi + R_\pi^0(1 + g_m R_C)C_\mu + R_C C_\mu] + s^2 R_\pi^0 R_C C_\pi C_\mu} \qquad (i)$$

where $$R_\pi^0 = R_S \| r_\pi = \frac{R_S r_\pi}{R_S + r_\pi}$$

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We find I_{SC} by shorting XX' as shown in Fig. 10.28, then $Z_0' = \dfrac{V_o}{I_{SC}}$.

If we short XX' then

$$I_{SC} = -g_m V_\pi + sC_\mu V_\pi \tag{ii}$$

KCL at Node A gives us

$$V_\pi \underbrace{\left[\frac{1}{r_\pi} + \frac{1}{R_S}\right]}_{=1/R_\pi^0} + s(C_\pi + C_\mu) - \frac{V_S}{R_S} = 0$$

$$\therefore \quad V_\pi = \frac{V_S \dfrac{R_\pi^0}{R_S}}{[1 + s(C_\pi + C_\mu)R_\pi^0]} \tag{iii}$$

From Eqs. (ii) and (iii),, $\quad I_{SC} = \dfrac{-(g_m - sC_\pi) \times V_S R_\pi^0}{[R_S(1 + s(C_\pi + C_\mu)R_\pi^0)]}$

$$\therefore \quad I_{SC} = -\frac{V_S \beta_0 (1 - sC_\mu / g_m)}{(R_S + r_\pi)[1 + sR_\pi^0(C_\pi + C_\mu)} \qquad \left(\because \frac{R_\pi^0 g_m}{R_S} = \frac{R_S\, r_\pi\, g_m}{R_S(R_S + r_\pi)} = \frac{\beta_0}{(R_S + r_\pi)}\right) \tag{iv}$$

Dividing Eq. (i) by Eq. (iv)

$$Z_0' = \frac{V_{TH}}{I_{SC}} = \frac{-\beta_0 R_C (1 - sC_\mu / g_m)/[(R_S + r_\pi)\{1 + s(R_\pi^0 C_\pi + R_\pi^0(1 + g_m R_C)C_\mu + R_C C_\mu) + s^2 R_\pi^0 C_\pi C_\mu\}}{-\beta_0 (1 - sC_\mu / g_m)/(R_s + r_\pi)(1 + sR_\pi^0(C_\pi + C_\mu))}$$

$$= \frac{R_C[1 + sR_\pi^0(C_\pi + C_\mu)]}{1 + s[R_\pi^0 C_\pi + R_\pi^0(1 + g_m R_C)C_\mu + R_C C_\mu] + s^2 C_\pi C_\mu R_\pi^0 R_C} \tag{v}$$

Denominator of Eq. (v) = $R_C[sC_\mu(1 + g_m R_\pi^0 + sR_\pi^0 C_\pi)] + 1 + sR_\pi^0(C_\pi + C_\mu)$

$\therefore$ Equation (v) can be put in the form:

$$Z_0' = \frac{R_C[1 + sR_\pi^0(C_\mu + C_\pi)]/[sC_\mu(1 + g_m R_\pi^0 + sR_\pi^0 C_\pi)]}{R_C + [1 + sR_\pi^0(C_\mu + C_\pi)]/[sC_\mu(1 + g_m R_\pi^0 + sR_\pi^0 C_\pi)]}$$

$$= \frac{R_C Z_0}{R_C + Z_0}$$

where $\quad Z_0 = \dfrac{1 + sR_\pi^0(C_\mu + C_\pi)}{sC_\mu(1 + g_m R_\pi^0 + sR_\pi^0 C_\pi)}$ **Ans.**

(b) When $r_0 < \infty$ then R_C is parallel with r_0. Therefore, we change

$$R_C \text{ to } R_L = R_C \| r_0$$

Then $\quad Z_0' = R_L \| Z_0 = R_C \| r_0 \| Z_0$

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'Z_0' here is $r_0 \| (Z_0$ of part (a))

i.e. $$Z_0 = r_0 \| \frac{1 + sR_\pi^0(C_\mu + C_\pi)}{sC_\mu(1 + g_m R_\pi^0 + sR_\pi^0 C_\pi)}$$ **Ans.**

10.13 COMMON EMITTER CONFIGURATION, ALTERNATE ANALYSIS APPROACH (The Unilateral Hybrid-π Equivalent for *CE*)

In the CE stages, the poles p_1 and p_2 are usually widely separated. We, therefore, use a single dominant-pole as a good approximation of the frequency response, i.e.,

$$A_{VH}(s) = \frac{A_{V0}}{1 + s/p_1}$$

$$= \frac{A_{V0}}{1 + a_1 s} = \frac{A_{V0}}{1 + s/(2\pi f_H)} \tag{10.59}$$

By using Miller's theorem, we redraw the circuit in Fig. 10.24 as shown in Fig. 10.29.

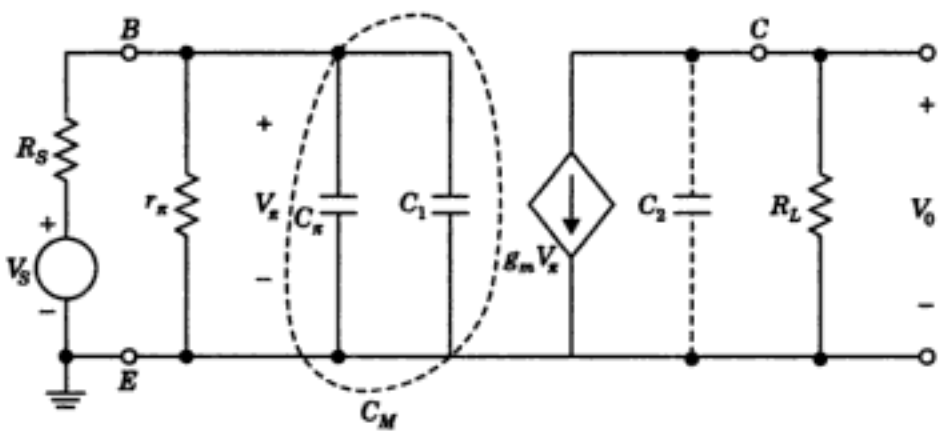


Fig. 10.29 The unilateral hybrid equivalent circuit obtained by the use of Miller theorem. (Fig. 10.24 redrawn by using Miller's theorem)

Let $$K = \frac{V_0}{V_{in}} \simeq -g_m R_L$$

$\therefore$ $$C_1 = C_\mu(1 - K) = C_\mu(1 + g_m R_L)$$

$$C_2 = C_\mu\left(1 - \frac{1}{K}\right) = C_\mu(1 + g_m R_L)/g_m R_L$$

and $$C_M = C_\pi + C_1 = C_\pi + C_\mu(1 + g_m R_L) \tag{10.59a}$$

Figure 10.29 has *two independent time constants.* One is associated with C_M. Resistance seen by C_M is $R_S \| r_\pi \triangleq R_\pi^0$.

$\therefore$ The time constant $C_M R_\pi^0 = R_\pi^0[C_\pi + C_\mu(1 + g_m R_L)]$

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$\therefore$ $$g_m = \frac{1}{25} = 40 \text{ m}\mho \qquad \text{(Taking } V_T = 25 \text{ mV)}$$

and $$r_\pi = \frac{\beta_0}{g_m} = \frac{125}{40} = 3.125 \text{ k}\Omega$$

[To find C_π]

As $$f_T = \beta_0 f_\beta$$

where $$f = \frac{1}{2\pi}\omega_\beta = \frac{1}{2\pi}\frac{\beta_0}{r_\pi(C_\pi + C_\mu)}$$

$$= \frac{1}{2\pi}\frac{g_m}{(C_\mu + C_\mu)} \qquad \text{[see Eq. (10.43)]}$$

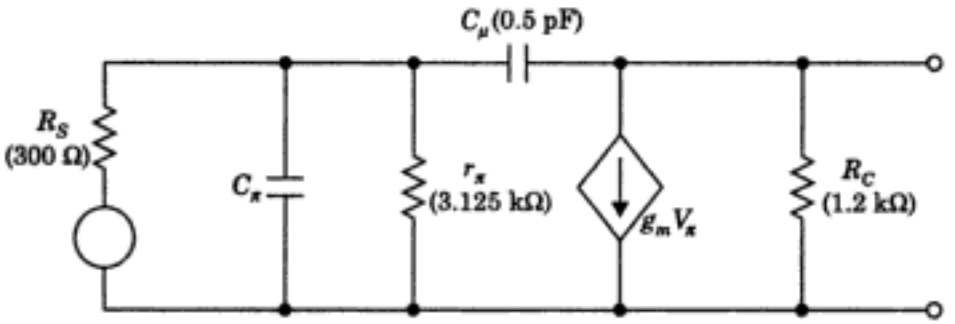


Fig. 10.30 The given equivalent circuit for Ex. 10.7.

Here $$f_T = 300 \times 10^6 = \frac{40 \times 10^{-3}}{2\pi(C_\pi + C_\mu)}$$

$\therefore$ $$C_\pi + C_\mu = \frac{40}{2\pi} \times \frac{10^{-6-3}}{300} = 21.2 \times 10^{-12} \text{ F}$$

or $$C_\pi = 21.2 - 0.5 = 20.7 \text{ pF}$$

Also $$A_{V0} = \frac{-\beta_0 R_C}{R_s + r_\pi}$$

$$= \frac{-125 \times 1.2}{0.3 \times 3.125} = -43.79 \quad \textbf{Ans.}$$

i.e., midband gain is –43.79

As $$\frac{V_0}{V_s} = \frac{[-\beta_0 R_L/(R_s + r_\pi)][1 - sC_\mu/g_m]}{1 + a_1 s + a_2 s^2} \qquad \text{[from Eq. (10.55)]}$$

where $$a_1 = R_\pi^0 C_\pi + R_\mu^0 C_\mu$$

$$= R_\pi^0 C_\pi + [R_\pi^0 + R_L(1 + g_m R_\pi^0)]\, C_\mu$$

and $$R_\pi^0 = R_s \,||\, r_\pi$$

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$$R_\pi^0 = R_S \,||\, r_\pi = \frac{r_\pi R_S}{r_\pi + R_S} \qquad \text{(from Eq. (10.56))}$$

Also $$f_H = \frac{1}{2\pi}\frac{1}{C_M R_\pi^0} \qquad \text{(from Eq. (10.60))}$$

where $$C_M = C_\pi + (1 + g_\mu R_L)C_\mu \qquad \text{(from Eq. (10.59a))}$$

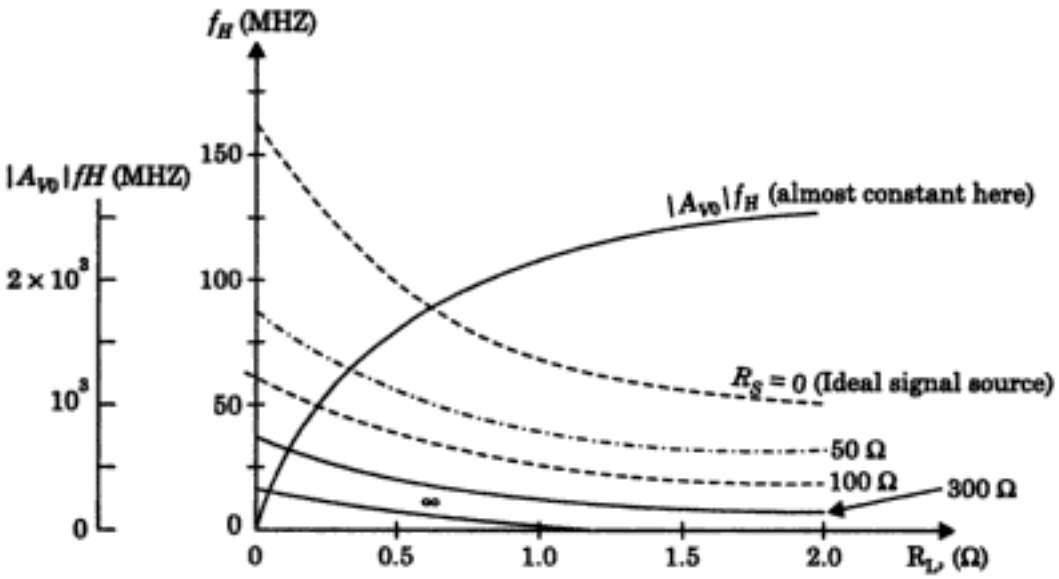


Fig. 10.31 Variation of bandwidth f_H as a function of R_L for different values of source resistance R_S. Typical curves for a single-stage *CE* amplifier are drawn. Equation (10.60) is used to compute f_H using the numerical values given in Fig. 10.29.

Note that we had calculated the value of $\omega_H = \dfrac{1}{(R_S \,||\, R_i)C_M}$ in Eq. (10.60).

Here, $R_i = r_\pi$, hence $R_S||R_i = R_S||r_\pi = R_\pi^0$. Also, C_M is shown in Fig. 10.29 and $C_M = C_\pi + C_1$ where $C_1 = (1 + g_m R_L)C_\mu$.

Using these values, we can write

$$|A_{V0} \cdot f_H| = \left(\frac{\beta_0 R_L}{r_\pi + R_S}\right) \cdot \frac{1}{2\pi[C_\pi + (1 + g_m R_L)C_\mu]} \frac{r_\pi + R_S}{r_\pi R_S}$$

$$= \frac{g_m}{2\pi[C_\pi + (1 + g_m R_L)C_\mu]} \frac{R_L}{R_S} = \frac{g_m}{2\pi C_M} \frac{R_L}{R_S} \qquad (\because\ C_\pi + (1 + g_m R_L)C_\mu = C_M \text{ and } \beta_0/r_\pi = g_m)$$

$$= \frac{g_m/[2\pi(C\pi + C_\mu)]}{1 + \dfrac{g_m R_L C_\mu}{C\pi + C_\mu}} \times \frac{R_L}{R_S}$$

From Eqn. (10.43), $\dfrac{g_m}{2\pi(C_\pi + C_\mu)} = f_T$

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However, in Fig. 10.32, the *three capacitors C_{gs}, C_{gd} and C_{ds} are not independent* as these form a loop. Thus, in the transfer function, $A_{VH}(s) = \dfrac{V_0}{V_S}$ in Fig. 10.32 we expect two poles and two zeros (one finite zero and one non-finite zero).

[To find $A_{VH}(s)$ for the circuit in Fig. 10.32]

By using model analysis, we obtain

At node G:
$$V_{gs}\left(\frac{1}{R_S} + sC_{gs} + sC_{gd}\right) - \frac{V_S}{R_S} - sC_{gd}V_0 = 0$$

$$\therefore \quad V_{gs}\left(\frac{1}{R_S} + sC_{gs} + sC_{gd}\right) - sC_{gd}V_0 = \frac{V_S}{R_S} \tag{10.62}$$

At node D:
$$V_{gs}(-sC_{gd} + g_m) + V_0\left(\frac{1}{R_L} + sC_{gd} + sC_{ds}\right) = 0 \tag{10.63}$$

where $R_L = r_d \| R_D$

From (10.63),

$$V_{gs} = \frac{-V_0\left(\dfrac{1}{R_L} + sC_{gd} + sC_{ds}\right)}{g_m - sC_{gd}}$$

Putting the value of V_{gs} in Eq. (10.62), we get

$$-\frac{V_0\left(\dfrac{1}{R_L} + sC_{gd} + sC_{ds}\right)}{g_m - sC_{gd}}\left(\frac{1}{R_s} + sC_{gs} + C_{gd}\right) - sC_{gd}V_0 = \frac{V_s}{R_s}$$

$$\therefore \quad -V_0\left[\left(\frac{1}{R_L} + sC_{gd} + sC_{ds}\right)\left(\frac{1}{R_s} + sC_{gs} + sC_{gd}\right) + (g_m - sC_{gd})sC_{gd}\right]$$

$$= (g_m - sC_{gd})\frac{V_s}{R_s}$$

or
$$-\frac{V_0}{V_s}\left[\frac{1}{R_L R_s} + s\left\{(C_{gs} + C_{gd})\frac{1}{R_L} + (C_{gd} + C_{ds})\frac{1}{R_s} + g_m C_{gd}\right\} + s^2\{(C_{gs} + C_{gd})(C_{gd} + C_{ds}) - C_{gd}^2\}\right]$$

$$= g_m \frac{1}{R_s}\left(1 - s\frac{C_{gd}}{g_m}\right)$$

$$\therefore \quad -\frac{V_0}{V_s}\frac{1}{R_L R_s}\{1 + s\{(C_{gs} + C_{gd})R_s + (C_{gd} + C_{ds})R_L + g_m C_{gd}R_L R_s\} + s^2\{C_{gs}C_{gd} + C_{gs}C_{ds} + C_{gd}C_{ds}\}R_s R_L\}$$

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$$= \frac{g_m R_L}{R_L R_s}(1 - sC_{gd}/g_m) \tag{10.63a}$$

Now coeff. of $s = C_{gs}R_s + C_{ds}R_L + C_{gd}R_s + C_{gd}R_L + g_m R_L R_s C_{gd}$

$$= R_s C_{gs} + ((1 + g_m R_L)R_S + R_L)C_{gd} + R_L C_{ds}$$

$\therefore$ (10.63a) gives

$$\frac{V_0}{V_s}\left[1 + (R_s C_{gs} + \{(1 + g_m R_L)R_S + R_L\}C_{gd} + R_L C_{ds})s + (C_{gs}C_{gd} + C_{gs}C_{ds} + C_{gd}C_{ds})R_s R_L s^2\right]$$

$$= -g_m R_L(1 - sC_{gd}/g_m)$$

$\therefore$

$$A_{VH}(s) = \frac{V_0}{V_s} = \frac{A_{V0}(1 - sC_{gd}/g_m)}{1 + a_1 s + a_2 s^2} \tag{10.64a}$$

where

$$A_{V0} = -g_m R_L \tag{10.64b}$$

$$a_1 = R_s C_{gs} + [(1 + g_m R_L)R_s + R_L]C_{gd} + R_L C_{ds} \tag{10.64c}$$

$$a_2 = R_s R_L[C_{gs}C_{gd} + C_{gs}C_{ds} + C_{ds}C_{gd}] \tag{10.64d}$$

Note that a_1 comprises the sum of time constants viz. $R_s C_{gs}$, $[(1 + g_m R_L)R_s + R_L]C_{gd}$ and $R_L C_{ds}$, and these are equal to the zero-frequency resistance (with capacitors open-circuited) seen at each capacitor terminal. For example,

$R_s C_{gs}$ = Time constant as seen by C_{gs} with C_{gd}, C_{ds} open circuited

$R_L C_{ds}$ = Time constant as seen by C_{ds} with C_{gs}, C_{gd} open circuited

Since $(1 + g_m R_L)R_s + R_L$ is the impedance seen by C_{gd} with C_{gs} and C_{ds} both open circuited [see Section 10.12, Eq. (10.58)], hence $[(1 + g_m R_L)R_s + R_L]C_{gd}$ is the time constant as seen by C_{gd} with C_{gs} and C_{ds} open circuited.

For typical parameters values shown in Fig. 10.33, we have

$$a_1 = R_s C_{gs} + [(1 + g_m R_L)R_s + R_L]C_{gd} + R_L C_{ds}$$

$$= 0.3 \times 3 + [(1 + 2 \times 16) + 16] \times 1 + 16 \times 1.5$$

$$\left(\because R_L = 80\text{k}\Omega \,||\, 20\text{ k}\Omega = \frac{80 \times 20}{80 + 20} = 16\text{ k}\Omega\right)$$

$$= 0.9 + (33 + 16) + 24 = 73.9 \text{ ns}$$

$$a_2 = R_s R_L[C_{gs}C_{gd} + C_{gd}C_{ds} + C_{ds}C_{gs}]$$

$$= 0.3 \times 16[3 \times 1 + 1 \times 1.5 + 1.5 \times 3]$$

$$= 4.8(3 + 1.5 + 4.5) = 43.2 \text{ (ns)}^2$$

Also, from Eq. (10.51)

$$p_1 = \frac{1}{a_1} = \frac{1}{73.9} \times 10^9 = 13.53 \times 10^6 \text{ rad/s}$$

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$$\therefore \quad V_0\left[\left(\frac{1}{R_S}+sC_\mu+\frac{1}{Z_\pi}\right)\left(g_m+\frac{1}{Z_\pi}+\frac{1}{R_E}\right)-\left(g_m+\frac{1}{Z_\pi}\right)\frac{1}{Z_\pi}\right]=\left(g_m+\frac{1}{Z_\pi}\right)\frac{V_S}{R_S}$$

or $$\frac{V_0}{V_S}\left[\left(\frac{1}{R_S}+sC_\mu\right)\left(g_m+\frac{1}{Z_\pi}\right)+\left(\frac{1}{R_S}+sC_\mu\right)\left(\frac{1}{R_E}\right)+\frac{1}{Z_\pi R_E}\right]=\left(g_m+\frac{1}{Z_\pi}\right).\frac{1}{R_S} \quad \text{(10.70a))}$$

As $$g_m+\frac{1}{Z_\pi}=g_m+\frac{r_\pi+\frac{1}{sC_\pi}}{r_\pi\cdot\frac{1}{sC_\pi}}=g_m+\frac{1+sC_\pi r_\pi}{r_\pi}$$

$$=\frac{g_m r_\pi+1+sC_\pi r_\pi}{r_\pi}=\frac{(1+\beta_0)+sC_\pi r_\pi}{r_\pi} \qquad (\because\ g_m r_\pi=\beta_o)$$

$$=\frac{1+sC_\pi r_\pi/(1+\beta_0)}{r_\pi/(1+\beta_0)}=\frac{(1+\beta_0)[1+sC_\pi r_\pi/(1+\beta_0)]}{r_\pi}$$

Therefore, Eq. (10.70a) reduces to, using $Z_\pi=\frac{r_\pi}{(1+sC_\pi r_\pi)}$,

$$\frac{V_0}{V_S}\left[\left(\frac{1}{R_S}+sC_\mu\right)\left(\frac{1+\beta_0+sC_\pi r_\pi}{r_\pi}\right)+\left(\frac{1}{R_S}+sC_\mu\right)\frac{1}{R_E}+\frac{1}{R_E}.\frac{1+sC_\pi r_\pi}{r_\pi}\right]$$

$$=\frac{(1+\beta_0)[1+sC_\pi r_\pi/(1+\beta_0)]}{r_\pi R_S}$$

$$\therefore \quad \frac{V_0}{V_S}\left[\left(\frac{1+\beta_0}{R_\pi r_\pi}+\frac{1}{R_S R_E}+\frac{1}{R_E r_\pi}\right)+s\left(\frac{C_\pi}{R_S}+\frac{(1+\beta_0)C_\mu}{r_\pi}+\frac{C_\mu}{R_E}+\frac{C_\pi}{R_E}\right)+s^2(C_\mu C_\pi)\right]$$

$$=\frac{(1+\beta_0)[1+sC_\pi r_\pi/(1+\beta_0)]}{r_\pi R_S}$$

or $$\frac{V_0}{V_S}\left[\frac{(1+\beta_0)R_E+r_\pi+R_S}{r_\pi R_S R_E}+\frac{s}{r_\pi R_S R_E}\left(\frac{(R_E+R_S)r_\pi C_\pi}{1}+\frac{((1+\beta_0)R_E R_S+r_\pi R_S)C_\mu}{1}\right)\right.$$

$$\left.+s^2\frac{R_E R_S r_\pi C_\pi C_\mu}{R_E R_S r_\pi}\right]=\frac{(1+\beta_0)[1+sC_\pi r_\pi/(1+\beta_0)]}{r_\pi R_S}$$

Dividing both sides by $\frac{R_S+r_\pi+(1+\beta_0)R_E}{r_\pi R_S R_E}$, we get

$$\frac{V_0}{V_S}\left[1+s\left(\frac{r_\pi(R_E+R_S)C_\pi}{R_S+r_\pi+(1+\beta_0)R_E}+\frac{R_E\{r_\pi+(1+\beta_0)R_E\}C_\mu}{R_S+r_\pi+(1+\beta_0)R_E}\right)\right.$$

$$\left.+s^2\frac{R_E R_S r_\pi C_\pi C_\mu}{R_S+r_\pi+(1+\beta_0)R_E}\right]=\frac{(1+\beta_0)R_E}{R_S+r_\pi+(1+\beta_0)R_E}\times\frac{1+sC_\pi r_\pi/(1+\beta_0)}{1}$$

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$$= \frac{(40.95 + 45.75) \times 10^{-9}}{153.1 \times 10^3} = 0.566 \times 10^{-9} \text{ seconds}$$

and $$a_2 = \frac{R_E R_S r_\pi C_\pi C_\mu}{[R_S + r_\pi + (1 + \beta_0) R_E]}$$

$$= \frac{(1.5 \times 0.6 \times 1 \times 19.5 \times 0.5) 10^9 \times 10^{-24}}{153.1 \times 10^3}$$

$$= \frac{8.775 \times 10^{-15}}{153.1 \times 10^3} = 0.0573 \times 10^{-18} \, s^2$$

$\therefore$ Zero frequency $$Z_1 = \frac{g_m}{C_\pi}$$

$$= \frac{0.1}{19.5 \times 10^{-12}} = 5.128 \times 10^9 \text{ rad/s}$$

Approximate dominant-pole angular frequency is given by Eq. (10.51).

$$p_1 = \omega_H$$

$$= \frac{1}{a_1} = \frac{1}{(0.566 \times 10^{-9})} = 1.766 \times 10^9 \text{ rad/s}$$

$\therefore$ $$f_H = \frac{\omega_H}{2\pi}$$

$$= \frac{1.766 \times 10^9}{(2\pi)} = 281.19 \text{ MHz}$$

Also $$p_2 = \frac{a_1}{a_2}$$

$$= \frac{0.566 \times 10^{-9}}{0.0573 \times 10^{-18}} = 9.8778 \times 10^9 \text{ rad/s}$$

and $$f_2 = \frac{p_2}{(2\pi)} = 1.572 \text{ GHz}$$

The ratio $\frac{p_2}{p_1} = \frac{9.8778 \times 10^9}{1.766 \times 10^9} = 5.59 < 8$, hence the dominant-pole approximation does not give particularly accurate results. (*Note this point*)

The exact solution for poles yields as follows:

$$1 + a_1 s + a_2 s^2 = 0$$

or $$1 + 0.566 \times 10^{-9} \, s + 0.0573 \times 10^{-18} \, s^2 = 0$$

or $$s^2 + 9.8778 \, s + 17.45 = 0$$

or $$s = \frac{-9.8778 \pm \sqrt{(9.8778)^2 - 4 \times 17.45}}{2} = \frac{-9.8778 \pm 5.269}{2}$$

$$= -7.57 \times 10^9, \quad -2.30 \times 10^9 \text{ rads/s}$$

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i.e., $p_1 = 2.3 \times 10^9, \quad p_2 = 7.57 \times 10^9$

$\therefore \quad f_1 = \dfrac{p_1}{2\pi}$

$$= \frac{2.3 \times 10^9}{(2\pi)} = 366 \text{ MHz}$$

and $f_2 = \dfrac{p_2}{2\pi} = 1.204 \text{ GHZ}$

We note here that $f_H \approx 366$ MHz, ($\because$ 3 dB BW is nearly equal to pole p_1 frequency), zero frequency $Z_1/2\pi = 816$ MHz are of high order and "are the order of magnitude of f_T" we had for *CE* stage, $f_H \cong 16.9$ MHz (Section 10.11) and here for the *CC* stage, f_H is nearly 281.2 MHz. Thus, the *C-C (Emitter follower) stage has considerably larger bandwidth than does the CE stage.*

If we have a *CE* stage with $R_C = 1.5$ kΩ, driven from a source with $R_S = 0.6$ kΩ and the same parameters of transistor as in the above example, we would get f_H for *CE* stage as 4.37 MHz. In cascaded *CE-CC* or *CC-CE*, the overall f_H is the 'f_H' that of the CE stage.

10.16.1 Derivation of $A_{VH}(s)$ by Time Constant Method for the Emitter Follower Circuit (Short Cut)

We can also derive Eqs. (10.71) to (10.73) by an alternative method. The circuit in Fig. 10.36 has two capacitors hence two poles and two zeros. We know that for an emitter follower

$$A_{V0} = \text{DC gain}$$

$$= \frac{(1+\beta_0)R_E}{R_s + r_\pi + (1+\beta_0)R_E} \tag{10.74}$$

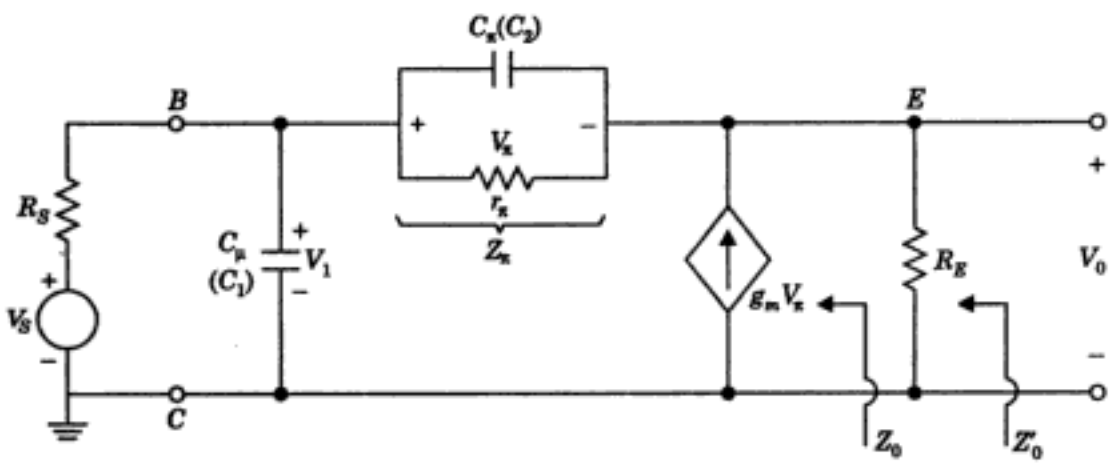


Fig. 10.36 The emitter follower circuit at high frequency.

Let $$A_{VH}(s) = A_{V0}\frac{N(S)}{D(S)} \tag{10.75}$$

Zeros of $A_V(s)$: One zero occurs when no current flows in R_E. Then $V_\pi = V_1$ Current from *B* to *E* side through $(C_\pi || r_\pi)$ is:

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$$\frac{V_1}{Z_\pi} = V_1 \frac{(1 + sC_\pi r_\pi)}{r_\pi}$$

If $A_{VH} = 0$ then

$$V_1 \frac{1 + sC_\pi r_\pi}{r_\pi} = -V_\pi g_m$$

(current from B to E is $-g_m V_\pi$ and no current in R_E)

As $V_\pi = V_1$ and $r_\pi \cdot g_m = \beta_0$, above equation gives us

$$1 + sC_\pi r_\pi = -\beta_0$$

Thus, $$s = \frac{-(1 + \beta_0)}{C_\pi r_\pi}$$

$\left(1 + s\frac{C_\pi r_\pi}{1 + \beta_0}\right)$ is a factor of numerator $N(s)$ of Eq. (10.75). Second zero of $A_{VH}(s)$ occurs at $s \to \infty$ as then C_μ gives shorting effect hence V_s cannot reach V_0. Thus, $N(s)$ is of degree 1 and $D(s)$ of degree 2 in $A_{VH}(s)$ of Eq. (10.75).

[To find a_1]

$$a_1 = R_{11}^0 C_1 + R_{22}^0 C_2$$

$$R_{11}^0 = R_S \,||\, (r_\pi + (1 + \beta_0) R_E) = \frac{R_S (r_\pi + (1 + \beta_0) R_E)}{R_S + r_\pi + (1 + \beta_0) R_E}$$

Impedance R_{11}^0 is seen by C_1 (i.e., by C_μ) with C_2 (i.e., C_μ) open circuited. For an emitter follower, we know that the input impedance is R_i equalling $r_\pi + (1 + \beta_0)R_E$. Therefore, R_{11}^0 is equal to R_S parallel with R_i, as may be seen in Fig. 10.37.

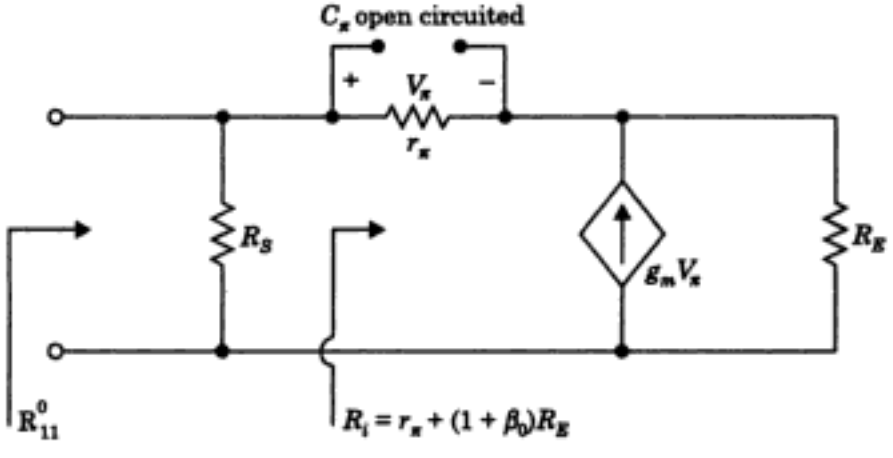


Fig. 10.37 To find R_{11}^0 (impedance seen by C_1 (i.e. by C_μ)), open circuit capacitor C_2 (which is C_π here).

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R_{22}^0 is the impedance seen by C_2 (i.e., by C_π) with C_μ open circuited, as shown in Fig. 10.38.

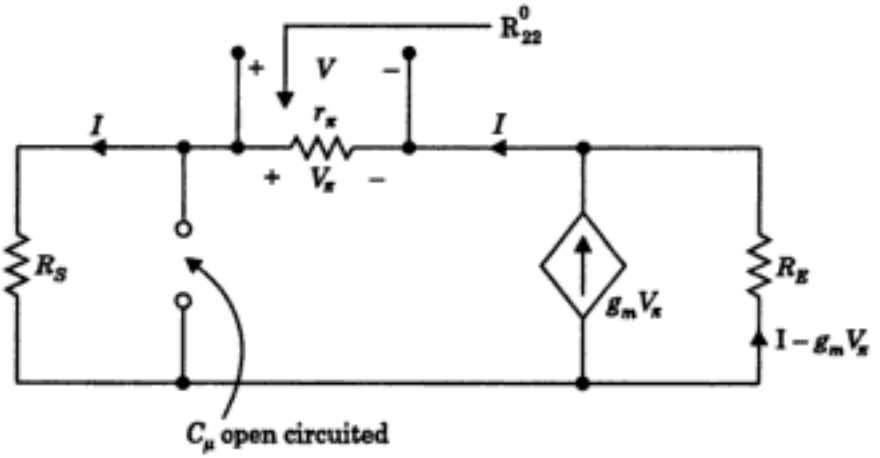


Fig. 10.38 To find R_{22}^0 (impedance seen by C_2 with C_1 open circuited).

$$R_{22}^0 = r_\pi \| \text{impedance seen by } V/I$$

Apply a test voltage V and find current I.

As $$V = IR_S + (I - g_m V)R_E$$

$\therefore$ $$V(1 + g_m R_E) = I(R_S + R_E)$$

$$\frac{V}{I} = \frac{R_S + R_E}{1 + g_m R_E}$$

$\therefore$ $$R_{22}^0 = \frac{r_\pi (R_S + R_E)(1 + g_m R_E)}{r_\pi + (R_S + R_E)} = \frac{r_\pi (R_S + R_E)}{r_\pi + R_S + (1 + \beta_o) R_E}$$

$\therefore$ $$a_1 = \frac{R_S [r_\pi + (1 + \beta_0) R_E] C_\mu}{R_S + r_\pi + (1 + \beta_0) R_E} + \frac{r_\pi (R_S + R_E) C_\pi}{R_S + r_\pi + (1 + \beta_0) R_E}$$ (see Eq. (10.72))

[*To find* a_2]

$$a_2 = (R_{11}^0 C_1)(R_{22}^1 C_2)$$

But $$R_{22}^1 = R_{22}^0 \Big|_{R_s = 0} = \frac{r_\pi R_E}{r_\pi + (1 + \beta_0) R_E}$$

$\therefore$ $$a_2 = \frac{R_S [r_\pi + (1 + \beta_0) R_E] C_\mu}{R_S + r_\pi + (1 + \beta_0) R_E} \frac{r_\pi R_E C_\pi}{[r_\pi + (1 + \beta_0) R_E]}$$

$$= \frac{R_S r_\pi R_E C_\pi C_\mu}{R_S + r_\pi + (1 + \beta_0) R_E}$$

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Hence $$A_{VH}(s) = \frac{(1+\beta_0)R_E}{R_s + r_\pi + (1+\beta_0)R_E} \frac{1 + [sC_\pi r_\pi/(1+\beta_0)]}{1 + a_1 s + a_2 s^2}$$ (see Eq. (10.71))

The values of a_1, a_2 and $A_{VH}(s)$ obtained here are the same as we derived in section 16.1.

Thus, in many circuits it is easy to derive the voltage gain transfer function by using time constant method.

10.16.2 The Output Impedance Z_0 of the Emitter Follower

We use the Thevenin's equivalent to find first Z_0', where

$$Z_0' = \frac{V_0}{I_{SC}} = \frac{V_s A_{VH}}{I_{SC}}$$

By using the value of $A_{VH}(s)$ from Eq. (10.71), we have

$$I_{SC} = \frac{V_0}{R_E}\bigg|_{R_E=0} = \frac{A_{VH}(s).V_S}{R_E}\bigg|_{R_E=0}$$

$$= \frac{(1+\beta_0)[1 + sC_\pi r_\pi/(1+\beta_0)]V_S}{[R_S + r_\pi + (1+\beta_0)R_E](1 + a_1 s + a_2 s)R_E}\bigg|_{R_E=0}$$

$$= \frac{V_S(1+\beta_0)[1 + sC_\pi r_\pi/(1+\beta_0)]}{(R_S + r_\pi)(1 + a_1 s + a_2 s^2)}\bigg|_{R_E=0}$$

As $$a_1|_{R_E=0} = \frac{r_\pi(R_E + R_S)C_\pi + R_S[r_\pi + \overbrace{(1+\beta_0)R_E}^{=0}]C_\mu}{R_S + r_\pi + \underbrace{(1+\beta_0)R_E}_{=0}}\bigg|_{R_E=0}$$

$$= \frac{r_\pi R_S C_\pi + R_S r_\pi C_\mu}{R_S + r_\pi} = \frac{R_S r_\pi (C_\pi + C_\mu)}{R_S + r_\pi}$$

$$a_2|_{R_E=0} = \frac{R_E R_S r_\pi C_\pi C_\mu}{R_S + r_\pi + (1+\beta_0)R_E}\bigg|_{R_E=0} = 0$$

Hence $$I_{SC} = \frac{(1+\beta_0)[1 + sC_\pi r_\pi/(1+\beta_0)]V_S}{(R_S + r_\pi)[1 + sR_S r_\pi(C_\pi + C_\mu)/(R_S + r_\pi)]}$$ (10.76)

$$\therefore \quad Z_0' = \frac{(1+\beta_0)R_E[1 + sC_\pi r_\pi/(1+\beta_0)]V_S}{[R_S + r_\pi + (1+\beta_0)R_E][1 + a_1 s + a_2 s^2]} \Big/ \frac{(1+\beta_0)[1 + sC_\pi r_\pi/(1+\beta_0)]V_S}{(R_S + r_\pi)[1 + sR_S r_\pi(C_\pi + C_\mu)/(R_S + r_\pi)]}$$

$$= \frac{R_E(R_S + r_\pi)[1 + sr_\pi R_S(C_\pi + C_\mu)/(R_S + r_\pi)]}{[R_S + r_\pi + (1+\beta_0)R_E](1 + a_1 s + a_2 s^2]}$$

$$= \frac{R_E[(R_S + r_\pi)/(1+\beta_0)][1 + sr_\pi R_S(C_\pi + C_\mu)/(R_S + r_\pi)]}{[R_E + (R_S + r_\pi)/(1+\beta_0)][1 + a_1 s + a_2 s^2]}$$ (10.77)

As
$$Z_0' = \frac{R_E[(R_s + r_\pi)/(1+\beta_0)]}{R_E + [(R_s + r_\pi)/(1+\beta_0)]} \cdot \frac{1 + sr_\pi R_S(C_\pi + C_\mu)/(R_S + r_\pi)}{1 + a_1 s + a_2 s^2} \tag{10.78}$$

Note that $Z_0 = Z_0'\big|_{R_E \to \infty}$ $\because$ $Z_0' = Z_0 \,||\, R_E$

$\therefore$
$$Z_0 = \frac{R_E[(R_s + r_\pi)/(1+\beta_0)]}{R_E + [(R_s + r_\pi)/(1+\beta_0)]} \cdot \frac{1 + sr_\pi R_S(C_\pi + C_\mu)/(R_S + r_\pi)}{1 + a_1 s + a_2 s^2}\Bigg|_{R_E \to \infty}$$

$$a_1\big|_{R_E \to \infty} = \frac{r_\pi(R_E + R_S)C_\pi + R_S C_\mu[r_\pi + (1+\beta_0)R_E]}{R_S + r_\pi + (1+\beta_0)R_E}\Bigg|_{R_E \to \infty}$$

$$= \frac{r_\pi C_\pi + R_S C_\mu(1+\beta_0)}{1+\beta_0} = \frac{r_\pi C_\pi}{1+\beta_0} + R_s C_\mu$$

$$a_2\big|_{R_E \to \infty} = \frac{R_E R_S r_\pi C_\pi C_\mu}{R_S + r_\pi + (1+\beta_0)R_E}\Bigg|_{R_E \to \infty} = \frac{R_S r_\pi C_\pi C_\mu}{(1+\beta_0)}$$

$\therefore$
$$Z_0 = \frac{(R_S + r_\pi)/(1+\beta_0)}{1} \cdot \frac{1 + sr_\pi R_S(C_\pi + C_\mu)/(R_S + r_\pi)}{1 + s\left(\dfrac{r_\pi C_\pi}{1+\beta_0} + R_S C_\mu\right) + s^2 \dfrac{R_S r_\pi C_\pi C_\mu}{1+\beta_0}}$$

$$= \frac{R_S + r_\pi}{(1+\beta_0)} \cdot \frac{1 + sr_\pi R_S(C_\pi + C_\mu)/(R_S + r_\pi)}{(1 + s\underbrace{r_\pi C_\pi/(1+\beta_0)}_{\triangleq 1/p_2})(1 + s\underbrace{R_s C_\mu}_{\triangleq 1/p_2})} \tag{10.79}$$

Let $Z_0\big|_{s=0} = R_0$ (output impedance at DC)

$\therefore$
$$Z_0 = R_0 \frac{(1 + s/Z_1)}{(1 + s/p_1)(1 + s/p_2)} \tag{10.80a}$$

where
$$R_0 = \frac{(R_S + r_\pi)}{(1+\beta_0)} \tag{10.80b}$$

$$p_1 = \frac{1+\beta_0}{r_\pi C_\pi} \tag{10.80c}$$

$$p_2 = \frac{1}{R_S C_\mu} \tag{10.80d}$$

$$Z_1 = \frac{(R_S + r_\pi)}{(r_\pi R_S(C_\pi + C_\mu))} \tag{10.80e}$$

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For the values indicated in Fig. 10.35 (redrawn here as Fig. 10.39), we get

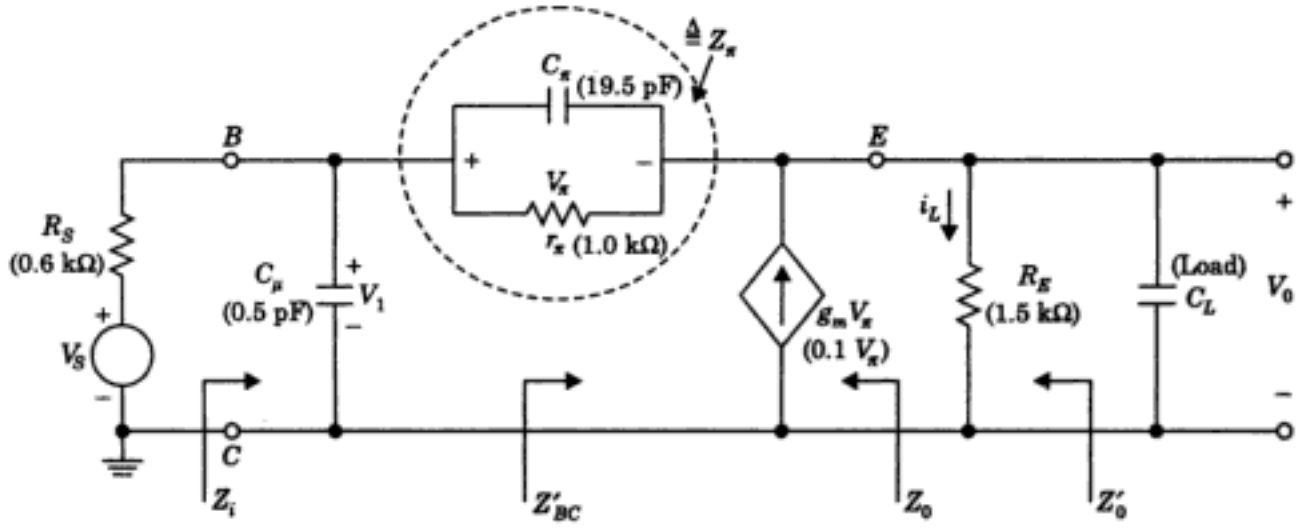


Fig. 10.39 The high frequency equivalent circuit of the emitter follower. The capacitor C_L forms part of the load fed by the emitter follower stage.

$$Z_1 = \frac{(R_S + r_\pi)}{[r_\pi R_S (C_\pi + C_\mu)]} \quad \text{(the frequency for } A_{VH}(s) = 0\text{) (from Eq. (10.80e))}$$

$$= \frac{(0.6 + 1.0)10^3}{(1 \times 0.6)10^6 (19.5 + 0.5) \times 10^{-12}}$$

$$= \frac{1.6 \times 10^3}{20 \times 0.6 \times 10^{-6}} = \frac{16}{12} \times 10^8 = 1.33 \times 10^8 \text{ rad/s}$$

Now, $$p_1 = \frac{(1 + \beta_0)}{r_\pi C_\pi} \quad \text{(from Eq. (10.80c))}$$

$$= \frac{(1 + 100)}{(1 \times 10^3) \times (19.5 \times 10^{-12})} = 5.179 \times 10^9 \text{ rad/s}$$

$$= 51.79 \times 10^8 \text{ rad/s}$$

From Eq. (10.80d), we get

$$p_2 = \frac{1}{R_S C_\mu}$$

$$= \frac{1}{(0.6 \times 10^3)(0.5 \times 10^{-12})} = 3.33 \times 10^9 = 33.3 \times 10^8 \text{ rad/s}$$

It is customary to name the poles p_i such that $p_1 < p_2 < p_3 \ldots$. We may therefore, rename p_1, p_2 as $p_1 = 3.33 \times 10^9$ rad/s, $p_2 = 5.179 \times 10^9$ rad/s.

Figure 10.40 shows $\log |Z_0(j\omega)|$ versus $\log \omega$. $|Z_0(j\omega)|$ increases in $Z_1 \leq \omega \leq p_1$, i.e., acts as inductive. When an emitter follower feeds a capacitive load, say, C_L, the circuit behaves as a resonant circuit since Z_0 is inductive and is parallel with capacitive load C_L.

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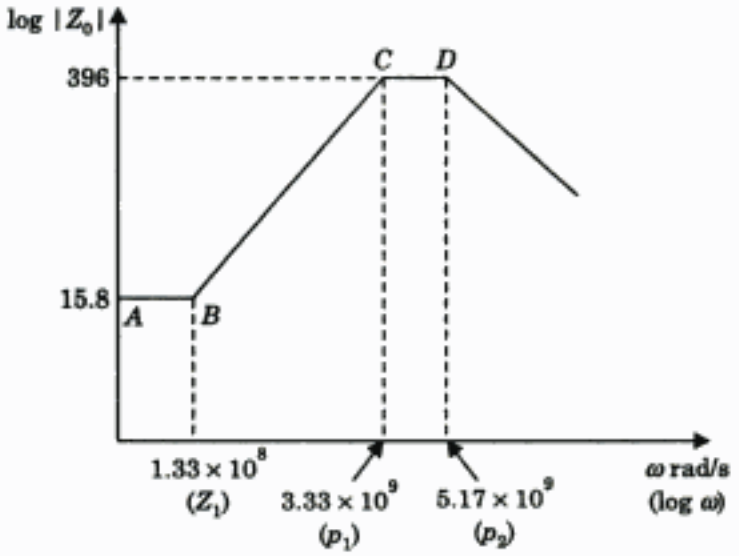


Fig. 10.40 Bode's approximation of magnitude of the output impedance Z_0 of the emitter follower in Fig. 10.39. From B to C, Z_0 is inductive. If load is capacitive, then the frequency range B to C causes RINGING due to resonance.

In systems excited by pulses such as the ECL family, high-speed logic, the load capacitance can cause excessive *ringing* on the output waveform. We usually provide sufficient damping to minimise the ringing.

10.16.3 The Input Impedance Z_i of the Emitter Follower

We now aim at determining the input impedance of the emitter follower, which is known to be fairly high.

The given circuit is shown in Fig. 10.41a. If we convert the controlled current source $g_m V_\pi$ to an equivalent voltage source, we can redraw the circuit as in Fig. 10.41b as far as Z_i and $Z_{B'C}$ are concerned. We have assumed $C_L = 0$ and $Z_\pi = r_\pi \| C_\pi$.

$$\therefore \qquad Z_\pi = \frac{r_\pi}{1 + sC_\pi r_\pi}$$

[*To find* $Z_{B'C}$]

Apply a test current I_X between XX'

$$\therefore \qquad V_{XX'} = I_X Z_\pi + I_X R_E + g_m R_E V_\pi$$

Put $V_\pi = I_X Z_\pi$

$$\therefore \qquad V_{XX'} = I_X[R_E + Z_\pi(1 + g_m R_E)]$$

Thus,
$$Z'_{BC} = \frac{V_{XX'}}{I_X} = R_E + Z_\pi(1 + g_m R_E)$$

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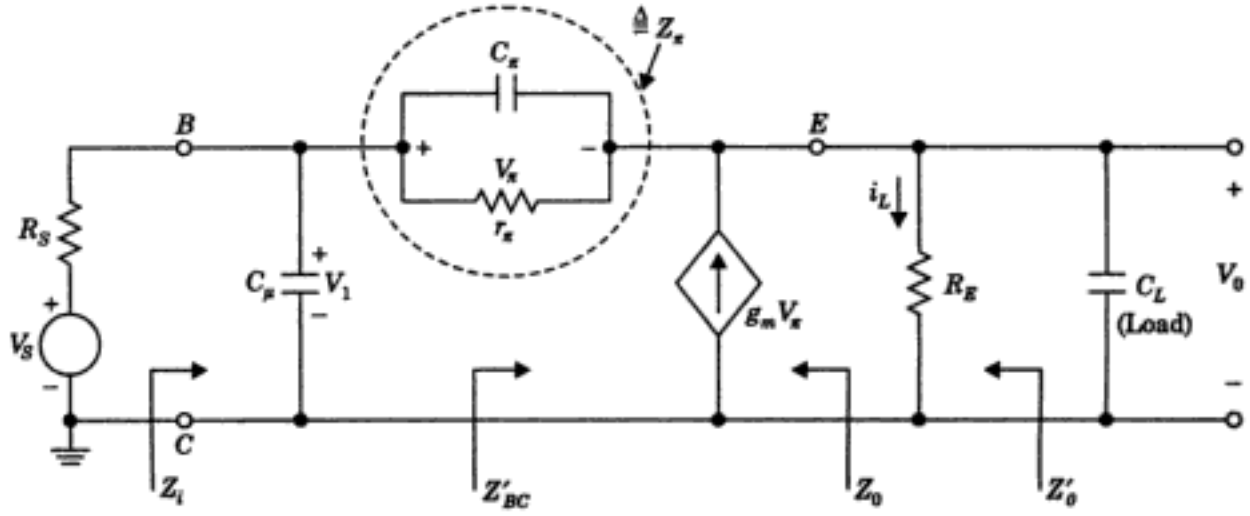


Fig. 10.41a The high frequency equivalent circuit of the emitter follower. C_L is part of the load, connected across R_E.

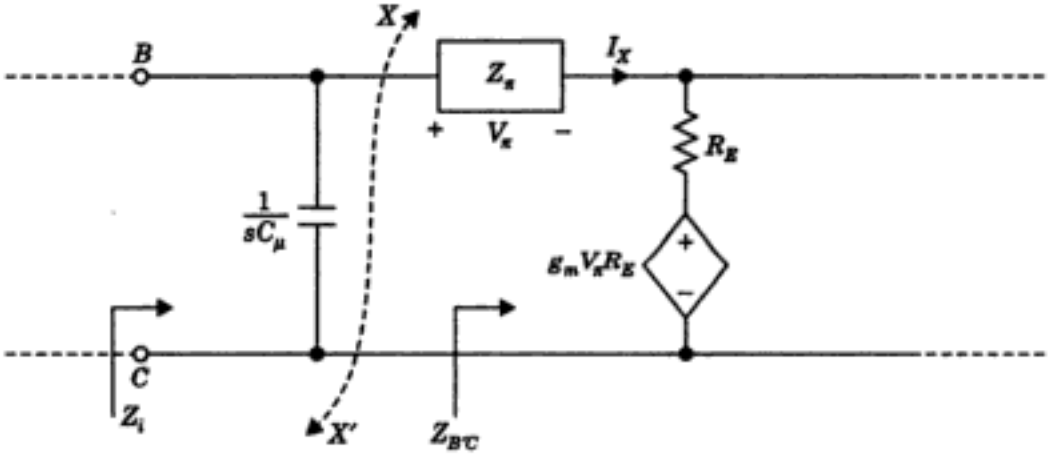


Fig. 10.41b Figure 10.41a redrawn for Z_i and $Z_{B'C}$ only (converting current source $g_m V_\pi$ into a voltage source $g_m V_\pi R_E$)

$$= R_E + \frac{r_\pi(1 + g_m R_E)}{1 + sC_\pi r_\pi} = \frac{r_\pi(1 + g_m R_E) + R_E(1 + sC_\pi r_\pi)}{1 + sC_\pi r_\pi}$$

$$= \frac{r_\pi + R_E(1 + \beta_0) + sC_\pi r_\pi R_E}{1 + sC_\pi r_\pi} \qquad (\because \; r_\pi g_m = \beta_0)$$

$$= \beta_0 R_E \cdot \frac{[r_\pi + R_E(1 + \beta_0)]/\beta_0 R_E + sC_\pi / g_m}{1 + sC_\pi r_\pi}$$

$$= \beta_0 R_E \frac{1 + sC_\pi / g_m}{1 + sC_\pi r_\pi}$$

Assuming $r_\pi << R_E(1 + \beta_0)$ and $\beta_0 >> 1$

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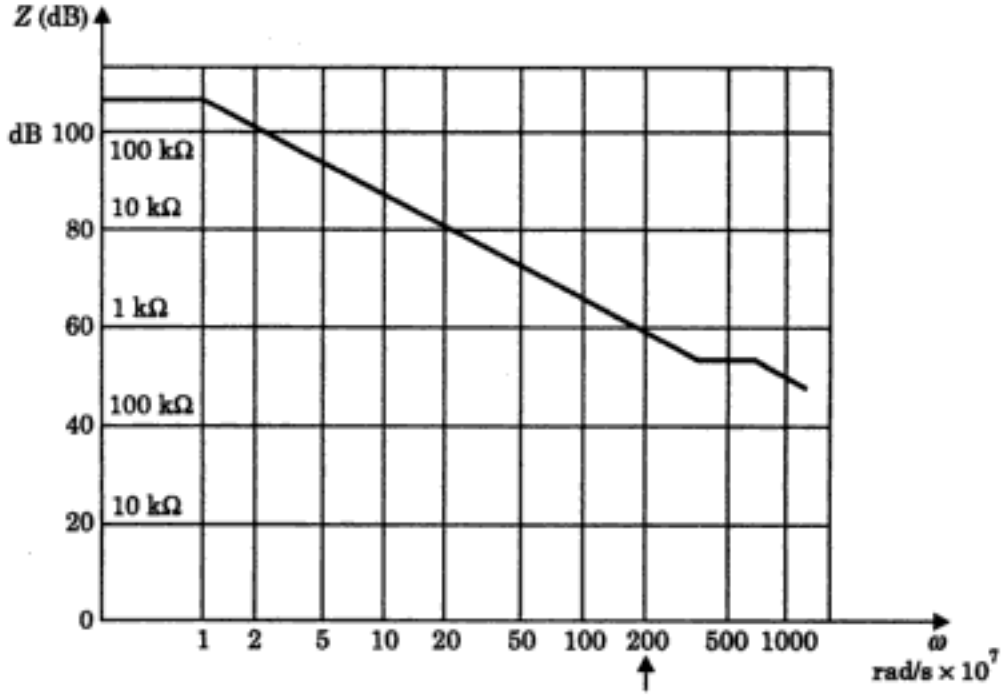


Fig. 10.42 Asymptotic Bode diagram for the input impedance $Z_i(s)$ of the Emitter Follower Fig. 10.36. Pole and zero frequencies obtained by the use of dominant-pole approximation.

$$\therefore \quad \frac{1}{\beta_0 R_E \omega_\beta} = \frac{1}{g_m r_\pi R_E \dfrac{1}{r_\pi C_\pi}} = \frac{1}{\left(R_E \dfrac{g_m}{C_\pi}\right)} = \frac{1}{(R_E \omega_T)}$$

10.17 THE SOURCE FOLLOWER (Frequency Response)

A source follower is analogous to the emitter follower (in BJT) and is an important circuit. The source follower model at high frequencies is shown in Fig. 10.43. This circuit is similar to the emitter follower circuit. If we let $r_\pi \to \infty$, $C_\mu \to C_{gd}$, $C_\pi \to C_{gs}$ and $R_L = R_E \to r_d \| R_S$, we can deduce the results for source follower from those of the emitter follower.

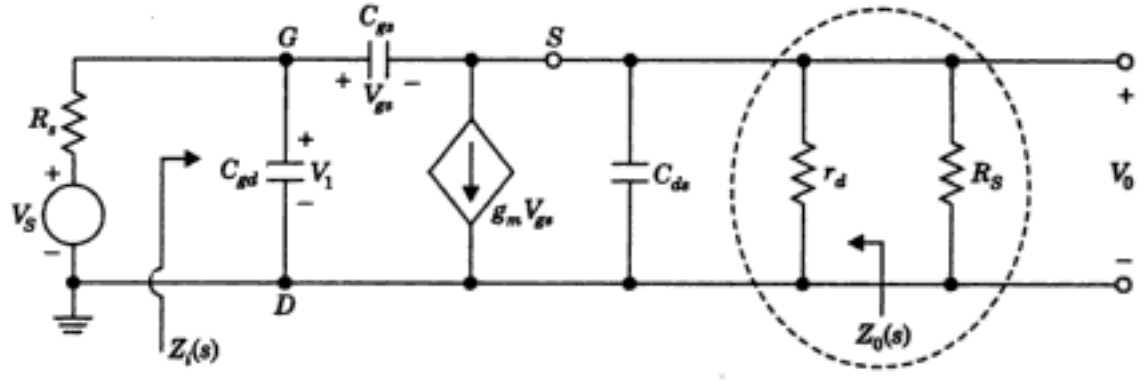


Fig. 10.43 The high frequency equivalent circuit of the Source Follower.

Only the capacitance C_{ds} cannot be identified in Fig. 10.43 and its effect on the coefficients a_1 and a_2 must be included. We can show that (see Example 10.10)

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Solution: Here

a_1 = Time constants due to C_{gd}, C_{gs} and C_{ds}

R_{11}^0 = Open circuit C_2 and C_3 and resistance seen by C_1 is clearly R_s

R_{33}^0 is calculated as follows: Open circuit C_1 and C_2, apply a test voltage V across C_3 terminals, and find current flowing through this test voltage V, as shown in Fig. 10.45.

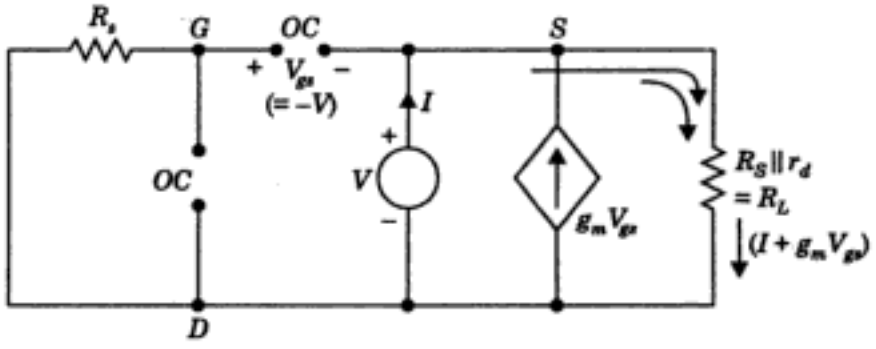


Fig. 10.45 To find R_{33}^0 for circuit in Fig. 10.44.

From Fig. 10.45, we have

$$V = (I + g_m V_{gs})R_L$$
$$= (I - g_m V)R_L \qquad (\because \quad V_{gs} = -V)$$

$$\therefore \qquad \frac{V}{I} = R_{33}^0 = \frac{R_L}{1 + g_m R_L}$$

Now, R_{22}^0 can be obtained as follows: Open circuit C_1 and C_3 and apply a test voltage V across C_2 terminals, as shown in Fig. 10.46

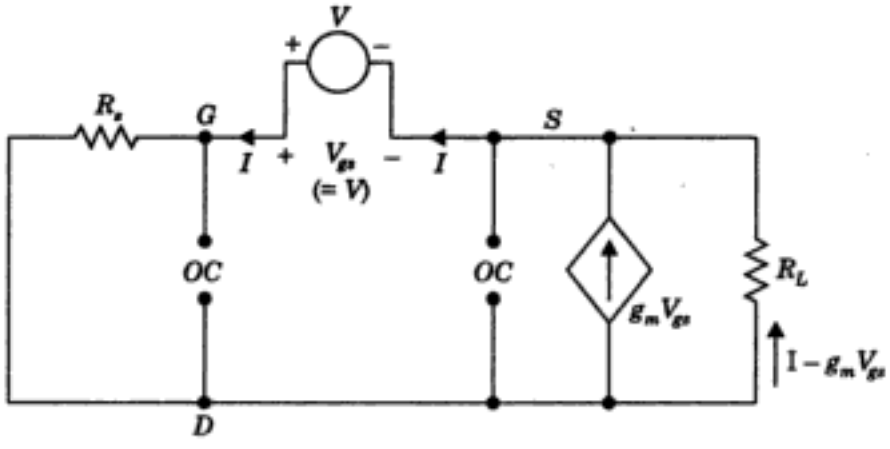


Fig. 10.46 To find R_{22}^0, for circuit in Fig. 10.44.

From Fig. 10.46, we get

$$V = IR_s + (I - g_m V_{gs})R_L$$
$$= IR_s + (I - g_m V)R_L$$

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$$\therefore \qquad V(1 + g_m R_L) = I(R_s + R_L)$$

or
$$R_{22}^0 = \frac{V}{I} = \frac{R_s + R_L}{1 + g_m R_L}$$

Thus,
$$a_1 = C_1 R_1^0 + C_2 R_2^0 + C_3 R_3^0 = R_s C_{gd} + \frac{(R_s + R_L) C_{gs}}{1 + g_m R_L} + \frac{R_L}{1 + g_m R_L} C_{ds} \quad \textbf{Ans.}$$

(which is the same as given in Eq. (10.84b))

The transfer function V_0/V_s has two poles and, therefore, two zeros. One zero is at $s = \infty$ when C_{gs} and C_{gd} short circuit making V_S and V_0 short circuited. The other zero is when the current in C_{gs} is such that

$$V_{gs}\, sC_{gs} = -g_m V_{gs}$$

$$\therefore \qquad s = -\frac{g_m}{C_{gs}} \quad \text{or} \quad \left(1 + s\frac{C_{gs}}{g_m}\right) = 0$$

Writing nodal equations

At node G

$$(V_1 - V_s)/R_s + sC_{gs}(V_1 - V_s) + sC_{gd}V_1 = 0 \tag{i}$$

$$\therefore \qquad V_1\left(\frac{1}{R_s} + sC_{gs} + sC_{gd}\right) - V_0(sC_{gs}) = \frac{V_s}{R_s} \tag{ii}$$

At node S

Using $V_{gs} = V_1 - V_0$,

$$sC_{gs}(V_0 - V_1) + V_0\left(\frac{1}{R_L} + sC_{ds}\right) - g_m(V_1 - V_0) = 0 \tag{iii}$$

$$\therefore \qquad -V_1[sC_{gs} + g_m] + V_0\left[sC_{gs} + \frac{1}{R_L} + sC_{ds} + g_m\right] = 0 \tag{iv}$$

Using $V_1 = \dfrac{\left(\frac{V_s}{R_s} + sC_{gs}V_0\right)}{\left(\frac{1}{R_s} + sC_{gs} + sC_{gd}\right)}$ from Eq. (ii) in Eq. (iv), we get

$$-\frac{\left(\frac{V_s}{R_s} + sC_{gs}V_0\right)}{\frac{1}{R_s} + sC_{gs} + sC_{gd}}(sC_{gs} + g_m) + V_0\left[\frac{1}{R_L} + g_m + s(C_{gs} + C_{ds})\right] = 0$$

or
$$V_0\left[-\frac{sC_{gs}(sC_{gs} + g_m)}{\frac{1}{R_s} + s(C_{gs} + C_{gd})} + \left(\frac{1}{R_L} + g_m + s(C_{gs} + C_{ds})\right)\right] = \frac{\frac{V_s}{R_s}(sC_{gs} + g_m)}{\frac{1}{R_s} + s(C_{gs} + C_{gd})}$$

or
$$\frac{V_0}{V_s}\left[-sC_{gs}(sC_{gs} + g_m) + \left(\frac{1}{R_s} + sC_{gs} + sC_{gd}\right)\left(\frac{1}{R_L} + g_m + sC_{gs} + sC_{ds}\right)\right] = \frac{g_m}{R_s}\left(1 + s\frac{C_{gs}}{g_m}\right)$$

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$$\therefore \quad \frac{V_0}{V_s}\left[\frac{1}{R_s}\left(\frac{1}{R_L}+g_m\right)+s\left\{-g_mC_{gs}+(C_{gs}+C_{gd})\left(\frac{1}{R_L}+g_m\right)+\frac{1}{R_s}(C_{gs}+C_{ds})\right\}\right.$$

$$\left.+s^2\left\{-C_{gs}^2+(C_{gs}+C_{gd})(C_{gs}+C_{ds})\right\}\right]=\frac{g_m}{R_s}\left(1+\frac{sC_{gs}}{g_m}\right)$$

$$\text{or} \quad \frac{V_0}{V_s}\frac{1+g_mR_L}{R_sR_L}\left[1+\frac{R_sR_L}{1+g_mR_L}.s\left\{C_{gd}\left(\frac{1+g_mR_L}{R_L}\right)+C_{gs}\left(-g_m+\frac{1+g_mR_L}{R_L}+\frac{1}{R_s}\right)+C_{ds}\left(\frac{1}{R_s}\right)\right\}\right.$$

$$\left.+\frac{R_sR_L}{1+g_mR_L}\times s^2\{C_{gs}C_{ds}+C_{gd}C_{gs}+C_{gd}C_{ds}\}\right]=\frac{g_m}{R_s}\left(1+\frac{sC_{gs}}{g_m}\right)$$

$$\therefore \quad \frac{V_0}{V_s}.\frac{1+g_mR_L}{R_sR_L}\left[1+s\left(R_sC_{gd}+\frac{R_s+R_L}{1+g_mR_L}C_{gs}+\frac{R_L}{1+g_mR_L}C_{ds}\right)\right.$$

$$\left.+s^2\left(\frac{R_sR_L}{1+g_mR_L}\right)(C_{gd}C_{ds}+C_{ds}C_{gs}+C_{gs}C_{gd})\right]=\frac{g_m}{R_s}\left(1+\frac{sC_{gs}}{g_m}\right)$$

$$\text{or} \quad A_{VH}(s)=\frac{\frac{g_mR_L}{1+g_mR_L}\left(1+\frac{sC_{gs}}{g_m}\right)}{[1+a_1s+a_2s^2]}$$

$$=\frac{A_{VO}(1+sC_{gs}/g_m)}{(1+a_1s+a_2s^2)} \qquad \text{(hence Eq. (10.84a) verified)}$$

where $$A_{VO}=\frac{g_mR_L}{1+g_mR_L}$$

$$a_1=R_sC_{gd}+\frac{R_s+R_L}{1+g_mR_L}C_{gs}+\frac{R_L}{1+g_mR_L}C_{ds}, \text{ (hence Eq. (10.84b) verified)}$$

and $$a_2=\frac{R_sR_L}{1+g_mR_L}(C_{gd}C_{ds}+C_{ds}C_{gs}+C_{gs}C_{gd}) \quad \text{(hence Eq. (10.84c) verified)}$$

$f_H=\frac{1}{2\pi}\omega_H=\frac{1}{2\pi}.\frac{1}{a_1}$ and may be found for specific cases, given the numerical values of various parameters/components.

An alternative method to obtain a_2

We can determine a_2 by an alternative approach as follows:

$$a_2=R_{11}^0C_1R_{22}^1C_2+R_{11}^0C_1R_{33}^1C_3+R_{22}^0C_2R_{33}^2C_3$$

where $C_1=C_{gd}, \quad C_2=C_{gs}, \quad C_3=C_{ds}$

$R_{11}^0=R_s$ (by inspection)

$$R_{22}^0=\frac{(R_s+R_L)}{(1+g_mR_L)} \qquad \text{(see Fig. 10.47)}$$

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$$= \frac{R_s R_L}{1 + g_m R_L}(C_1C_2 + C_2C_3 + C_3C_1)$$

or $$a_2 = \frac{R_s R_L}{1 + g_m R_L}(C_{gd}C_{gs} + C_{gs}C_{ds} + C_{ds}C_{gd}),$$ which is the same as Eq. (10.84c)

Also, $$A_{VO} = \frac{g_m R_L}{1 + g_m R_L}$$

and a zero occurs for $s = \infty$; $V_{gs}SC_{gs} = -g_m V_{gs}$, i.e., $s = \frac{-g_m}{C_{gs}}$.

$$\therefore \quad A_V(s) = \left(\frac{g_m R_L}{1 + g_m R_L}\right)\frac{(1 + sC_{gs}/g_m)}{1 + a_1 s + a_2 s^2}$$

where a_1 and a_2 are found earlier.

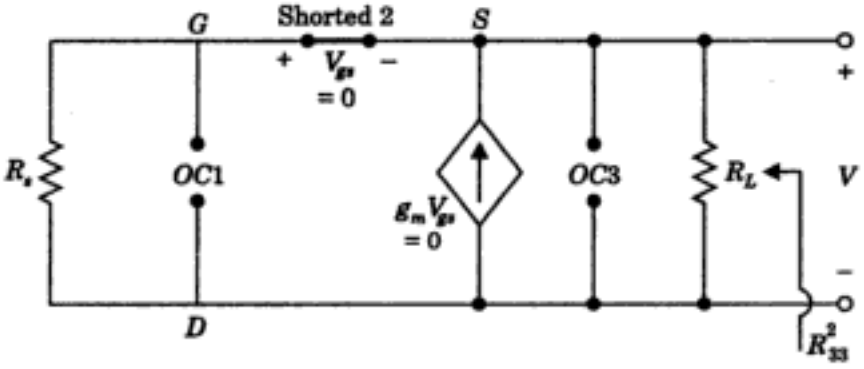


Fig. 10.49 Circuit to find R_{33}^2, clearly, $R_{33}^2 = R_s || R_L$ as $g_m V_{gs} = 0$.

EXAMPLE 10.9

Find the input impedance $Z_i(s)$ and the output impedance $Z_0(s)$ for the Source Follower, at high frequency [i.e., verify Eqs. (10.86) and (10.87)].

Solution: See Fig. 10.50 for equivalent circuit of source follower, and Fig. 10.51 drawn to find the value of $Z_i(s)$. We can see that (Fig. 10.51),

$$Z_i(s) = \left(\frac{1}{sC_{gd}}\right) || Z_1$$

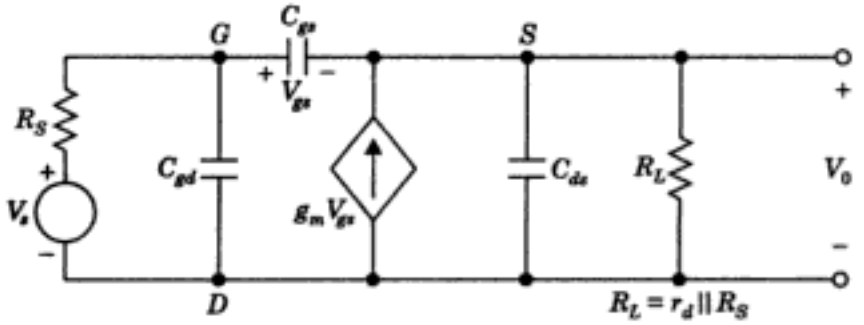


Fig. 10.50 The equivalent circuit of a Source Follower, Ex. 10.9.

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To find Z_1, apply a voltage V_{XX} at XX and let current I_X flows in C_{gs} (with G as +ve and D as –ve).

$$\therefore \quad V_{gs} = I_X \frac{1}{sC_{gs}}$$

and

$$V_{XX} = \left(I_X \cdot \frac{1}{sC_{gs}}\right) + (I_X + g_m V_{gs}) Z_2$$

$$= I_X \frac{1}{sC_{gs}} + I_X \left(1 + g_m \frac{1}{sC_{gs}}\right) Z_2$$

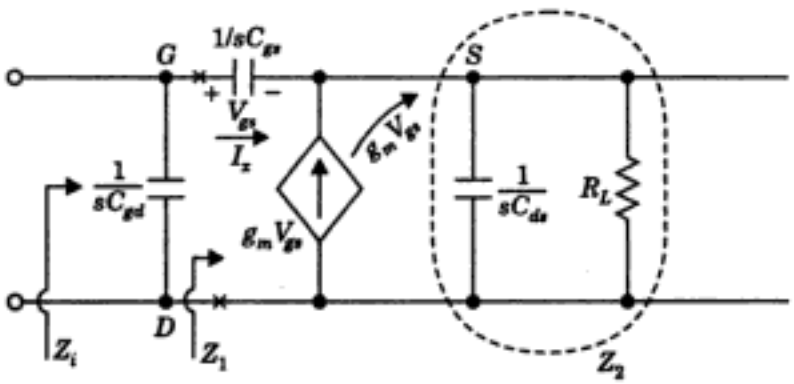


Fig. 10.51 Circuit to find $Z_i(s)$.

Thus,

$$Z_1 = \frac{V_{XX}}{I_X}$$

$$= \frac{1}{sC_{gs}} + Z_2 \left(1 + \frac{g_m}{sC_{gs}}\right)$$

Put

$$Z_2 = \frac{1}{sC_{ds}} \| R_L = \frac{R_L}{1 + sC_{ds}R_L}$$

$$\therefore \quad Z_1 = \frac{1}{sC_{gs}} + \frac{R_L}{1 + sC_{ds}R_L} \cdot \frac{sC_{gs} + g_m}{sC_{gs}} = \frac{(1 + sC_{ds}R_L) + (sC_{gs} + g_m)R_L}{sC_{gs}(1 + sC_{ds}R_L)}$$

$$= \frac{[(1 + g_m R_L) + sR_L(C_{ds} + C_{gs})]}{[sC_{gs}(1 + sC_{ds}R_L)]}$$

or

$$Z_1 = \frac{(1 + g_m R_L)(1 + sR_L(C_{ds} + C_{gs})/(1 + g_m R_L))/(1 + g_m R_L))}{[sC_{gs}\,(1 + sC_{ds}R_L)]}$$

or

$$Z_i(s) = \left(\frac{1}{sC_{gd}}\right) \| Z_1$$

Therefore, Eq. (10.86) has been verified.

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[*To find* $Z_0(s)$]

In Fig. 10.52, we note that

$$R_s \| \frac{1}{sC_{gd}} = Z_4$$

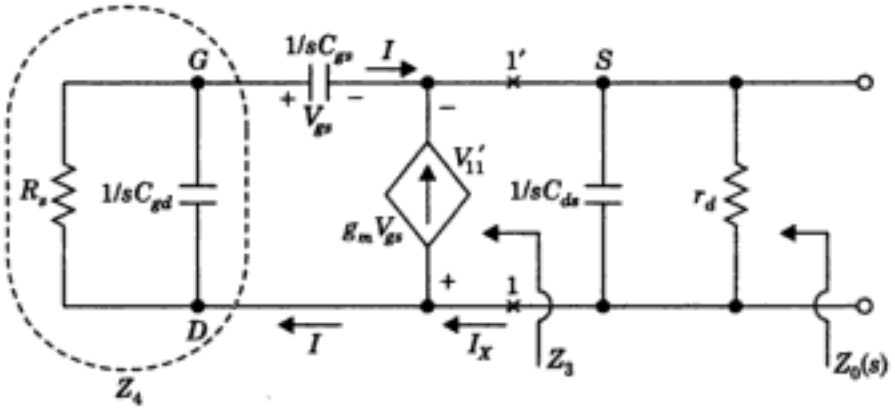


Fig. 10.52 Circuit to find $Z_0(s)$.

$$\therefore \qquad Z_4 = \frac{R_s}{1 + sC_{gd}R_s}$$

To find Z_3, apply a voltage source V_{XX} and let current I flows from G to S (i.e. $\rightarrow$) side if we apply V_{XX} at 11′.

$$\therefore \qquad V_{11}' = I\left(Z_4 + \frac{1}{sC_{gs}}\right) = \frac{I(1 + sC_{gs}Z_4)}{sC_{gs}}$$

$$\therefore \qquad \frac{V_{11}'}{I} = \frac{1 + sC_{gs}Z_4}{sC_{gs}}$$

or $$V_{gs} = I \times \frac{1}{sC_{gs}}$$

and $$I_X = I + g_m V_{gs} = I + g_m \cdot \frac{I}{sC_{gs}} = I\left(1 + \frac{g_m}{sC_{gs}}\right)$$

Thus, $$\frac{V_{11}'}{I_X} = \frac{V'_{11}}{I(1 + g_m/sC_{gs})} = \frac{[(1 + sC_{gs}Z_4)/sC_{gs}]}{(1 + g_m/sC_{gs})} \quad (\because V_{11}' = (1 + sC_{gs}Z_4)/sC_{gs})$$

$$\therefore \qquad Z_3 = \frac{V_{11}'}{I_X} = \frac{1 + sC_{gs}Z_4}{g_m + sC_{gs}} = \frac{1 + sC_{gs}\dfrac{R_s}{1 + sC_{gd}R_s}}{g_m + sC_{gs}}$$

$$= \frac{1 + sC_{gd}R_s + sC_{gs}R_s}{(g_m + sC_{gs})(1 + sC_{gd}R_s)} = \left(\frac{1}{g_m}\right)\frac{1 + sR_s(C_{gd} + C_{gs})}{(1 + sC_{gs}/g_m)(1 + sC_{gd}/R_s)}$$

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When $C_2 = C_3 = 0$ (open circuits), and the circuit contains only C_1 (as shown in Fig. 10.53b), the TF of circuit in Fig. 10.53a has only one pole whose angular frequency (rad/s) is $1/\tau = 1/(R_{11}^0 C_1)$. In Eq. (10.88), for $C_2 = C_3 = 0$, $a_1 = R_{11}^0 C_1$ and $p_1 = 1/a_1 = 1/R_{11}^0 C_1$. Similar arguments apply if we consider $C_3 = C_1 = 0$ and $C_1 = C_2 = 0$ cases, giving time constants $R_{22}^0 C_2$ and $R_{33}^0 C_3$, respectively.

For a system which contains M capacitors, the value of a_1 is given by summation of M open circuit constants due to each capacitor, i.e.,

$$a_1 = \sum_{i=1}^{M} R_{ii}^0 C_i \qquad \text{(open circuit constant)} \tag{10.89}$$

where R_{ii}^0 is the zero-frequency resistance, i.e. putting all capacitances, except C_i, equal to zero, as seen by C_i. Hence a_1 is the sum of open circuit time constants, with $R_{ii}^0 C_i$ being the circuit time constant when all the *other capacitances are open circuited.*

10.18.2 The Coefficient a_2

To perform the approximate frequency analysis, we need that pole p_2 must be away from pole p_1 such that $p_2 > 8p_1$. The location of the closest non-dominant pole given by p_2 and, therefore, the separation between the dominant and the non-dominant poles, is determined by a_2. We have seen that a_2 comprises the product of time constants. All possible pairs of capacitances from the time constants in a_2. For circuit in Fig. 10.54 we have

$$a_2 = (R_{11}^0 C_1)(R_{22}^1 C_2) + (R_{11}^0 C_1)(R_{33}^1 C_3) + (R_{22}^0 C_2)(R_{33}^2 C_3) \tag{10.90}$$

where R_{ii}^j is zero frequency resistance seen by C_i when C_j is short-circuited and other capacitors open circuited.

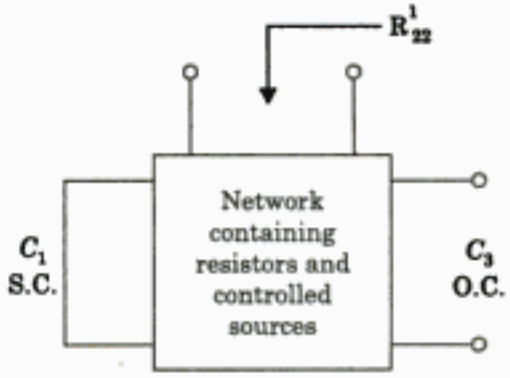


Fig. 10.54 Network in figure used to define R_{22}^1. C_1 is short-circuited and C_3 is open circuited.

$R_{11}^0 C_1, R_{22}^0 C_2$ are the open circuit time constants, $R_{22}^1 C_2, R_{33}^1 C_3$ and $R_{33}^2 C_3$ etc. are short circuit constants. For example, R_{11}^0 is resistance seen by C_1 when C_2, C_3 (i.e. all other capacitors) are open circuited, R_{22}^1 is resistance seen by C_2 when C_1 is shorted and C_3 (and all other capacitors) are open circuited.

The subscript in R_{ii}^j (i.e., ii) indicates the terminals at which the resistance is computed and *the superscript (i.e. j) indicates the capacitance which is shorted. All the capacitances not indicated either in subscript or in the superscript are open circuited. Each term in Eq. (10.90) is the product of one open circuited and one short circuited time constant.*

Also, for any pair of capacitors C_i and C_j, we have the product of one short circuit time constant (e.g. $R_{ii}^{j} C_i$) and the other open circuit time constant, i.e., $R_{ii}^{0} C_j$. Note that

$$\boxed{(R_{ii}^{0} C_i)(R_{jj}^{i} C_j) = (R_{ii}^{j} C_i)(R_{jj}^{0} C_j)} \tag{10.91}$$

i.e., the capacitor that is shorted to determine R_{jj}^{i} (on LHS of Eq. (10.91)) is the one for which open-circuit time constant $R_{ii}^{(0)} C_i$ is computed. These two subterms constitute the term $(R_{ii}^{0} C_i)(C_{jj}^{i} C_j)$ in LHS of Eq. (10.91).

Similarly, the value $R_{22}^{0} C_2 \, . \, R_{33}^{2} C_3$ can be replaced by $R_{22}^{3} C_2 \, . \, R_{33}^{0} C_3$. Depending upon the circuit/convenience, we find the product term with one OC time constant and the other SC time constant. This point will be clear from the following examples:

EXAMPLE 10.10

Determine the coefficient a_1 in the transfer function of the Common Emitter stage by time constant method.

Solution

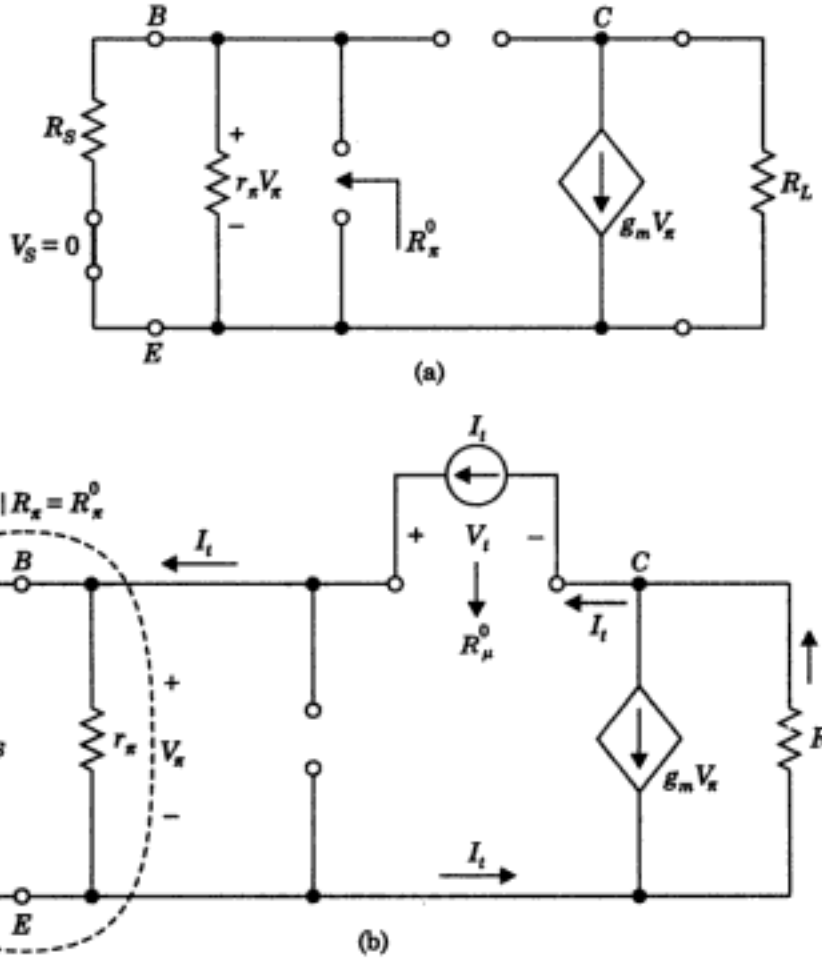


Fig. 10.55 (a) Circuit used to compute the zero-frequency (open circuit) resistance R_π^0 for the CE stage, and (b) R_μ^0 for the CE stage for Ex. 10.10.

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As $$a_1 = \sum_{i=1}^{M} R_{ii} C_i = R_\pi^0 C_\pi + R_\mu^0 C_\mu + R_\mu^0 C_\mu \quad \text{(Eq. (10.88))}$$

To obtain R_π^0, open circuit C_μ and make $V_S = 0$. Circuit (a) is obtained. We find impedance R_π^0 from Fig. 10.55a as

$$R_\pi^0 = R_S \,||\, r_\pi = \frac{r_\pi R_S}{r_\pi + R_S}$$

To find R_μ^0, open circuit C_π, put $V_S = 0$. Apply a test current I_t as shown in Fig. 10.55(b). Let voltage V_t be developed across the base (B) and the collector (C). Then

$$V_t = I_t(R_S \,||\, r_\pi) + R_L(I_t + g_m V_\pi)$$
$$= I_t [R_\pi^0 + R_L(1 + g_m R_\pi^0)]$$
$$(\because\ R_S \,||\, r_\pi = R_\pi^0, \text{ and } V_\pi = I_t \,.\, R_\pi^0)$$

or $$V_t = I_t [R_\pi^0 (1 + g_m R_L) + R_L]$$

$\therefore$ $$R_\mu^0 = \frac{V_t}{I_t} = R_\pi^0 (1 + g_m R_L) + R_L$$

Hence $$a_1 = R_\pi^0 C_\pi + R_\mu^0 C_\mu$$
$$= R_\pi^0 C_\pi + [R_\pi^0 (1 + g_m R_L) + R_L] C_\mu \quad \textbf{Ans.}$$

Note that we had obtained the same value of a_1 by direct method as given in Eq. (10.55). (see the coefficient of s in the expression in denominator of Eq. (11.55)).

EXAMPLE 10.11

Determine the a_2 coefficient for the circuit [see Fig. 10.56] by time constant method.

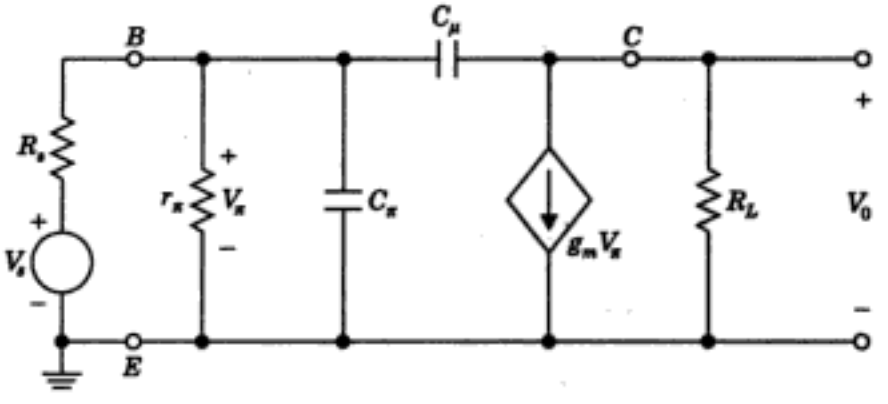


Fig. 10.56 The given circuit (a *CE* stage at high frequency), Ex. 10.11

Solution: This circuit contains two capacitors. Hence,

$$a_2 = R_\pi^0 C_\pi R_\mu^\pi C_\mu = R_\pi^\mu C_\pi R_\mu^0 C_\mu \quad \text{(Eq. (10.90) if } C_3 \text{ is made zero)}$$

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The source resistance for the second stage is the output resistance (R'_{01}) of the first stage. Clearly, $R'_{01} = R_{C1}$. Also

$$\left.\begin{aligned} R^0_{\pi 2} &= R^0_{33} = R_{C1} \| r_{\pi 2} && \text{(by inspection)} \\ R^0_{\mu 2} &= R^0_{44} = R^0_{33}(1 + g_{m2}R_{C2}) + R_{C2} && \text{(using (10.58))} \\ &= R^0_{33} + R_{C2}(1 + g_{m2}R^0_{33}) \end{aligned}\right\} \quad (10.94)$$

If $r_b = 0$, $\quad R_{L1} = R_{C2} \| r_{\pi 2} = R^0_{\pi 2} = R^0_{33}$

Using Eqs. (10.92), (10.93) and (10.94), we have

$$a_1 = \sum_{i=1}^{M} R^0_{ii} C_i \quad (10.95)$$

$$= R^0_{11} C_1 + R^0_{22} C_2 + R^0_{33} C_3 + R^0_{44} C_4$$

$$= R^0_{11} C_1 + [R^0_{11}(1 + g_{m1}R_{L1}) + R_{L1}]C_2 + R^0_{33} C_3 + [R^0_{33}(1 + g_{m2}R_{C2}) + R_{C2}]C_4 \quad (10.96)$$

The first two terms of Eq. (10.96) when added, give a_1 of Stage 1, i.e., a_{11} (see Eq. (10.55)), and the last two terms are 'a_1' of Stage 2, i.e., a_{12}. Thus,

$$a_1 = a_{11} + a_{12} \quad (10.97)$$

Now,
$$f_H = \frac{1}{2\pi a_1} = \frac{1}{2\pi}\left(\frac{1}{a_{11} + a_{12}}\right) \quad (10.98)$$

$\therefore$
$$\frac{1}{f_H} = \frac{1}{f_{H1}} + \frac{1}{f_{H2}} \quad (10.99)$$

Clearly, f_H is smaller than either f_{H1} and f_{H2}.

Thus the half power point frequency f_H of the cascaded stage is smaller than either f_{H1} or f_{H2}. *Therefore, the cascading stages decrease the bandwidth.*

The reduction of the bandwidth is an 'additive' process as seen in Eq. (10.99), whereas the midband gain increases multiplicatively. Thus, for numbers greater than unity, their product increases more rapidly than their sum. Hence the gain-bandwidth product of the cascade is more than that of an individual stage. For example, $A_1 = 100$, $f_{H1} = 0.1$ MHz for 1st stage and $A_2 = 10$, $f_{H2} = 1$ MHz for 2nd stage. Each stage has gain-bandwidth of 10. If we cascade them, then

$$f_H = \frac{0.1 \times 1}{0.1 + 1} = 0.091$$

and
$$A_1 A_2 = 100 \times 10 = 1000$$

Cascade stage has gain-BW product = $0.091 \times 1000 = 91$.

For N-stage cascaded amplifier, a_1 coefficient of the cascade is the sum of a_1 coefficients of the individual stages

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$$a_1 = \sum_{i=1}^{N} a_{1i} \qquad (10.100)^{**}$$

where a_{1i} = a_1 coefficient of the ith stage.

EXAMPLE 10.12

The parameters used in the *CE-CE* cascade in Fig. 10.59 are as follows:

$R_s = 600\ \Omega$, $R_{C1} = 1.5\ \text{k}\Omega$, $R_{C2} = 600\ \Omega$, $r_{\pi 1} = 1.2\ \text{k}\Omega$,
$g_{m1} = 0.1\ \text{℧}$, $C_1 = C_{\pi 1} = 24.5\ \text{pF}$, $C_2 = C_{\mu 1} = 0.5\ \text{pF}$, $r_{\pi 2} = 2.4\ \text{k}\Omega$,
$g_{m2} = 0.05\ \text{℧}$, $C_3 = C_{\pi 2} = 19.5\ \text{pF}$ and $C_4 = C_{\mu 2} = 0.5\ \text{pF}$

(a) Determine the approximate value of f_H and the approximate location of the dominant pole.

(b) Determine the approximate location of the closest non-dominant pole and comment on the validity of the dominant-pole approximation.

Solution: We use Eqs. (10.93a) and (10.93b).

(a) We first evaluate the resistances (see Fig. 10.60)

$$R_{\pi 1}^0 = R_{11}^0 = R_s \,\|\, r_{\pi 1}$$
$$= 600 \,\|\, 1200 = 0.40\ \text{k}\Omega \qquad \text{[From Eq. (10.93a)]}$$
$$R_{L1} = R_{C1} \,\|\, r_{\pi 2}$$
$$= 1500 \,\|\, 2400 = 0.923\ \text{k}\Omega$$

and
$$R_{\mu 1}^0 = R_{22}^0$$
$$= R_{11}^0 (1 + g_{m1} R_{L1}) + R_{L1} \qquad \text{[From Eq. (10.93b)]}$$
$$= 0.4(1 + 0.1 \times 923) + 0.923 = 38.2\ \text{k}\Omega$$

**For n numbers $a_1, a_2, \ldots, a_n$, if each $a_i \geq n^{\left(\frac{1}{n-1}\right)}$, then their product $\prod_{i=1}^{n} a_i \geq \sum_{i=1}^{n} a_i$. For $n = 2$, $a_i \geq 2$. For amplifier stages, usually, both the gain and bandwidth are greater than 2.

Let $a_i = Kn^{1/(n-1)}$

Product $P = \prod_{i=1}^{n} a_i = K^n n^{n/(1-n)}$

Sum $S = \sum_{i=1}^{n} a_i = nKn^{1/(n-1)}$

$\therefore$ $\frac{P}{S} = \frac{K^n n^{n/(1-n)}}{nKn^{1/(1-n)}} = K^{n-1} > 1$ if K i.e. the product P is more than the sum S.

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$$R^0_{\pi 2} = R^0_{33} = R_{C1} \| r_{\pi 2}$$

$$= 1500 \| 2400 = 0.923 \text{ k}\Omega \qquad \text{[From Eq. (10.94)]}$$

$$R^0_{\mu 2} = R^0_{44} = R^0_{33}(1 + g_{m2}R_{C2}) + R_{C2}$$

$$= 0.923(1 + 0.05 \times 600) + 0.60 = 29.2 \text{ k}\Omega$$

Using Eq. (10.100), we write

$$a_1 = \sum_{i=1}^{4} R^0_{ii} C_i$$

$$= R^0_{11}C_1 + R^0_{22}C_2 + R^0_{33}C_3 + R^0_{44}C_4$$

$$= (0.40 \times 24.5) + (38.2 \times 0.5) + (0.923 \times 19.5) + (29.2 \times 0.5)$$

$$= 61.5 \text{ ns}$$

$$\therefore \quad f_H = \frac{1}{2\pi a_1}$$

$$= \frac{1}{2\pi \times 61.5 \times 10^{-9}} = 2.59 \text{ MHz} \qquad \text{(i)}$$

The dominant pole is located at $-p_1$, where

$$p_1 = \frac{1}{a_1}$$

$$= \frac{1}{61.5 \times 10^{-9}} = 1.63 \times 10^7 \text{ rad/s}$$

Let us also determine the values of f_{H1} and f_{H2}.

As

$$a_{11} = R^0_{11}C_1 + R^0_{22}C_2$$

$$= (0.40 \times 24.5) + (38.2 \times 0.5) = 28.9 \text{ ns}$$

$$a_{12} = R^0_{33}C_3 + R^0_{44}C_4$$

$$= (0.923 \times 19.5) + (29.2 \times 0.5) = 32.6 \text{ ns}$$

$$\therefore \quad f_{H1} = \frac{1}{2\pi a_{11}} = \frac{1}{2\pi \times 28.9 \times 10^{-9}} = 5.51 \text{ MHz}$$

and

$$f_{H2} = \frac{1}{2\pi a_{12}} = \frac{1}{2\pi \times 32.6 \times 10^{-9}} = 4.88 \text{ MHz}$$

Check

$$f_H = \frac{f_{H1} \times f_{H2}}{f_{H1} + f_{H2}}$$

$$= \frac{5.51 \times 4.88}{5.51 + 4.88} = 2.59 \text{ MHz, same as found in (i)}$$

Thus, it is seen that f_H of the cascade is less than 60% of f_{H2}, the smaller of the two f_{H1} and f_{H2}. Let us now see the gain bandwidth product of the cascade.

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Also, note that $R_{33}^1 = R_{33}^0; R_{44}^1 = R_{44}^0$. We observe that when C_2 is open circuited, the portion of the circuit containing C_1 is decoupled from Stage 2 (C_3 and C_4). The resistances seen by C_3 and C_4 are thus independent of whether C_1 is open circuited or short circuited if C_2 is open circuited. Thus,

$$R_{33}^1 \ (C_1 \text{ short, all other } C_i \text{ open}) = R_{33}^0$$

$$R_{44}^1 \ (C_1 \text{ short, all other } C_i \text{ open}) = R_{44}^0$$

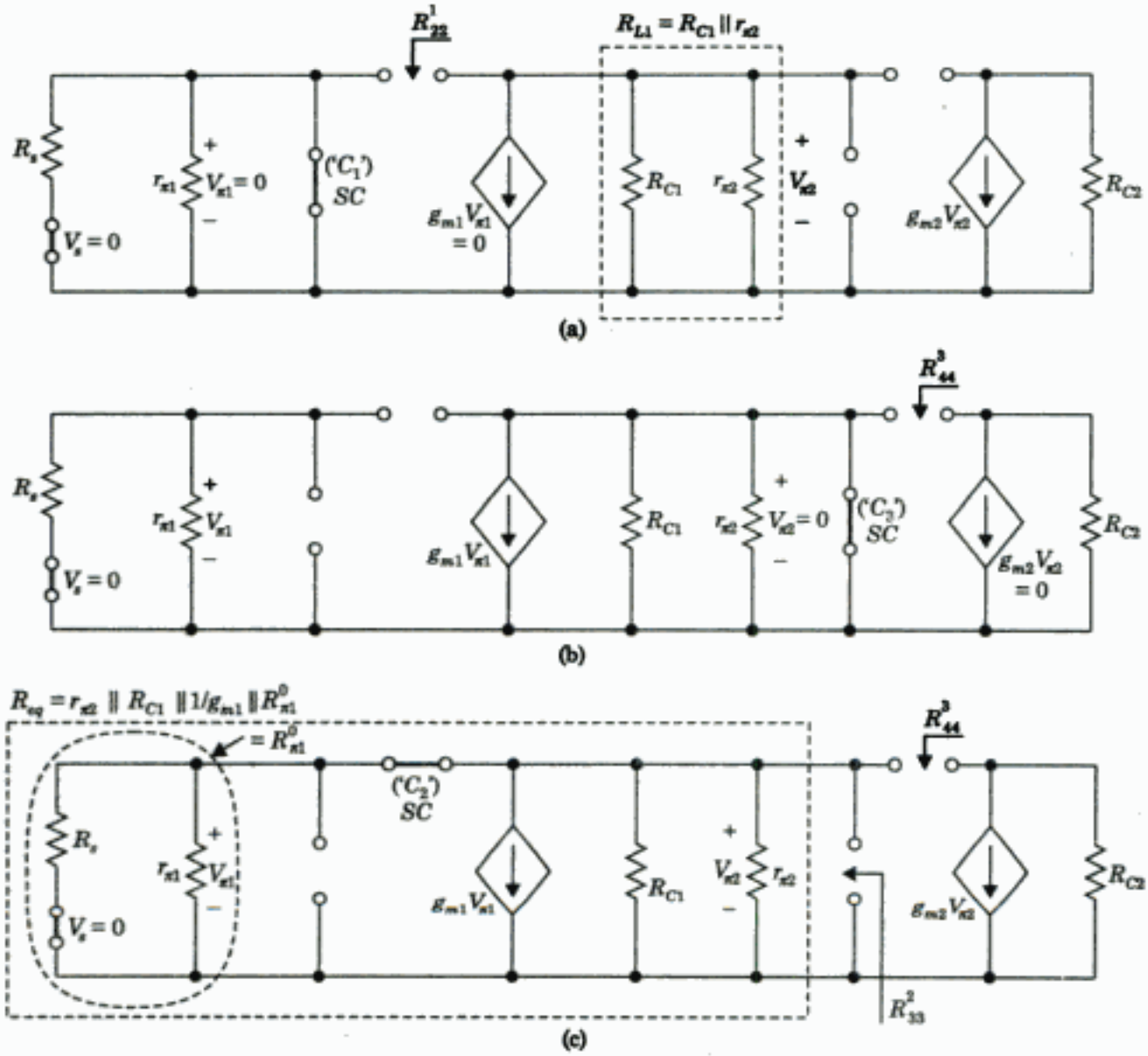


Fig. 10.61 Equivalent circuits used to calculate the values of (a) R_{22}^1, (b) R_{44}^3, (c) R_{44}^2, R_{33}^2, for Example 10.12.

Hence, we only need to find $R_{22}^1, R_{33}^2, R_{44}^2$ and R_{44}^3 to calculate a_2 in toto. R_{22}^1 may be computed from Fig. 10.61(a). Clearly,

$$R_{22}^1 = R_{C1} \| r_{\pi 2} = R_{L1}$$

From Fig. 10.61(b),

$$R_{44}^3 = R_{C2} \qquad (\because \ V_{\pi 2} = 0 \text{ and } C_3 \text{ is short circuited})$$

From Fig. 10.61(c), short circuiting C_2, gives

$$R_{33}^2 = r_{\pi 2} \,||\, R_{C1} \,||\, \frac{1}{g_{m1}} \,||\, R_{\pi 1}^0 \quad (\text{where } R_{\pi 1}^0 = R_s \,||\, r_{\pi 1})$$

and, therefore, $R_{44}^2 = R_{33}^2 (1 + g_{m2} R_{C2}) + R_{C2}$

Thus, we have all the values

$$R_{11}^0 = R_{\pi 1}^0 = R_s \,||\, r_{\pi 1} = 600 \,||\, 1200 = 0.40 \text{ k}\Omega$$

$$R_{22}^1 = R_{C1} \,||\, r_{\pi 2} = R_{L1} = 1500 \,||\, 2400 = 0.923 \text{ k}\Omega$$

$$R_{33}^1 = R_{33}^0 = R_{C1} \,||\, r_{\pi 2} = 1500 \,||\, 2400 = 0.923 \text{ k}\Omega$$

$$R_{44}^1 = R_{44}^0 = 29.2 \, k\Omega \quad \text{[found in Part (a)]}$$

Now, $R_{33}^2 = r_{\pi 2} \,||\, R_{C1} \,||\, \frac{1}{g_{m1}} \,||\, R_{11}^0$

$$= 2.4 \text{ k}\Omega \,||\, 1.5 \text{ k}\Omega \,||\, 0.01 \text{ k}\Omega \,||\, 0.4 \text{ k}\Omega \qquad \left(\because \frac{1}{g_{m1}} = 0.01 \text{ k}\Omega\right)$$

$\therefore$ $$= 0.0096 \approx 0.01 \text{ k}\Omega$$

and $R_{44}^2 = R_{33}^2 (1 + g_{m2} R_{C2}) + R_{C2}$ [i.e. $R_{44}^2 = R_{33}^2 + R_{C2}(1 + g_{m2} R_{33}^2)$]

$$= 0.01(1 + 0.05 \times 600) + 0.6 = 0.91 \text{ k}\Omega$$

$$R_{44}^3 = R_{C2} = 0.6 \text{ k}\Omega$$

$\therefore$ $$a_2 = R_{11}^0 C_1 [R_{22}^1 C_2 + R_{33}^0 C_3 + R_{44}^0 C_4] + R_{22}^0 C_2 [R_{33}^2 C_3 + R_{44}^2 C_4] + R_{33}^0 C_3 R_{44}^3 C_4$$

$$= 0.40 \times 24.5[0.923 \times 0.5 + 0.923 \times 19.5 + 29.2 \times 0.5]$$

$$+ 38.2 \times 0.5[0.01 \times 19.5 + 0.91 \times 0.5] + 0.923 \times 19.5 \times 0.6 \times 0.5$$

$$= 9.8(33.06) + 19.1(0.65) + 18.2985 = 341.8 \approx 342 \times 10^{-18} \text{ sec}^2$$

$\therefore$ $$p_2 = \frac{a_1}{a_2} = \frac{61.5 \times 10^{-9}}{342 \times 10^{-18}} = 1.8 \times 10^8 \text{ rad/s}$$

Thus, $$f_2 = \frac{1}{2\pi} p_2 = \frac{1.8 \times 10^8}{2 \times \pi} = 28.6 \text{ MHz}$$

As the poles are separated by a factor $\frac{p_2}{p_1} = \frac{1.8 \times 10^8}{0.163 \times 10^8} \cong 11$, i.e. more than 8, we can conclude that the dominant-pole approximation is valid, within an error of ± 10%.

Note that the dominant pole time-constant method is a pessimistic approximation and yields the values of f_{H1} and f_{H2} about 10% lower than the exact f_{H1} and f_{H2}, respectively.

A second observation is as follows:

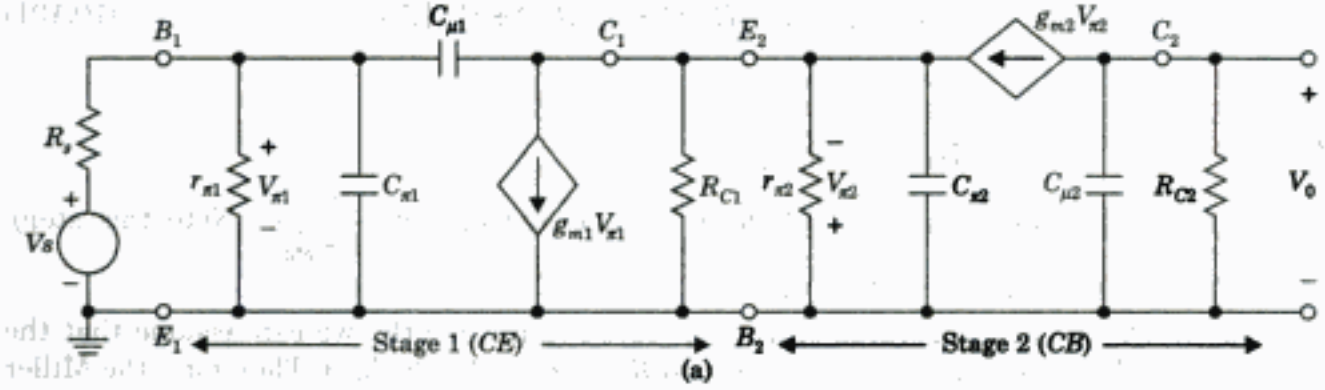
Individual stage has f_{H1} = 5.51 MHz and f_{H2} = 4.88 MHz.

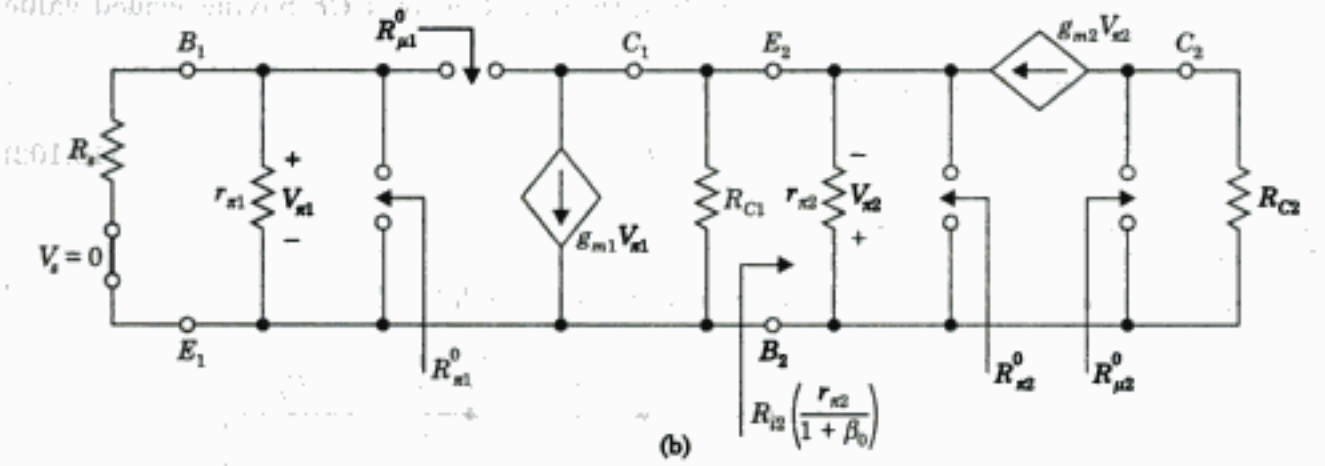
The cascaded stage has f_H = 2.59 MHz and its second pole frequency is 28.6 MHz. Hence, *one pole has moved closer to the origin and the other, further away*. This condition is often referred to as **pole splitting** and is often exploited in compensating operational amplifiers.

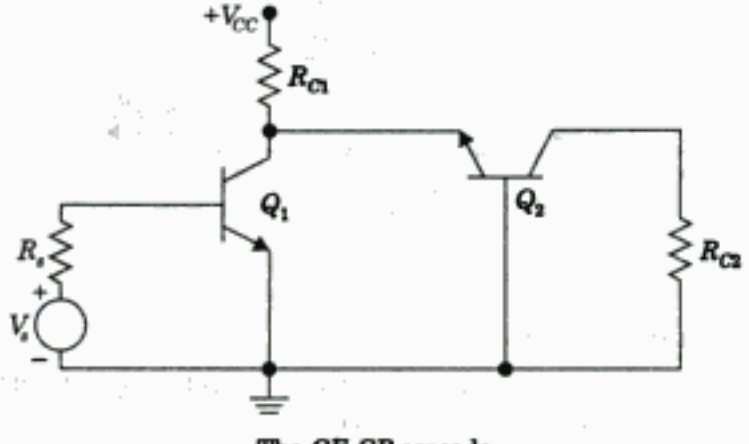
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10.20 THE CASCODE (*CE-CB*) AMPLIFIER

The cascode amplifier comprises of a Common Emitter stage cascaded with a **Common Base****. The midband gain of this combination is virtually **the same as** the gain of a ***CE*** **stage having** the same load resistance R_{C2} as **does** the *CB* stage. **The bandwidth of the frequency response of** the composite (cascode amplifier) **is greater than that obtained for the corresponding *CE* stage.**







The *CE-CB* cascode

Fig. 10.62 (a) The high-frequency equivalent of the cascode (*CE-CB* cascade)
(b) Circuit used to calculate $R^0_{\pi 1}, R^0_{\pi 2}, R^0_{\mu 2}$ etc.
(c) The basic connection of the cascode amplifier.

**Some authors have also described a *CC-CB* cascade as CASCODE. However, the most popular configuration CASCODE is CE-CB cascade, as assumed by us.

The high frequency equivalent circuit of the cascode is shown in Fig. 10.62(a) and that used to evaluate open-circuit resistances is given in Fig. 10.62(b). Figure 10.62(c) is the basic connection for the cascode amplifier.

Now, coeff. a_1 of the cascode = coeff. a_1 of *CE* (loaded) + coeff. a_1 of *CB* stage

i.e. $$a_1 = a_{11} + a_{12} \quad \text{(say)}$$

Then for the *CE* stage,

$$a_{11} = R_{\pi 1}^0 C_{\pi 1} + [R_{\pi 1}^0 (1 + g_{m1} R_{L1}) + R_{L1}] C_{\mu 1} \tag{10.101}$$

where $$R_{\pi 1}^0 = R_s \,\|\, r_{\pi 1}$$

$$R_{L1} = R_{C1} \,\|\, R_{i2}$$

where R_{i2} is the input resistance of the CB stage and equals $\frac{r_{\pi 2}}{(1+\beta_0)}$ (Note this step).

Since $R_{i2} << R_{C1}$, therefore $R_{L1} \approx R_{i2}$.

Due to $R_{L1} << R_{C1}$, the value of a_{11} is reduced (Equivalently, we can assume that the loaded gain of the *CE* stage is reduced due to $R_{L1} = R_{i2} \,\|\, R_{C1} << R_{C1}$). Therefore, the Miller effect multiplication of $C_{\mu 1}$ is reduced significantly from that of a *CE* having loaded value $R_{L1} = R_{C1}$.

It can be shown** that for the *CB* stage

$$\boxed{a_{12} = \frac{1}{\omega_T} + C_{\mu 2} R_{C2}} \tag{10.102}$$

****Proof**

To find a_1 coefficient for Stage 2 (redrawn from Fig. 10.62a)

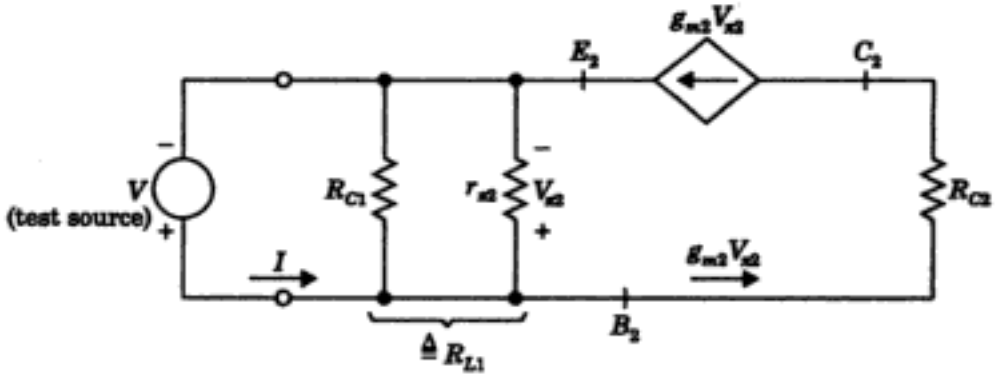


Fig. (a) To find $R_{\pi_2}^0$.

[*To find* $R_{\pi 2}^0$, *open circuit* $C_{\mu 2}$, *see Fig. (a)*]

$$V_{\pi 2} = (I - g_{m2} V_{\pi 2})\, R_{L1} \qquad \text{(put } V_{\pi 2} = V \text{ the test source voltage)}$$

$$\therefore \quad V(1 + g_{m2} R_{L1}) = I R_{L1}$$

$$\therefore \quad R_{\pi 2}^0 = \frac{V}{I} = \frac{R_{L1}}{(1 + g_{m2} R_{L1})} \approx \frac{1}{g_{m2}} = \frac{r_{\pi 2}}{\beta_{02}}$$

$$\therefore \quad R_{\pi 2}^0 = \frac{r_{\pi 2}}{\beta_{02}}$$

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The frequency $f_{H2} = \dfrac{1}{2\pi a_{12}}$ is comparable to $\tilde{f}_H \left(= \dfrac{1}{2\pi \tilde{a}_1} \right)$ where $\tilde{a}_1$ and $\tilde{f}_H$ correspond to an emitter follower. As f_{H2} (for the *CB* stage) is very high, therefore the effect of a_{12} (i.e., of f_{H2}) on the overall response $f_H = \dfrac{1}{2\pi a_1}$ of the cascode stage is minimal.

EXAMPLE 10.13

A cascode amplifier has $R_{C1} = R_{C2} = 1.5$ kΩ and $R_s = 300$ Ω. The transistors are identical and have $r_\pi = 2$ kΩ, $g_m = 0.05$ ℧, $\beta_0 = 100$, $C_\pi = 19.5$ pF, $C_\mu = 0.5$ pF and $\omega_T = 2.5 \times 10^9$ rad/sec. (a) Find f_H for the circuit. (b) Determine f_H for a common-emitter stage having $R_C = 1.5$ kΩ, driven from a source having $R_s = 300$ Ω and using the transistor whose parameters are given above. Compare the result with that obtained in part (a).

Solution: (a) *For the CE stage,*

Contd.

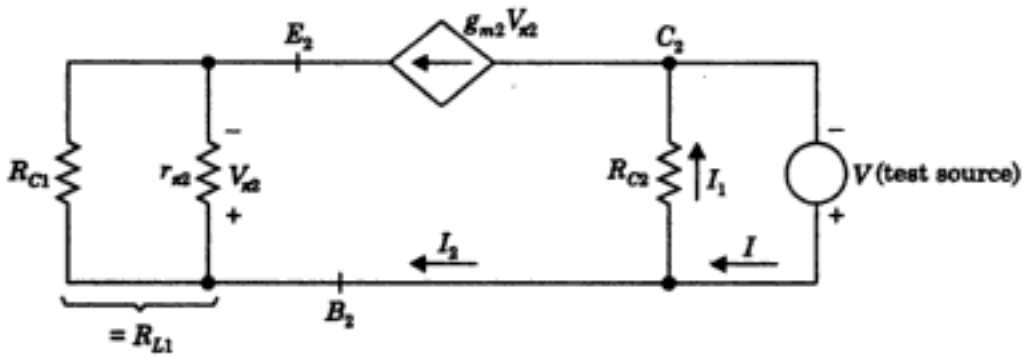


Fig. (b) To find $R^0_{\mu_2}$.

[To find $R^0_{\mu 2}$, open circuit $C_{\pi 2}$, see Fig. (b)]

As $\quad R_{L1} I_2 = V_{\pi 2} = (-g_{m2} V_{\pi 2}) R_{L1}$

$\therefore \quad V_{\pi 2}(1 + g_{m2} R_{L1}) = 0 \quad \therefore \quad V_{\pi 2} = 0 \quad \therefore \quad I_2 = 0$

or $\quad \dfrac{V}{I} = \dfrac{V}{I_1 + 0} = R_{C2}$

i.e. $\quad R^0_{\mu 2} = R_{C2}$

[To find a_{12}] $\quad a_{12} = R^0_{\pi 2} C_{\pi 2} + R^0_{\pi 2} C_{\mu 2}$

$$= \frac{r_{\pi 2}}{\beta_{02}} C_{\pi 2} + R_{C2} C_{\mu 2}$$

$$= \frac{1}{\omega_T} + C_{\mu 2} R_{C2} \qquad \left(\because \omega_T = \frac{\beta_0}{r_\pi (C_\pi + C_\mu)} \approx \frac{g_m}{C_\pi} \text{ from Eq. (10.43a)} \right)$$

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$$R_{\pi 1}^0 = R_s \,||\, r_{\pi 1} = 0.30 \,||\, 2.0 = 0.261\ \text{k}\Omega$$

For the common base,

$$R_{i2} = \frac{r_{\pi 2}}{1+\beta_0} = \frac{2.0}{1+100} = 0.0198\ \text{k}\Omega$$

$\therefore$ 'R_{L1}' of Stage 1 (CE) = $R_{C1} \,||\, R_{i2}$

$$= 1.5 \,||\, 0.0198 = 0.0195\ \text{k}\Omega$$

Hence $$a_{11} = R_{\pi 1}^0 C_{\pi 1} + [R_{\pi 1}^0 (1 + g_{m1} R_{L1}) + R_{L1}] C_{\mu 1}$$

$$= 0.261 \times 19.5 + [0.261(1 + 0.05 \times 19.5) + 0.0195] \times 0.5$$

$$= 5.36\ \text{ns}$$

For CB stage,

$$a_{12} = \frac{1}{\omega_T} + C_{\mu 2} R_{C2} \qquad \text{(Eqn. (10.102))}$$

$$= \frac{1}{2.5 \times 10^9} + 0.5 \times 1.5 \times 10^{-9} = 1.15\ \text{ns}$$

For the CE–CB stage: $a_1 = a_{11} + a_{12}$

$$= 5.36 + 1.15 = 6.51\ \text{ns}$$

and hence $$f_H = \frac{1}{2\pi a_1} = \frac{10^9}{2\pi \times 6.51} = 24.44\ \text{MHz}$$ (for the cascode) ***Ans.***

(b) For the equivalent *CE* stage if *CB* stage were not there

$$a_1 = R_{\pi 1}^0 C_{\pi 1} + [R_{\pi 1}^0 (1 + g_{m1} R_{C1}) + R_{C1}] C_{\mu 1}$$

$$= 0.261 \times 19.5 + [0.261(1 + 0.05 \times 1500) + 1.5]0.5$$

$$= 15.75\ \text{ns}$$

$\therefore$ $$f_H = \frac{1}{2\pi a_1} = \frac{1}{2\pi \times 15.75 \times 10^{-9}} = 10.10\ \text{MHz}$$ (for *CE* alone)

Clearly, the cascode amplifier has a higher f_H (by a factor 24.44/10.1 = 2.4) than does the *CE* stage. If the load resistance R_{C2} = 5 kΩ then

$$a_{12} = \frac{1}{\omega_T} + C_{\mu 2} R_{C2}$$

$$= \frac{1}{2.4 \times 10^9} + 0.5 \times 5 \times 10^{-9} = 2.916$$

and $$a_1 = a_{11} + a_{12} = 5.36 + 2.916 = 8.276\ \text{ns}$$

$\therefore$ Cascode $$f_H = \frac{1}{2\pi a_1} = \frac{10^9}{2\pi \times 8.276} = 19.23\ \text{MHz}$$

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When $\frac{1}{\omega C_E} = 0$ then from Fig. 10.64.

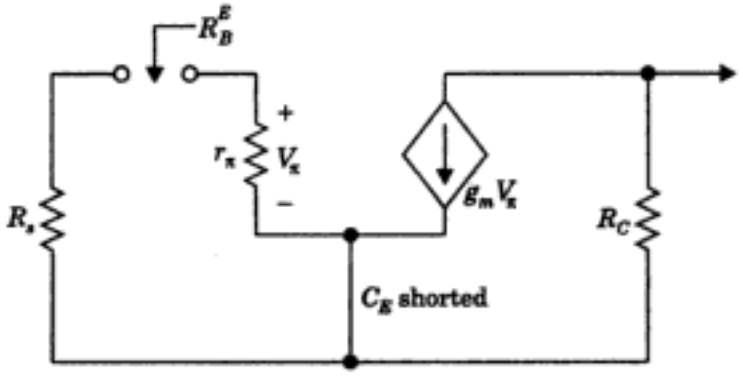


Fig. 10.64 To find R_B^E with $C_E \to \infty$ $\therefore$ $\frac{1}{\omega C_E} = 0\,(5\,C)$.

$$I_b = \frac{V_S}{\underbrace{\left(R_s + r_\pi\right)}_{R_B^E} + \frac{1}{sC_B}} \qquad (\because C_E \text{ offers short circuit, connecting point } E \text{ to ground})$$

$$= \frac{V_s}{\left(R_B^E + \frac{1}{sC_B}\right)} \qquad (\because R_s + r_\pi = R_B^E)$$

Then

$$V_\pi = I_b r_\pi = \frac{V_s \,.\, r_\pi}{\left(R_B^E + \frac{1}{sC_B}\right)}$$

$$V_0(s) = -g_m V_\pi \,.\, R_C = \frac{-g_m \,.\, R_C \,.\, V_s r_\pi}{\left(R_B^E + \frac{1}{sC_B}\right)}$$

$$= \left[\frac{-g_m r_\pi R_C C_B s}{(1 + sR_B^E C_B)}\right] V_s$$

$\therefore$

$$A_{VL}(s) = \frac{V_0(s)}{V_s(s)} = \frac{-g_m R_C \,.\, r_\pi sC_B}{(1 + sR_B^E C_B)}$$

$$= \frac{-g_m R_C \,.\, \frac{r_\pi}{R_s + r_\pi}(R_s + r_\pi)\, sC_B}{1 + sR_B^E C_B}$$

But

$$\frac{-g_m r_\pi R_C}{(R_s + r_\pi)} = \frac{-\beta_0 R_C}{(R_s + r_\pi)} = A_{V0}, \text{ the mid band gain}$$

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$$Z_E = \infty \quad \text{if} \quad 1 = sC_E R_E = 0 \quad \text{i.e.} \quad \text{if } s = -\frac{1}{R_E C_E}$$

$$\therefore \quad \boxed{Z_1 = \frac{+1}{R_E C_E} = \omega_E} \tag{10.105}$$

For the case CE with R_E (and no C_E across R_E) we have the TF gain by

$$A_V = \frac{-\beta_0 R_C}{R_s + r_\pi + (\beta_0 + 1)R_E} \tag{10.106}$$

For our case here when $C_E \neq \infty$, we replace R_E by $R_E \| C_E$, i.e., we here replace R_E by $\frac{R_E}{1 + sR_E C_E}$ in Eq. (10.106) for our case. Doing so, we get

$$A_{VL}(s) = \frac{-\beta_0 R_C}{R_s + r_\pi + (\beta_0 + 1).\dfrac{R_E}{(1 + sC_E R_E)}}$$

$$= \frac{-\beta_0 R_C (1 + sC_E R_E)}{(R_s + r_\pi)(1 + sC_E R_E) + (\beta_0 + 1)R_E}$$

$$= \frac{-\beta_0 R_C}{R_s + r_\pi + (\beta_0 + 1)R_E} \times \frac{(1 + sC_E R_E)}{1 + \dfrac{s(R_s + r_\pi)R_E C_E}{R_s + r_\pi + (\beta_0 + 1)R_E}}$$

$$= \frac{-\beta_0 R_C}{R_s + r_\pi} \times \underbrace{\frac{(R_s + r_\pi)}{R_s + r_\pi + (\beta_0 + 1)R_E} \times \frac{R_E}{R_E}}_{= R_E^B \text{ (see Eq. 10.112)}} \times \frac{(1 + sC_E R_E)}{1 + sC_E \dfrac{(R_s + r_\pi)R_E}{R_s + r_\pi + (\beta_0 + 1)R_E}}$$

$$= \frac{A_{V0}(R_E^B / R_E)(1 + s/\omega_E)}{1 + sR_E^B C_E}$$

Hence

$$A_{VL}(s) = \frac{A_{V0} \,.\, (R_E^B / R_E)(1 + sC_E R_E)}{1 + sR_E^B C_E}$$

$$= \frac{A_{V0}(R_E^B / R_E)(1 + s/\omega_E)}{1 + sR_E^B C_E} \tag{10.107}$$

$$\omega_E = \frac{1}{R_E C_E} \quad \text{Effect of imperfect } C_E,\ C_B \to \infty \tag{10.108}$$

$$R_E^B = \frac{(R_s + r_\pi) \,.\, R_E}{R_s + R_\pi + (\beta_0 + 1)R_E} = \frac{(R_s + r_\pi)/(\beta_0 + 1) \,.\, R_E}{(R_s + r_\pi)/(\beta_0 + 1) + R_E} \tag{10.109a}$$

$$= \frac{R_s + r_\pi}{\beta_0 + 1} \| R_E \tag{10.109b}$$

$$A_{V0} = \frac{-\beta_0 R_C}{(R_s + r_\pi)}, \quad \text{the midband gain with perfect } C_B \text{ and } C_E \tag{10.110}$$

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$$\therefore \qquad Z_B = \frac{1 + sC_B R_s}{sC_B}, \text{ and } Z_E = \frac{R_E}{1 + sC_E R_E}$$

As $$A_V(s) = \frac{V_0}{V_s} = \frac{-\beta_0 R_C}{Z_B + r_\pi + (1 + \beta_0) Z_E}$$

(A "CE with Z_E" on the emitter side)

$$= \frac{-\beta_0 R_C}{\frac{1 + sC_B R_s}{sC_B} + r_\pi + (1 + \beta_0)\frac{R_E}{1 + sC_E R_E}}$$

$$= \frac{-\beta_0 R_C \, sC_B (1 + sC_E R_E)}{(1 + sC_B R_s)(1 + sC_E R_E) + sC_B r_\pi (1 + sC_E R_E) + sC_B (1 + \beta_0) R_E}$$

$$= \frac{(-\beta_0 R_C /(R_s + r_\pi)) \cdot sC_B (R_s + r_\pi)(1 + sC_E R_E)}{1 + s[C_E R_E + C_B R_s + C_B r_\pi + C_B (1 + \beta_0) R_E] + s^2 [R_E C_E R_s C_B + R_E C_E r_\pi C_B]}$$

$$= \frac{A_{V0} \cdot \frac{s}{1/C_B (R_s + r_\pi)} \cdot \left(1 + \frac{s}{1/C_E R_E}\right)}{1 + s[R_E C_E + (R_s + r_\pi + (1 + \beta_0) R_E) C_B] + s^2 [R_E C_E (R_s + r_\pi) C_B]}$$

i.e., $$A_V(s) = \frac{A_{V0}(s/\omega_\beta)(1 + s/Z_1)}{1 + a_1 s + a_2 s^2}$$

which is Eq. (10.112a), hence proved.

Here $$A_{V0} = \frac{-\beta_0 R_C}{(R_s + r_\pi)}$$

$$\omega_\beta = \frac{1}{C_B (R_s + r_\pi)}$$

$$Z_1 = \frac{1}{C_E R_E}$$

$$a_1 = R_E C_E + (R_s + r_\pi + (1 + \beta_0) R_E) C_B$$

$$a_2 = R_E C_E \,.\, (R_s + r_\pi) C_B$$

Note that $$R_E^0 = R_E, \; R_B^0 = R_s + r_\pi + (1 + \beta_0) R_E$$

R_B^E = Impedance seen by C_B with C_E shorted = $R_s + r_\pi$

$$\therefore \qquad \left.\begin{aligned} a_1 &= R_E^0 C_E + R_B^0 C_B \\ a_2 &= (R_E^0 C_E)(R_B^E C_B) \end{aligned}\right\} \text{ as expected from Eq. (10.112a)}$$

Note 1: If $C_E \to \infty$ and C_B imperfect coupling case, we get

$$A_V(s)\big|_{C_E \to \infty} = \frac{A_{V0} S/C_B (R_s + r_\pi)(1 + sC_E R_E)}{1 + s[R_E C_E + (R_s + r_\pi + (1 + \beta_0) R_E) C_B] + s^2 [R_E C_E (R_s + r_\pi) C_B}\Bigg|_{C_E \to \infty}$$

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$$\therefore \quad f_E = \frac{1}{2\pi R_E C_E} = \frac{1}{2\pi \times 1.5 \times 10^3 \times 408 \times 10^{-6}} = 0.260 \text{ Hz} \quad \textit{Ans.}$$

This implies that at $|s| = |j\omega| = \dfrac{1}{C_E R_E}$, the gain is –3 dB for imperfect C_E bypass.

Note:

1. In Example 10.15, the value of C_E required is much larger than the value of C_B.
2. Zero introduced by C_E occurs at such a low frequency compared to the desired value of f_L that it has negligible effect on the low-frequency response.
3. Both size and the cost of discrete capacitances increase with increasing capacitance value. Thus, it is customary to select C_E to meet the desired value of f_L. Then C_B is selected to make f_{LB} occur at a much lower frequency than f_L.

	Choose	$f_{LE} = f_L$
As a thumb rule,	Choose	$f_{LB} \le \dfrac{1}{10} f_L$

(10.115)

In the part (a) of this Example 10.15, if we choose $f_{LE} = f_L = 50$ Hz, we shall obtain

$$C_E = \frac{408}{2} = 204 \ \mu\text{F}$$

For $f_{LB} = \dfrac{1}{10} f_L = 5$ Hz, we require

$$C_B = \frac{1 \times 10^{-3}}{2\pi \times 5 \times (1 + 0.6)} = 19.9 \ \mu\text{F}$$

Thus, the total capacitance now required = 204 + 19.9 = 224 μF, as compared to the earlier value of 408 + 3.98 = 412 μF, i.e., nearly one-half. Thus, we save both cost and size.

ADDITIONAL SOLVED EXAMPLES

EXAMPLE 10.16

A common-emitter stage uses the transistor whose parameters are given in Fig. 10.69. For R_C = 1.5 kΩ and R_s = 0.6 kΩ, determine A_{V0} and f_H.

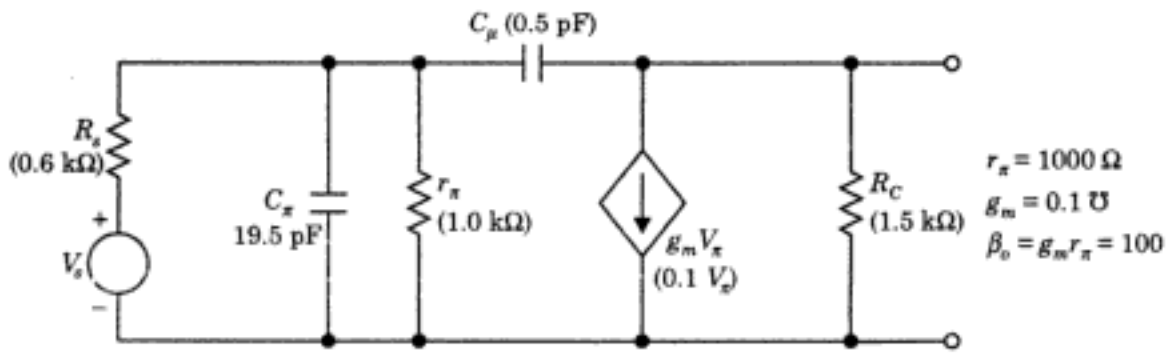


Fig. 10.69 The given circuit, Ex. 10.16.

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Solution: As we know,

$$A_{V0} = \frac{-\beta_0 R_C}{R_s + r_\pi}$$

$$= \frac{-100 \times 1.5}{0.6 + 1} = -93.75$$

Given data is: $r_\pi = 1000\ \Omega,\ g_m = 0.1\ \Omega$

$\therefore$ $\beta_0 = g_m r_\pi = 100$

$$R_\pi^0 = R_s \| r_\pi = 0.6 \| 1 = 0.375\ \text{k}\Omega$$

$$R_\mu^0 = R_\pi^0 + (1 + g_m R_\pi^0) R_C$$

$$= 0.375 + (1 + 0.1 \times 375) \times 1.5 = 0.375 + 57.75 = 58.125\ \text{k}\Omega$$

$$a_1 = R_\pi^0 C_\pi + R_\mu^0 C_\mu$$

$$= (0.375 \times 19.5 + 58.125 \times 0.5)10^{-9} = 36.375 \times 10^{-9}\ \text{sec}$$

$$a_2 = R_\pi^0 C_\pi . R_\mu^\pi C_\mu = R_\pi^0 C_\pi . R_C C_\mu$$

$$= (0.375 \times 19.5)(1.5 \times 0.5) \times 10^{-18} = 5.484 \times 10^{-18}\ \text{sec}^2$$

$$A_V(s) = \frac{A_{V0}(1 - s/\omega_Z)}{1 + a_1 s + a_2 s^2} \approx \frac{A_{V0}}{1 + a_1 s}$$

This is valid approximation as $\frac{p_2}{p_1} = \frac{a_1/a_2}{1/a_1} = \frac{a_1^2}{a_2} = 241.3 >> 8$

$\therefore$ $\omega_H = \frac{1}{a_1} = \frac{10^9}{36.375}$

$$f_H = \frac{1}{2\pi}\omega_H = \frac{1000}{2\pi \times 36.375} \times 10^6 = 4.375\ \text{MHz}$$ **Ans.**

EXAMPLE 10.17

(a) Derive the voltage gain $\frac{V_0}{V_S}$ at high frequency for a *CE* stage, as shown in Fig. 10.70.

(b) Given the source resistance R_S = 0.3 kΩ, r_π = 2 kΩ, R_C = 0.6 kΩ, g_m = 0.1 mΩ, C_π = 19.5 pF and C_μ = 0.5 pF, find the values of a_1 and a_2 by time constant method.

Solution: (a) Without C_π and C_μ, the voltage gain is:

$$A_{V0} = \frac{-\beta_0 R_L}{R_S + r_\pi}$$

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$$p_2 = \frac{a_1}{a_2} = \frac{5.5078 \times 10^{-9}}{1.521 \times 10^{-18}} = 3621.1 \times 10^6 \text{ rad/s} = 576.32 \text{ MHz},$$

$$\frac{p_2}{p_1} = 19.94 > 8 \quad \therefore \quad \text{valid amplifier analysis by time constant method.}$$

EXAMPLE 10.18

For the two-stage amplifier shown in Fig. 10.71 evaluate the upper 3 dB frequency f_H using the time constant method and assuming the dominant-pole approximation. Compare the bandwidth, the gain-bandwidth product of the cascade with those of the individual stages.

Given $r_{x1} = 1.4$ kΩ, $r_{x2} = 2.8$ kΩ, $g_{m1} = 0.15$ ℧,

$g_{m2} = 0.05$ ℧, $C_{x1} = 20$ pF, $C_{x2} = 25$ pF, $C_{\mu 1} = C_{\mu 2} = 0.5$ pF

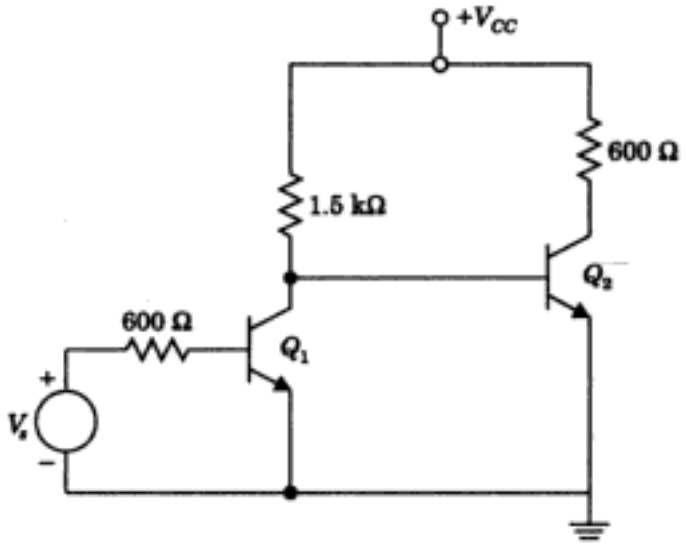


Fig. 10.71 The given circuit, Ex. 10.18.

Solution:

$$\beta_{01} = g_{m1} r_{x1} = 0.15 \times 1.4 \times 10^3 = 210$$

$$\beta_{02} = g_{m2} r_{x2} = 0.05 \times 2.8 \times 10^3 = 140$$

The ac model is drawn in Fig. 10.72.

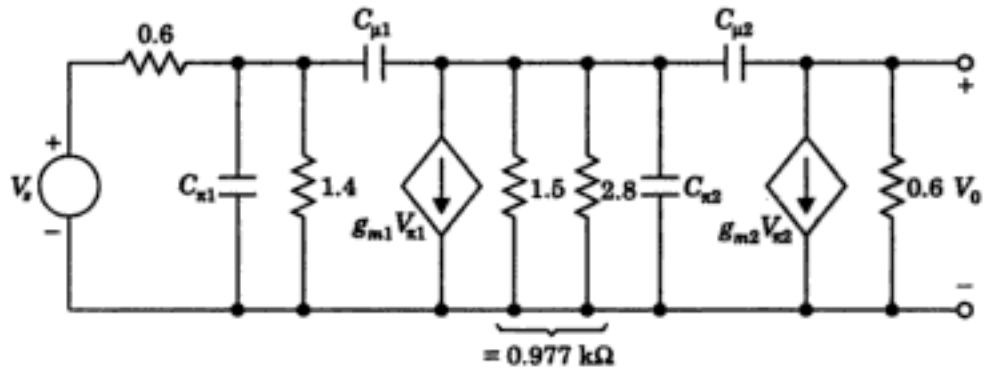


Fig. 10.72 The equivalent diagram of the given circuit. (Values of resistances are in kΩ)

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EXAMPLE 10.19

In the circuit shown in Fig. 10.73, Q_1 and Q_2 have $\beta_F = 150$, $V_A = 120$ V, $f_T = 400$ MHz and $C_\mu = 0.5$ pF at a bias current $I_{CQ} = 100$ μA. For $R_S = 50$ kΩ and $R_C = 250$ kΩ, determine the approximate value of f_H.

Solution

$$g_m = \frac{I_{CQ}}{V_T} = \frac{100 \times 10^{-6}}{25 \times 10^{-3}} = 4 \text{ m℧}$$

$$r_\pi = \frac{\beta_F}{g_m} = \frac{150}{4 \times 10^{-3}} = 37.5 \text{ kΩ}$$

$$r_0 = \frac{V_A}{I_{CQ}} = \frac{120}{100 \times 10^{-6}} = 1.2 \text{ MΩ} = 1200 \text{ kΩ}$$

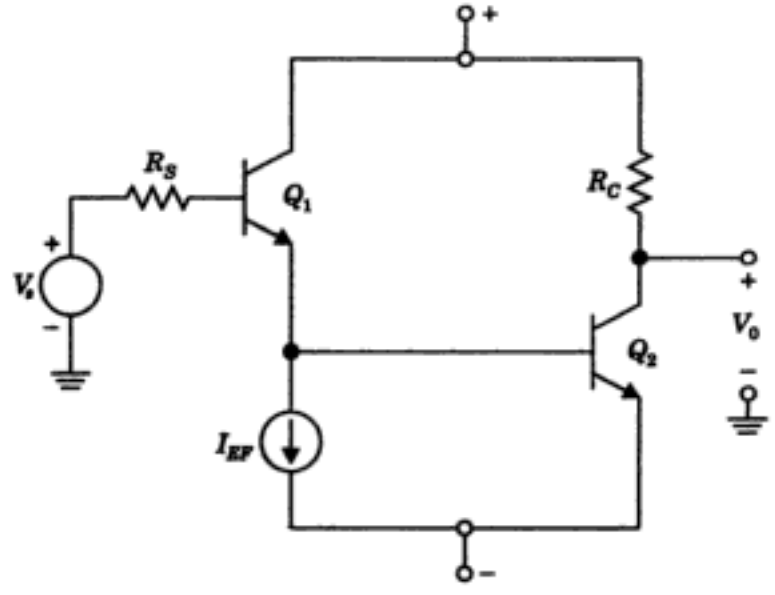


Fig. 10.73 The given circuit, Ex. 10.19.

As $$2\pi f_T = \frac{\beta_0}{r_\pi (C_\pi + C_\mu)}$$

$\therefore$ $$C_\pi = \frac{150 \times 10^{-8}}{4 \times 2\pi (37.5 \times 10^3)} - 0.5 \times 10^{-12} \quad (\because f_T = 400 \times 10^6,\ r_\pi = 37.5 \text{ kΩ})$$

$$= (1.59 - 0.5) \times 10^{-12} = 1.09 \text{ pF}$$

The AC model is shown in Fig. 10.74 and $R^0_{\mu 1} = R_s \,||\, R_i$ at XX' of emitter follower.

As $$R_i = r_{\pi 1} + (1 + 150)(r_{01} \,||\, r_{\pi 2})$$

$$= 37.5 + 151 \times \frac{1200 \times 37.5}{1200 + 37.5}$$

$$= 37.5 + 5490.5 = 5528 \text{ kΩ}$$

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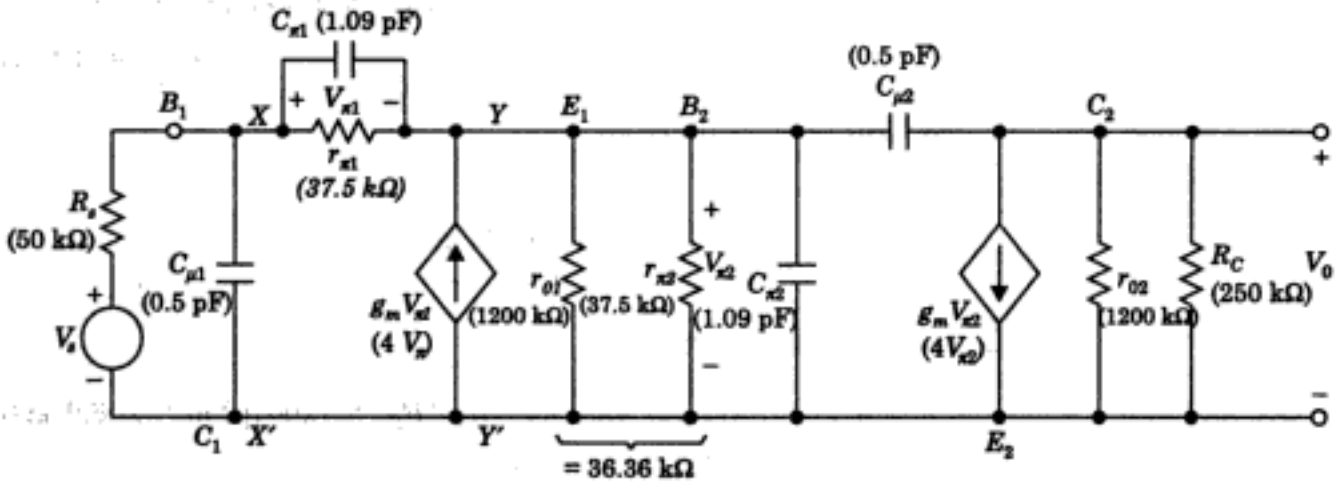
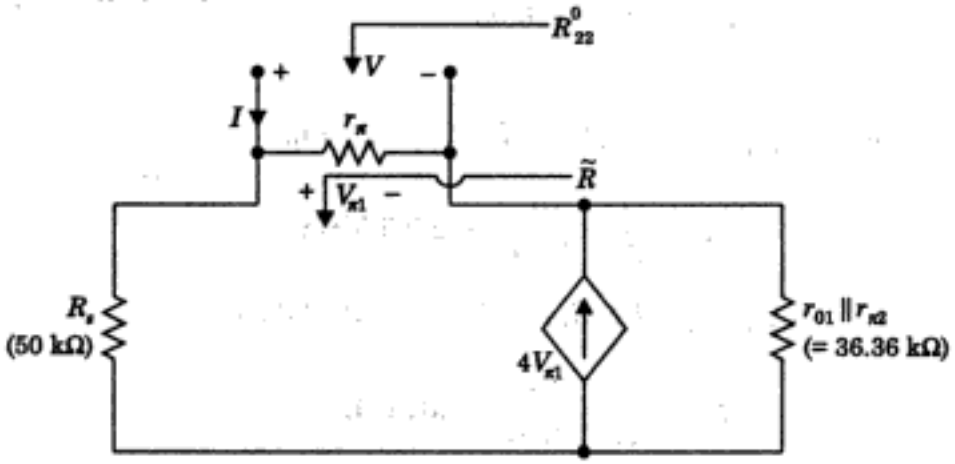


Fig. 10.74 The equivalent AC model of the circuit.

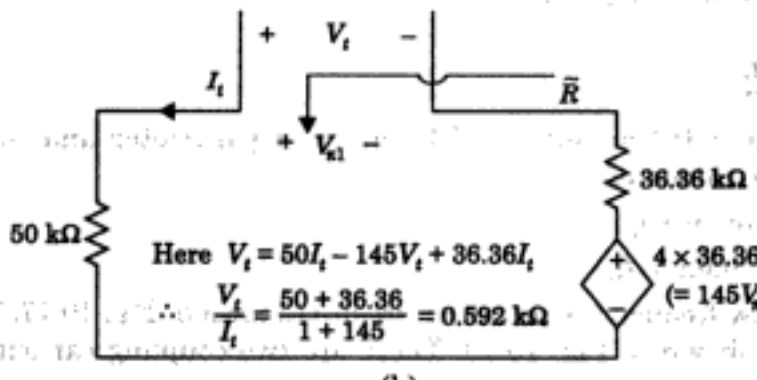
$\therefore \quad R^0_{\mu 1} = 50 \,||\, 5528 = 49.55 \text{ k}\Omega$

In Fig. 10.75a $\quad R^0_{22} = r_\pi \,||\, \tilde{R} \qquad (\because R^0_{22} = R^1_{\pi 1})$

$= 37.5 \text{ k}\Omega \,||\, 0.592 \text{ k}\Omega = 0.5828 \text{ k}\Omega \qquad (\tilde{R} \text{ is found in Fig. 10.75b})$



(a)


$+ V_t -$
I_t
$\tilde{R}$
$+ V_{\pi 1} -$
36.36 kΩ
50 kΩ
Here $V_t = 50I_t - 145V_t + 36.36I_t$
$\therefore \frac{V_t}{I_t} = \frac{50 + 36.36}{1 + 145} = 0.592 \text{ k}\Omega$
$4 \times 36.36V_{\pi 1}$ (= $145V_{\pi 1}$)

(b)

Fig. 10.75 To find R^0_{22}. First find $\tilde{R}$ then $R^0_{22} = r_\pi \,||\, \tilde{R}$. $\tilde{R}$ infound Fig. (b)

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R_{22}^{∞} = Resistance seen by C_2 with C_1, C_3 short circuited

$\therefore$ $V_{gs1} = V_{gs2} = 0$ for $V_s = 0$

and $R_{22}^{\infty} = R_{D2} + R_L = 5 + 10 = 15\ \text{k}\Omega$

$$\tau_2 = C_2 R_{22}^{\infty} = 10 \times 10^{-6} \times 15 \times 10^3 = 150\ \text{ms}$$

R_{33}^{∞} = Resistance seen by C_3 with C_1, C_2 short circuited

$$= R_{S2} \| \frac{1}{g_{m2}} = 0.15\ \text{k}\Omega \| \frac{1}{10}\ \text{k}\Omega$$

$$= \frac{0.15 \times 0.1}{0.15 + 0.1} = \frac{0.015}{0.25} = 0.06\ \text{k}\Omega$$

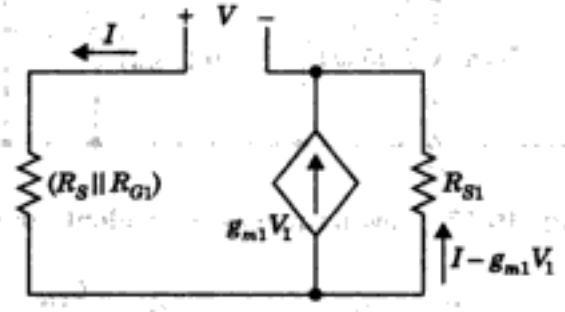
$$\tau_3 = C_3 R_{33}^{\infty} = 5.3 \times 10^{-6} \times 0.06 \times 10^3 = 0.32\ \text{ms}$$

$$f_L = \frac{1}{2\pi} \sum_{i=1}^{3} \frac{1}{C_i R_{ii}^{\infty}} = \frac{1}{2\pi} \left(\frac{10^3}{50.2} + \frac{10^3}{150} + \frac{10^3}{0.32} \right) = \frac{10^3 \times 0.315066}{2\pi} = 501\ \text{Hz}$$ **Ans.**

[*To find R_{gs1} — see Fig. 10.79*]

(b) $$R_{gd1} = R_S \| R_{G1} = 0.2\ \text{k}\Omega \| 50\ \text{k}\Omega = \frac{0.2 \times 50}{0.2 + 50} = 0.1992\ \text{k}\Omega$$

As $$R_{gs1} = \frac{(R_S \| R_{G1}) + R_{S1}}{1 + g_{m1} R_{S1}} = \frac{(0.1992) + 0.25}{1 + 10 \times 0.25} = 0.1283\ \text{k}\Omega$$



$$V = I(R_S \| R_{G1}) + R_{S1}(I - g_{m1} V) \quad \therefore \quad \frac{V}{I} = \frac{(R_S \| R_{G1}) + R_{S1}}{1 + g_{m1} R_{S1}}.$$

Fig. 10.79 To find R_{gs1}

and $$R_{gs2} = R_{S1} \| \frac{1}{g_m}$$

$$= (0.25\ \text{k}\Omega) \| \left(\frac{1}{10}\ \text{k}\Omega \right) = (250\ \Omega) \| (100\ \Omega) = 71.4\ \Omega = 0.0714\ \text{k}\Omega$$

$$R_{gd2} = R_{gs2} + (R_{D2} \| R_L) + R_{gs2}(R_{D2} \| R_L) \cdot g_{m2}$$

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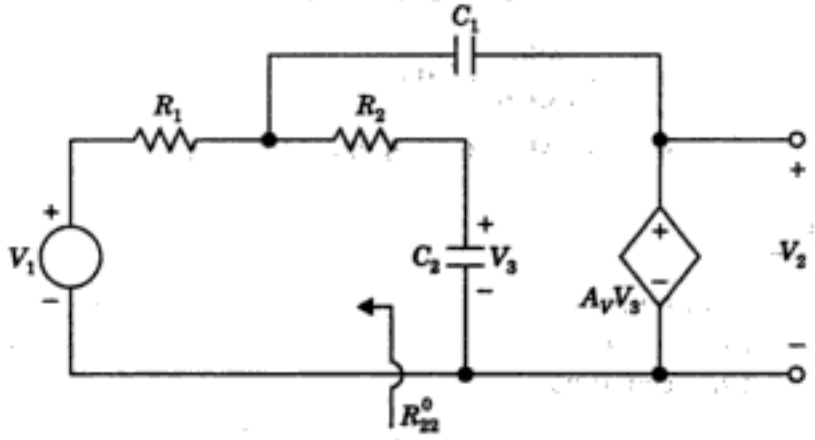


Fig. 10.82 The equivalent diagram of Fig. 10.81.

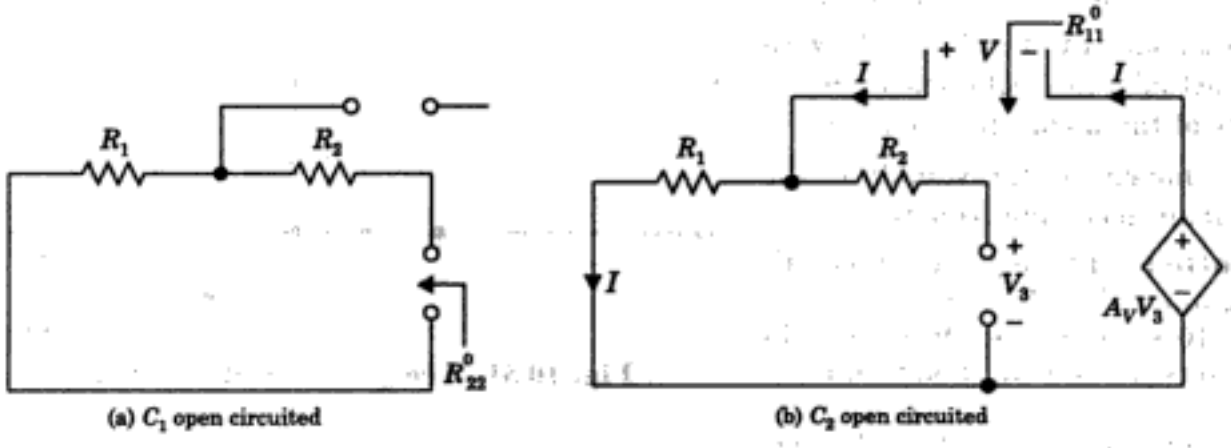


Fig. 10.83 Circuits to find (a) R_{22}^0 and (b) R_{11}^0.

Clearly $R_{11}^2 = R_1 \| R_2$

$\therefore$ $a_2 = (R_{11}^2 C_1)(R_{22}^0 C_2)$

$$= \left(\frac{R_1 R_2}{R_1 + R_2} C_1\right)((R_1 + R_2)C_2)$$

$\therefore$ $a_2 = R_1 R_2 C_1 C_2$ **Ans.**

(b) For $R_1 = R_2 = R_1$, $C_1 = C_2 = C$, $A_V = 2$

$a_1 = CR(1 - 2) + C(R + R) = CR$

$a_2 = C^2R^2$

For dominant pole,

$$|p_1| = \frac{1}{a_1} = \frac{1}{RC}$$ **Ans.**

and $$|p_2| = \frac{a_1}{a_2} = \frac{CR}{C^2R^2} = \frac{1}{RC}$$ **Ans.**

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and C_μ = 1 pF. Assume that the frequency response of the emitter follower (Q_1 stage) is sufficiently high so that it has negligible effect on the value of f_H of the cascade.

Compute the value of f_H for the cascade by time constant method verify that the dominant-pole assumption is valid.

Solution: β_0 = 100 for all transistors

$r_{\pi 1} = r_{\pi 2}$ = 0.5 kΩ

$r_{\pi 3}$ = 1.0 kΩ

We first replace Stage 1(Q_1) by an equivalent voltage source and output impedance since Stage 1 is assumed having negligible effect on f_H. See Fig. 10.86.

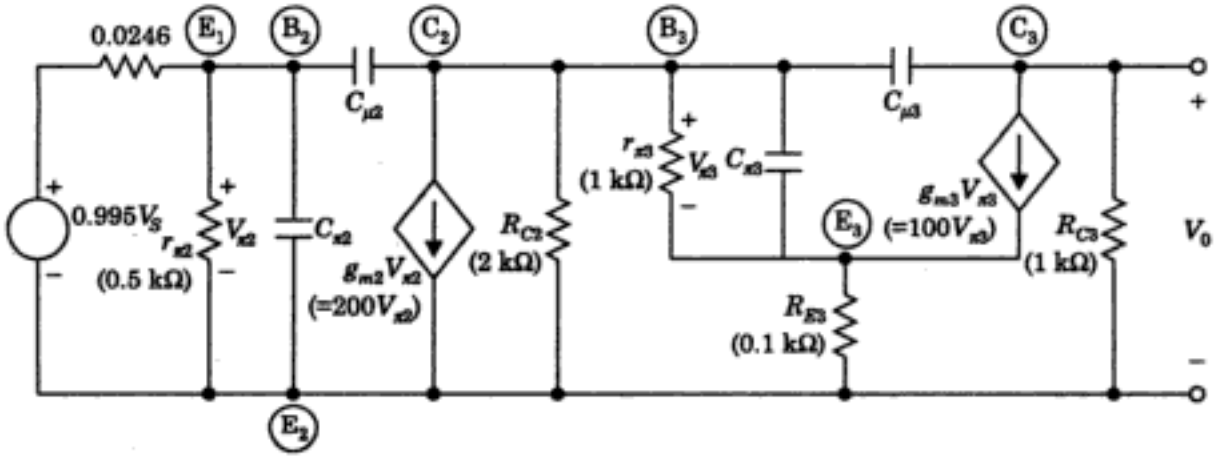


Fig. 10.86 Replacing Q_1 stage by $0.995V_S$ and R'_{01} = 0.0246 kΩ AC model of stages Q_2 and Q_3.

Stage 1

$$\text{Gain } A_{V1} = \frac{(1+\beta_0)R_{E1}}{R_S + r_{\pi 1} + (1+\beta_0)R_{E1}}$$

$$= \frac{(1+100)5}{2+0.5+(1+100)\times 5} = 0.995$$

$$R'_{01} = R_{E1} \| \frac{R_S + r_{\pi 1}}{1+\beta_0} = 5 \| \frac{2+0.5}{1+100} = 5 \| \frac{2.5}{101} = 0.0246 \text{ k}\Omega$$

$$g_{m2} = \frac{\beta_{02}}{r_{\pi 2}} = \frac{100}{0.5} = 200 \text{ m}\mho$$

$$g_{m3} = \frac{\beta_{03}}{r_{\pi 3}} = \frac{100}{1.0} = 100 \text{ m}\mho$$

$$C_{\pi 2} + C_{\mu 2} = \frac{\beta_{02}}{r_{\pi 2} \cdot \omega_{T2}} = \frac{100}{0.5\times 10^3 (2\pi \times 200 \times 10^6)} = \frac{10^{-12}\times 10^3}{0.5(2\pi \times 2)} = 159 \text{ pF}$$

$\therefore$ $C_{\pi 2} = 159 - C_{\mu 2} = 159 - 1 = 158$ pF

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At low frequencies, we have

$$A_{V01} = 0.995 \text{ already found, } R'_{01} = 0.0246 \text{ k}\Omega$$

$$A_{V02} = \frac{-\beta_{02} . R_{C2}}{R'_{01} + r_{\pi 2}} = \frac{-100 \times 2.0}{0.0246 + 0.5} = -381$$

$$R'_{02} = R_{C2} || r_{02} = R_{C2} = 2.0 \text{ k}\Omega$$

$$A_{V03} = \frac{-\beta_{03} R_{C3}}{R'_{02} + r_{\pi 3} + (1 + \beta_{03}) R_{E3}} = \frac{-100 \times 1}{2.0 + 1.0 + (1 + 100)0.1} = -7.63$$

$$R'_{03} = R_{C3} \quad (\because \text{ here } r_{03} = \infty) = 1 \text{ k}\Omega$$

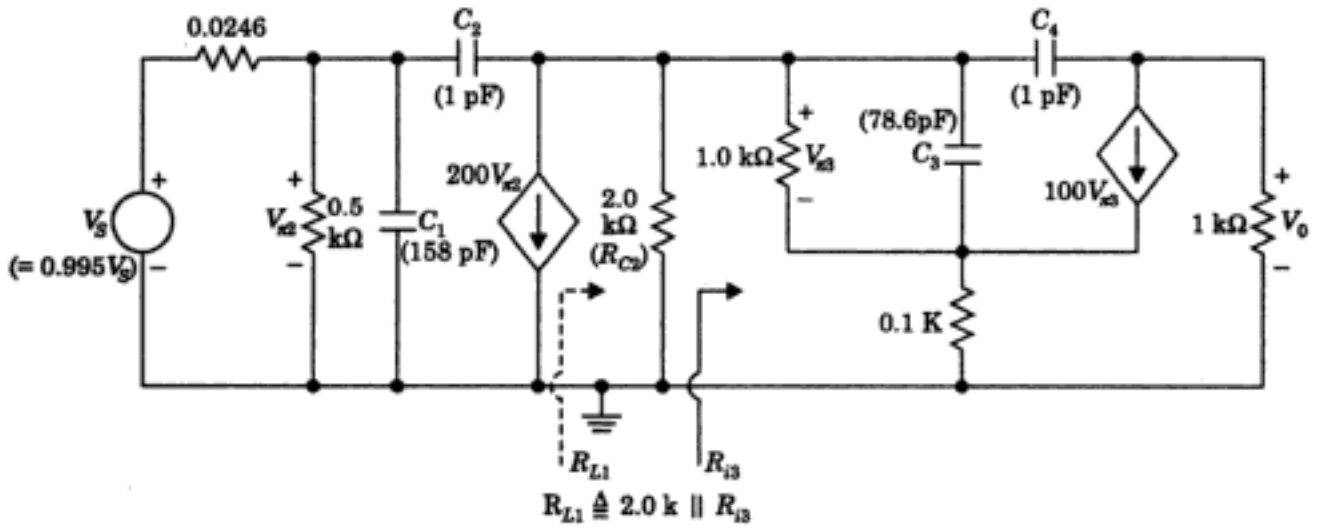


Fig. 10.87 Fig. 10.86 redrawn by renumbering C_π and $C_{\mu i}$, i = 2, 3.

Overall DC gain $A_{V0} = A_{V01} . A_{V02} . A_{V03}$

$$= (0.995)(-381)(-7.63) = 2892$$

Renumbering $C_{\pi 2}$ as C_1, $C_{\mu 2}$ as C_2, $C_{\pi 3}$ as C_3 and $C_{\mu 3}$ as C_4, we have the circuit, as given in Fig. 10.87

Here $R^0_{11} = 0.0246 || 0.5 = 0.0234$ $(\therefore R^0_{11} = 0.0234 \text{ k}\Omega)$

$R_{L1} = 2 \text{ k}\Omega || R_{i3} = 2 \text{ k}\Omega || [r_{\pi 3} + (1 + \beta_{03}) R_{E3}] = 2 || (11.1) = 1.69 \text{ k}\Omega$ $(\therefore R_{L1} = 1.69 \text{ k}\Omega)$

$R^0_{22} = R^0_{11} + R_{L1}(1 + g_m R^0_{11})$

$= 0.0234 + 1.69(1 + 200 \times 10^{-3} \times 0.0234 \times 10^3) = 9.623$ $(\therefore R^0_{22} = 9.623 \text{ k}\Omega)$

[*To determine* R^0_{33}] (see Fig. 10.88)

$$R^0_{33} = 1.0 \text{ k}\Omega || R'$$

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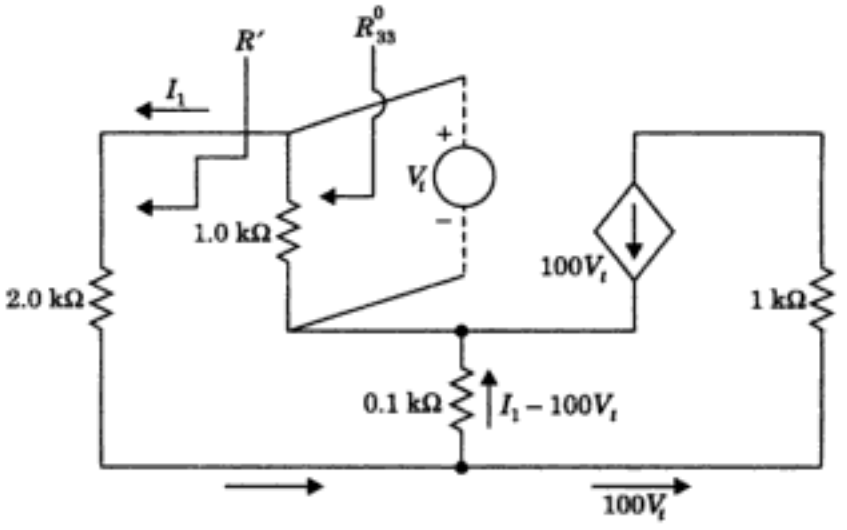


Fig. 10.88 To calculate R_{33}^0. V_t is the test voltage.

[*To determine first R′*] In order to find R_{33}^0, we first need R' as shown in Fig. 10.88.

$$V_t = I_1 \times 2 + 0.1(I_1 - 100V_t) \qquad (V_t \text{ is the test voltage applied})$$

$$\therefore \quad \frac{V_t}{I_1} = R' = \frac{2.1}{1+10} = 0.1909 \text{ k}\Omega$$

and $$R_{33}^0 = (1.0 \text{ k}\Omega) \| (0.1909 \text{ k}\Omega) = \frac{1 \times 0.1909}{1 + 0.1909} = 0.160 \text{ k}\Omega$$

$$(\therefore \; R_{33}^0 = 0.160 \text{ k}\Omega)$$

[*To find* R_{44}^0] (see Fig. 10.89)

$$V_t = (I_t - I_1) \times 2 + (I_1 + 100I_1) \times 1$$

or $$V_t = 3I_t + 98I_1 \qquad \text{(i)}$$

Also, $$2 \times (I_t - I_1) = 1 \times I_1 + 101 \times 0.1I_1$$

$$\therefore \quad I_1 = (2/13.1)I_t \qquad \text{(ii)}$$

From Eqs. (i) and (ii),

$$V_t = 3I_t + 98 \times \frac{2}{13.1} I_t$$

$$\therefore \quad \frac{V_t}{I_t} = R_{44}^0 = 3 + \frac{2 \times 98}{13.1} = 17.962 \text{ k}\Omega \qquad (\therefore \; R_{44}^0 = 17.962 \text{ k}\Omega)$$

$$a_1 = R_{11}^0 C_1 + R_{22}^0 C_2 + R_{33}^0 C_3 + R_{44}^0 C_4$$

$$= (0.0234 \times 158) + (9.623 \times 1) + (0.160 \times 78.6) + (17.962 \times 1) = 43.8582 \text{ ns}$$

$$\therefore \quad f_H = \frac{1}{2\pi \times a_1} = \frac{10^9}{2\pi \times 43.8582} = 3.628 \times 10^6 = 3.628 \text{ MHz}$$

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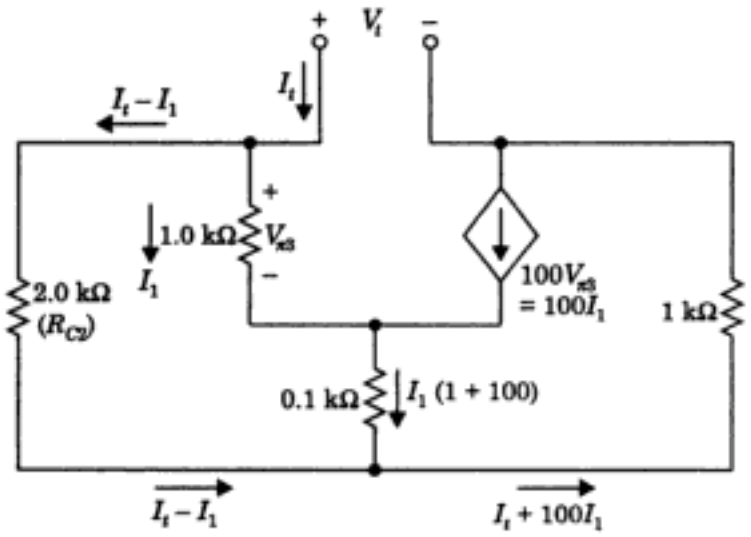


Fig. 10.89 To determine R_{44}^0. Apply a test voltage V_t.

[To find a_2]

$$R_{22}^1 = 2.0\ \text{k}\Omega \,||\, R_{i3} = R_{L1} = 1.69\ \text{k}\Omega \qquad (\therefore\ R_{22}^1 = 1.69\ \text{k}\Omega)$$

$$R_{33}^1 = R_{33}^0 = 0.160\ \text{k}\Omega \qquad (\therefore\ R_{33}^1 = 0.160\ \text{k}\Omega)$$

$$R_{44}^1 = R_{44}^0 = 17.962\ \text{k}\Omega \qquad (\therefore\ R_{44}^1 = 17.962\ \text{k}\Omega)$$

$$R_{22}^3 = R_{11}^0 + \tilde{R}_{L1}(1 + g_m R_{11}^0)$$

where $$\tilde{R}_{L1} = 2.0\ \text{k}\Omega \,||\, R_{i3}\big|_{C_3 \text{ shorted}}$$

$$= 2.0\ \text{k}\Omega \,||\, 0.1\ \text{k}\Omega = 0.09524\ \text{k}\Omega$$

$\therefore$ $$R_{22}^3 = 0.0234 + 0.09524(1 + 200 \times 0.0234)$$

$$= 0.564\ \text{k}\Omega \qquad (\therefore\ R_{22}^3 = 0.564\ \text{k}\Omega)$$

$$R_{44}^1 = R_{44}^0 = 17.962\ \text{k}\Omega \qquad (\therefore\ R_{44}^1 = 17.962\ \text{k}\Omega)$$

$$R_{44}^3 = 2.0\ \text{k}\Omega \,||\, 0.1\ \text{k}\Omega + 1.0\ \text{k}\Omega = 0.09524 + 1.0 = 1.09524\ \text{k}\Omega$$

$$(\therefore\ R_{44}^3 = 1.09524\ \text{k}\Omega)$$

[*To find* R_{44}^2]

We draw circuit similar to Fig. 10.79 but with R_{C2} replaced by

$$2.0\ \text{k}\Omega \,||\, \frac{1}{g_{m2}} \,||\, R_{11}^0 = 2.0 \,||\, \frac{1}{200} \,||\, 0.0234 = 0.0041\ \text{k}\Omega$$

Now, we get

$$a_2 = R_{11}^0 C_1 (R_{22}^1 C_2 + R_{33}^1 C_3 + R_{44}^1 C_4) + R_{22}^0 C_2 (R_{33}^2 C_3 + R_{44}^2 C_4) + R_{33}^0 C_3 R_{44}^3 C_4$$

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or $$a_2 = 0.0234 \times 158(1.69 \times 1 + 0.160 \times 78.6 + 17.962 \times 1) + (0.564 \times 1 \times 0.160 \times 78.6 + 9.623 \times 1 \times 1.04 \times 1) + 0.160 \times 79.6 \times 1.09524 \times 1$$

$$= 119.15 + 17.10 + 13.95 = 150.2$$

$$p_2 = (a_2/a_1)^{-1} = (150.2/43.8582)^{-1} = 0.29199 \times 10^6 \text{ rad/sec}$$

$\therefore$ $$f_2 = p_2/2\pi = 46.47 \text{ MHz.}$$

Clearly $f_2 > 8f_1$ $\therefore$ our assumption is of dominant pole valid.

SUMMARY

- To analyse the performance of amplifiers over wide frequency range, we must include the effect of external capacitances (C_C and C_E, etc.) and the device capacitance (C_π, C_μ for BJT and C_{gs}, C_{gd} and C_{ds} for FET).
- Bode diagram (also called asymptotic Bode diagram) are very useful to assess the frequency response.
- Gain in decibels (dB) is used in Bode diagrams.
- For lowpass circuit of a BJT, the frequency response is 3 dB down at frequency:

$$f_H = \frac{1}{2\pi(R_S \parallel R_i) \cdot C_M}$$

- For a highpass circuit of a BJT, the frequency response is highest at $\omega = \infty$ and is 3 dB down at frequency

$$f_L = \frac{1}{2\pi(R_S + R_i)C_C}$$

- 3 dB bandwidth is the range of frequency in which the amplitude response is not below half power of its value at maximum amplitude response.
- Step response gives an assessment of fidelity of the amplifier to various types of input signals.
- Rise time and tilt (sag) are useful parameters determined by the step response and square-wave response.
- Common emitter short circuit gain in given by

$$\beta(s) = \frac{\beta_0(1 - s/\omega_z)}{1 + s/\omega_\beta}$$

where $$\omega_z = \frac{g_m}{C_\mu} \quad \text{and} \quad \omega_\beta = \frac{1}{r_\pi(C_\pi + C_\mu)}$$

- At the terminal frequency f_T the gain is unity and $\omega_T = 2\pi f_T = \beta_0\omega_\beta \approx g_m/(C_\pi + C_\mu)$.
- For any single-pole system with high gain,

Unity frequency f_T = Midband gain β_0 × 3 dB Bandwidth f_β

- In generalised Transfer Function of a system, the number of poles is equal to the number of zeros.

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10.5 What is meant by open circuit constant a_1? It is well known that a_1 = sum of time constants $C_i R_{ii}^0$, where R_{ii}^0 is called zero frequency resistant. Why is it so called?

10.6 Explain the method how do we compute R_{11}^0 and R_{22}^1. Is $(R_{11}^0 C_1)(R_{22}^1 C_2)$ equal to $(R_{11}^2 C_1)(R_{22}^0 C_2)$?

10.7 If a CC stage is cascaded with a CE stage, which stage decides the overall 3-dB bandwidth of the cascaded amplifier?

10.8 In what way, the imperfect coupling and bypass capacitors affect low frequency response of an amplifier?

NUMERICAL PROBLEMS

P10.1 (a) An amplifier has a voltage gain given by

$$A_V(s) = \frac{Ks}{(s+100)(s+10^5)} = \frac{V_0}{V_i}$$

In the asymptotic Bode plot of $A_V(j\omega)$, over what values of frequency (the midband frequency) is the gain constant in amplitude?

(b) If $K = 10^8$, determine the midband frequency gain in decibels.

(***Ans.*** (a) $100 < \omega \leq 10^5$ rad/sec (b) 20 dB)

P10.2 (a) Draw the asymptotic Bode diagram for

$$A_V(s) = \frac{10^4(s+40)}{s^2+410s+4000}$$

(b) Determine the value of $A_V(j800)$.

(**Ans.** (b) $A_V(j800)$ = 22 dB = 12.6; Arg$(j800)$ = –58.5°)

P10.3 (a) For the common emitter stage shown in the Figure 10.90, by using hybrid-π model, and r_0 not infinity, find the gain.

$$A_{VH}(s) = \frac{V_0}{V_S} = \frac{A_{V0}(1 - s/Z_1)}{1 + a_1 s + a_2 s^2}$$

What are the values of A_{V0}, Z_1, a_1 and a_2?

(b) Assume R_S = 0.3 kΩ, r_π = 2.0 kΩ, C_π = 19.5 pF and C_μ = 0.5 pF, find the values of Z_1, a_1, a_2 and f_h if $r_0 \to \infty$ and g_m = 0.05 ℧.

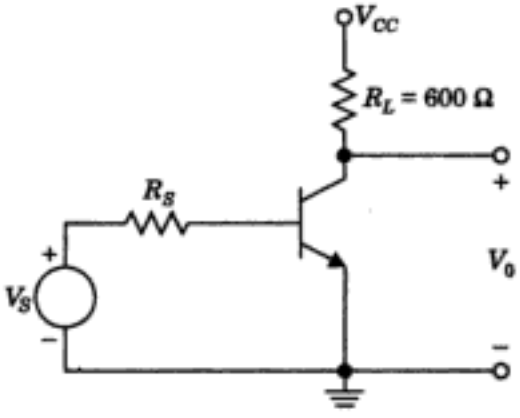


Fig. 10.80 The given CE circuit, P10.3.

(***Ans.*** (a) $A_{V0} = -\beta_0 \tilde{R}_L / (R_s + r_\pi)$ where $\tilde{R}_L = R_L \| r_0$;

$Z_1 = g_m / C_\mu$; $a_1 = R_\pi^0 C_\pi + (R_\pi^0 + (1 + g_m R_\pi^0)\tilde{R}_L) C_\mu$ where $R_\pi^0 = R_S \| r_\pi$;

$a_2 = R_\pi^0 \tilde{R}_L C_\pi C_\mu$, (b) $Z_1 = 10^{11}$ rad/s; $a_1 = 9.416 \times 10^{-9}$ sec; $a_2 = 1.521 \times 10^{-18}$ sec^2)

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P10.4 The following data are available for the amplifier shown in Fig. 10.91

$I_{CQ} = 5$ mA, $f_T = 750$ MHz, $\beta = 150$, $r_b = 200\ \Omega$, $C_\mu = 2$ pF

Find the upper 3-dB frequency of the circuit.

(***Ans.*** $a_1 = 3066.25 \times 10^{-9}$ sec, $f_1 = 1/2\pi a_1 = 51.9$ kHz)

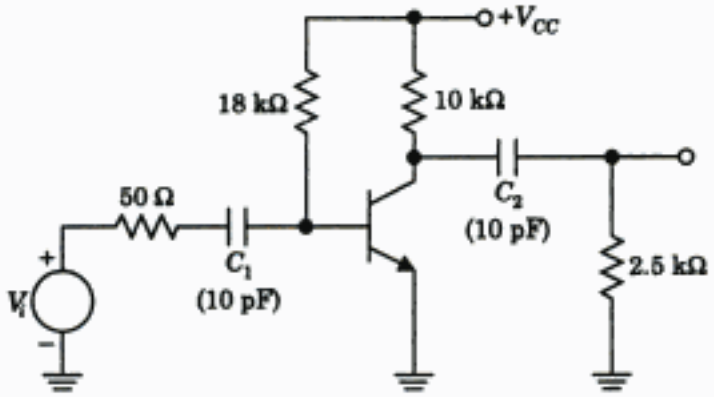


Fig. 10.91 The given circuit, P10.4.

P10.5 A pnp transistor is used in the circuit shown in Fig. 10.92 and biased at $I_{CQ} = -2.5$ mA. Determine the midband gain and upper half-power frequency.

(***Ans.*** Midband gain $A_V = -\beta_0 R_L/[R_S + r_\pi + (1 + \beta_0)R_E] = -20.93$, $a_1 = 17.464 \times 10^{-9}$ sec, $f_H = 1/2\pi a_1 = 9.11$ MHz)

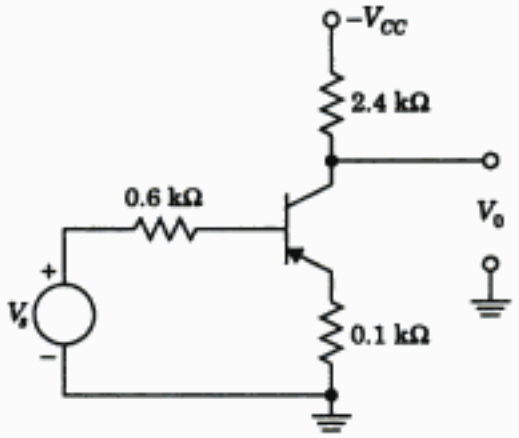


Fig. 10.92 Transistor has the parameters $\beta_0 = \beta_F = 150$, $V_A = \infty$ V, $f_T = 100$ MHz, $C_\mu = 0.5$ pF P10.5.

P10.6 A common emitter amplifier shown in Fig. 10.93 is fed from a high frequency source with $R_S = 450\ \Omega$. The amplifier delivers its output to a 800 Ω resistive load. The transistor parameters are $C_\pi = 21$ pF, $C_\mu = 0.75$ pF, $g_m = 0.05\ \Omega$, $\beta_0 = 150$.

(a) Draw the unilateral hybrid-π model for the amplifier.
(b) Determine a_1 and a_2 using the time-constant method.
(c) Evaluate the upper 3 dB frequency.
(d) Test the circuit for a dominant pole.

Assume $r_0 = \infty$.

(**Ans.** (b) $a_1 = R_\pi^0 C_\pi + R_\mu^0 C_\mu = 20.834 \times 10^{-9}$ sec

$$a_2 = (R_\pi^0 C_\pi)(R_\mu^\pi C_\mu) = 4.927 \times 10^{-18} \text{ sec}^2$$

(c) $p_1 = \dfrac{1}{a_1} = 47.9984 \times 10^6$ rad/s, $p_2 = \dfrac{a_1}{a_2} = 4.229 \times 10^9$ rad/s

(d) $p_2/p_1 = 88 > 8$, therefore, the analysis by dominant pole is valid.)

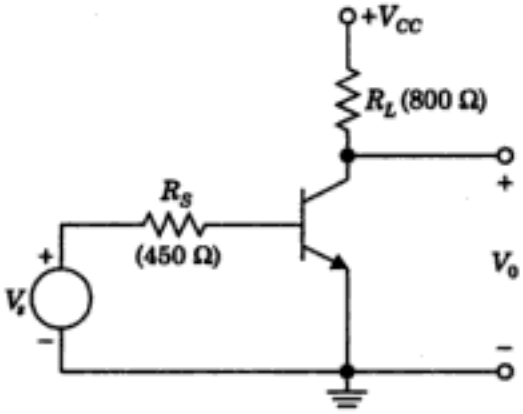


Fig. 10.93 The given CE amplifier P10.6.

P10.7 (a) Determine the a_1 coefficient in the TF of the amplifier stage whose equivalent circuit is displayed in Fig. 10.94.

(b) By using the numerical values indicated, approximate the upper 3 dB frequency f_H.

(**Ans.** (a) $a_1 = R_{gs}^0 C_{gs} + R_{gd}^0 C_{gd} + R_{ds}^0 C_{ds}$

where $R_{gs}^0 = \dfrac{(R_s + R_A)}{(1 + \bar{\mu})}$

$R_A = (r_d + R_D) \| R_S$

$\bar{\mu} = \dfrac{\mu R_A}{(r_d + R_D)}$

$R_{gd}^0 = R_s + \dfrac{R_D[r_d + \mu R_s + (1 + \mu)R_S]}{R_D + r_d + (1 + \mu)R_S}$

$R_{ds}^0 = \dfrac{r_d(R_S + R_D)}{R_D + r_d + (1 + \mu)R_S}$

(b) $f_H = 5.40$ MHz)

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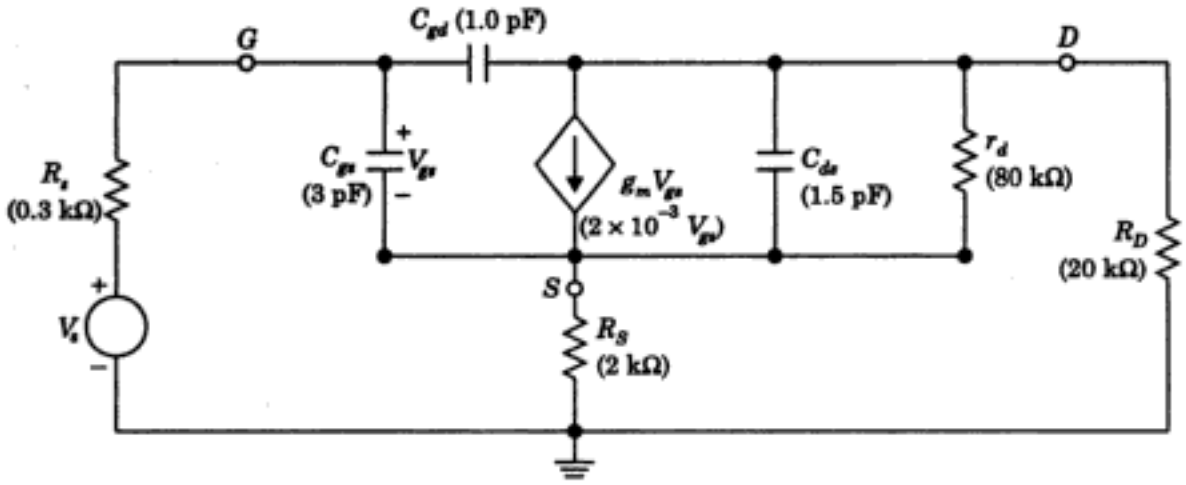


Fig. 10.94 The high frequency equivalent circuit of the common source stage with source resistance for the given amplifier circuit, P10.7.

P10.8 For the circuit shown in Fig. 10.95, determine the value of the dominant pole p_1 in rad/s.

(***Ans.*** $a_1 = 42225 \times 10^{-12}$ sec, $f_1 = 3.769$ MHz)

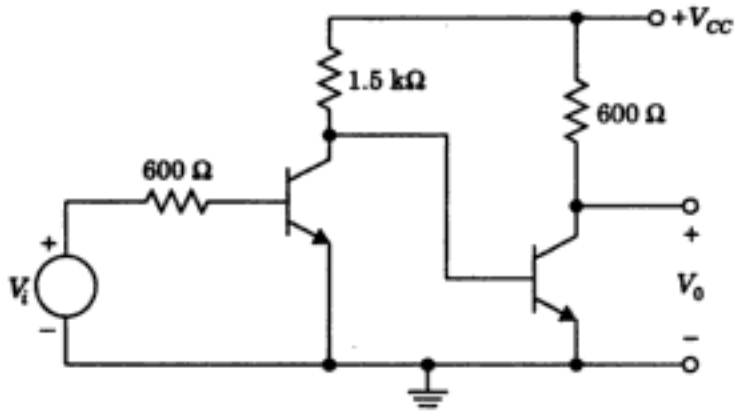


Fig. 10.95 The given circuit, P10.8.

P10.9 In the circuit shown in Fig. 10.96, Q_1 and Q_2 have $\beta_F = 150$, $V_A = 120$ V, $I_{CQ} = 100\,\mu$A, $f_T = 400$ MHz. Each transistor has $C_\mu = 0.5$ pF, and $R_S = 500$ kΩ, $R_C = 250$ kΩ. Determine the approximate value of 3 dB high frequency (i.e. f_H), by time constant method using dominant-pole approximation.

(***Ans.*** $a_1 = 1682.2$ ns, $f_H = 94.611$ kHz)

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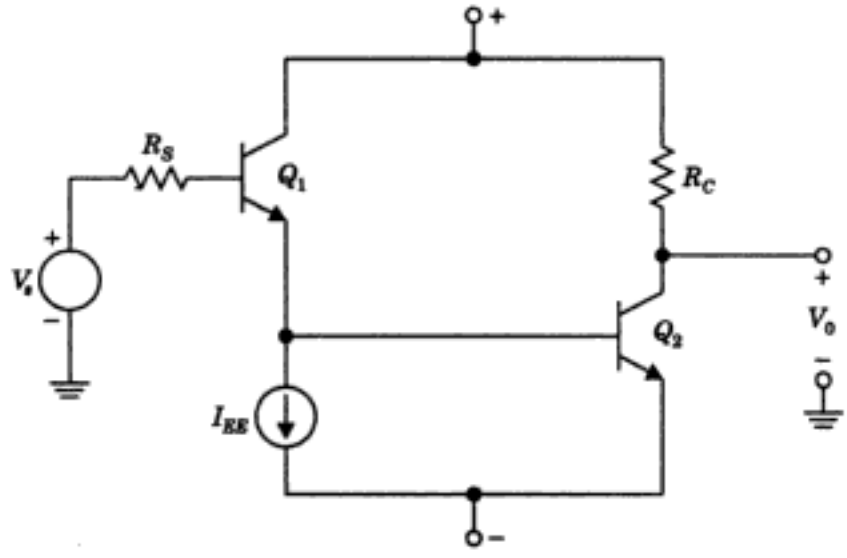


Fig. 10.96 The given circuit for P10.9.

P10.10 For the transistor circuit shown in Fig. 10.97,

(a) Determine the value of f_L.

(b) If $i(t)$ = 200 Hz square wave, determine the percentage tilt in the output.

(c) Find the lowest frequency square wave which gives not more than 2% tilt.

(***Ans.*** (a) 2.6525 Hz, (b) P = 4.167%, (c) f = 417 Hz)

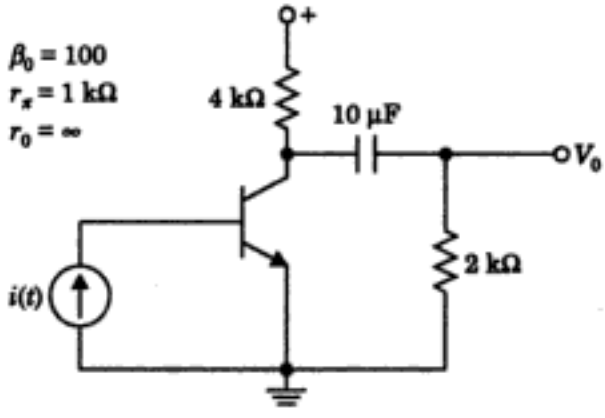


Fig. 10.97 The given circuit for P10.10.

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CHAPTER 11

Feedback Amplifiers

11.1 INTRODUCTION

Feedback is considered to be one of the fundamental processes in nature. For example, balancing the bicycle run, the mechanism of the hand-eye coordination to turn the page, the accelerator and brake control we use to drive an automobile at constant speed, maintaining constant internal body temperature, or the natural population control in an ecosystem etc. In fact, there are so many examples, where feedback constitutes a vital mechanism for the very operation.

In feedback, a portion of the output is returned to the input to form a part of the system excitation. This action, when appropriately applied, tends to make the system self-regulating, i.e., the system tends to stabilize and minimizes oscillations.

Feedback is also used to make the operating point of a transistor insensitive to both manufacturing variation of β_F** and temperature. In common emitter configuration, addition of a resistance R_E in the emitter circuit provides a –ve feedback and it helps to maintain constant gain if $\beta (= \alpha/(1 - \alpha))$ varies. The bandwidth of an op-amp having feedback resistances (R_2 and R_1) between the output and the input points is greater.

The high input resistance and low output resistance of an emitter follower (source follower) is also an example of feedback.

The negative feedback operation renders the advantages such as control of impedance, bandwidth improvement and rendering circuit performance relatively insensitive to manufacturing/environmental variations. Thus, by using the negative feedback, precision in the control systems can easily be achieved, besides other benefits as will be discussed in this chapter.

The input signal to the amplifier is proportional to the difference between the excitation and the fraction of the output signal in the case of negative feedbacks. We shall study its effects in detail.

**β_F refers to DC/quiescent state value of β. It will be seen later that the symbol β will also be used as a fraction of open loop gain which is fedback. We shall clarify this aspect as we progress.

There are the following disadvantages of the feedback:

(i) The gain gets reduced by negative feedback.

(ii) With positive feedback the amplifier may oscillate and be rendered useless. We, however, intentionally provide positive feedback for the case of oscillators.

(iii) The Miller effect multiplication of C_μ (or C_{gd} in FETs), which reduces to upper 3-dB frequency, is an undesirable effect of the negative feedback.

(iv) The parasitic elements such as the capacitance between the input and the output leads of an IC package simulate unwanted feedback effects.

We shall discuss the following topics in this chapter

- Classification of controlled amplifiers of four types
- The feedback concept, how it works
- Feedback amplifier topologies viz. shunt-shunt, shunt-series, series-series and series-shunt
- The ideal feedback amplifier, explaining the basic assumptions made, the return ratio (T) and calculation of feedback amplifier gain (A_F)
- Properties of negative feedback amplifiers. Its effect on sensitivity, non-linear distortion noise, and the bandwidth
- Impedance transformation by negative feedback due to the four types of topologies
- Approximate analysis of feedback amplifiers

11.2 CLASSIFICATION OF CONTROLLED AMPLIFIERS

Most of the amplifiers simulate *controlled sources*. This implies that an amplifier, designed in practice, aims at obtaining either a voltage controlled voltage source amplifier (VCVS) or a current controlled current source (CCCS), or a voltage controlled current source (VCCS) or a current controlled voltage source (CCVS). The ideal amplifiers should have either infinite input impedance (VCVS and VCCS) or infinite output impedance (CCCS, VCCS) or zero input impedance (CCCS, CCVS) or zero output impedance (VCVS and CCVS). However, it is not possible to achieve zero/infinite input or output impedances. The negative feedback, as we shall see in this chapter, will render the practically designed amplifier more close to the ideal (desired) ones. We first describe, briefly the four types of amplifiers.

The voltage amplifier: It resembles a practical op-amp circuit. Refer to Fig. 11.1.

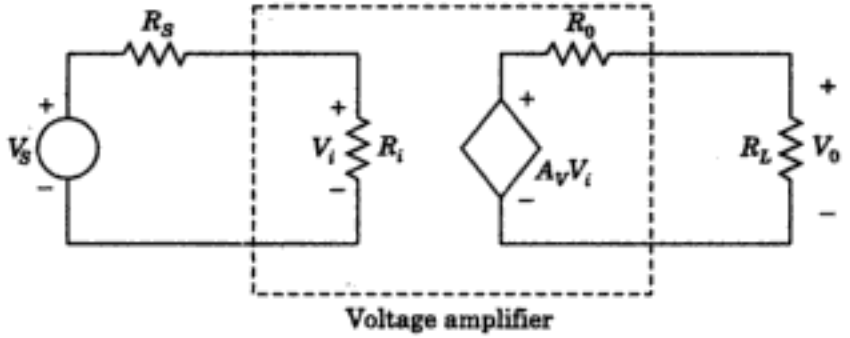


Fig. 11.1 Equivalent circuit of a voltage amplifier (To simulate VCVS).

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Ideally $R_i = \infty, \quad R_0 = 0$

If $R_L >> R_0$ and $R_S << R_i$ then

$$V_0 \approx A_V V_i \approx A_V V_S \quad (\text{if } R_S = 0, R_L = \infty)$$

$$\therefore \quad \boxed{A_V = \left.\frac{V_0}{V_i}\right|_{R_L \to \infty} \quad \text{(Open circuit voltage gain)}} \tag{11.1}$$

It is called a voltage-voltage converter and is a VCVS category.

The current amplifier: An ideal current controlled current source has $R_S \to \infty$, $R_0 \to \infty$ and $R_i \to 0$. If $R_L << R_0$ then referring Fig. 11.2, we have

$$I_0 = A_i I_i \quad (\text{if } R_0 >> R_L)$$
$$\approx A_i I_S \quad (\text{if } R_i << R_S)$$

$$\therefore \quad A_i = \frac{I_0}{I_S}, \quad \text{when } R_L = 0$$

Thus,

$$\boxed{A_i = \left.\frac{I_0}{I_i}\right|_{R_L = 0} \quad \text{(Short circuit current gain)}} \tag{11.2}$$

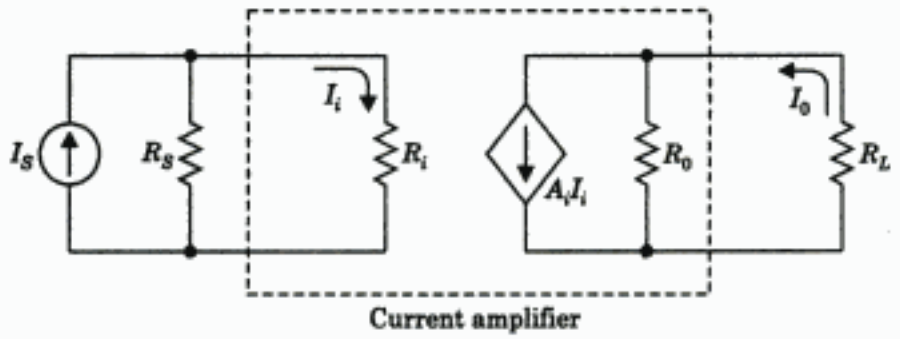


Fig. 11.2 Current amplifier equivalent circuit (To simulate CCCS).

Hence, the current amplifier in Fig. 11.2 acts as a CCCS.

The voltage-current converter **(Transconductance amplifier):** An ideal transconductance amplifier has $R_i \to \infty$, $R_0 \to \infty$. Referring Fig. 11.3, we write:

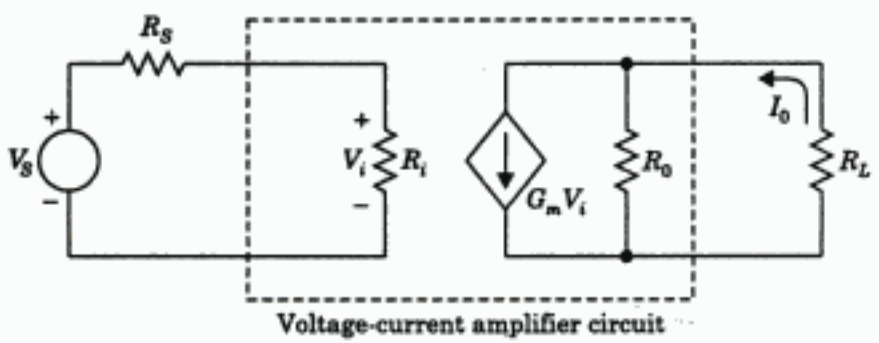


Fig. 11.3 Voltage-current amplifier circuit (To simulate VCCS).

If, $R_i >> R_S$ and $R_L << R_0$

Then $I_0 \approx G_m V_i \approx G_m V_S$

$$G_m = \left.\frac{I_0}{V_i}\right|_{R_L=0} \quad \text{(Short-circuit transconductance)} \tag{11.3}$$

The circuit in Fig. 11.3 acts as a VCCS.

The current-voltage converter **(Transimpedance amplifier):** For ideal cases $R_S \to \infty$, $R_0 \to 0$. Practically, $R_i << R_S$, $R_0 << R_L$. Then, in Fig. 11.4 we can write:

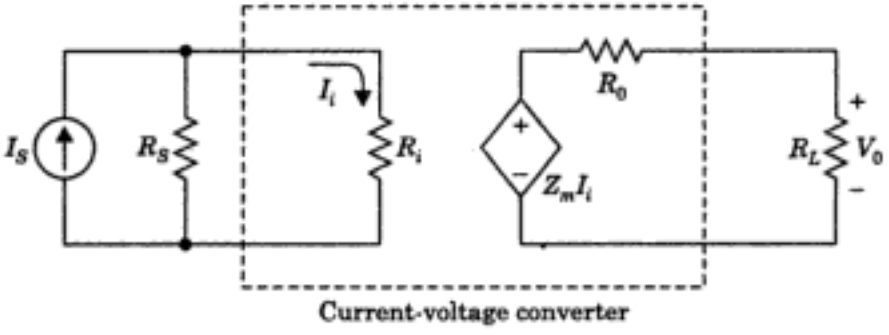


Fig. 11.4 Current-to-voltage (transimpedance) amplifier equivalent circuit (To simulate CCVS).

$$V_0 = Z_m I_i$$
$$= Z_m I_S$$

$$Z_m = \left.\frac{V_0}{I_i}\right|_{R_L \to \infty} \quad \text{(Open-circuit transimpedance)} \tag{11.4}$$

Hence, the circuit in Fig. 11.4 acts as a CCVS.

Table 11.1 Basic Amplifier Characteristics

Parameter	*Voltage Amp. (VCVS)*	*Current Amp. (CCCS)*	*Transconductance Amp. (VCCS)*	*Transimpedance Amp. (CCVS)*
Z_i	∞; $Z_i >> R_S$	0; $Z_i << R_S$	∞, $Z_i >> R_S$	0; $Z_i << R_S$
Z_0	0; $Z_0 << R_L$	∞; $Z_0 >> R_L$	∞; $Z_0 >> R_i$	0; $Z_m << R_L$
Gain or Transfer ratio	$V_0 \approx A_V V_S$	$I_0 \approx A_i I_S$	$I_0 = G_m V_S$	$V_0 \approx Z_m I_S$
Circuit model	Fig. 11.1	Fig. 11.2	Fig. 11.3	Fig. 11.4

In the first two rows (i.e., Z_i and Z_0), the ideal values are those shown first and the practical values follow 0 or ∞ thereon. In the third row (Gain or transfer ratio) if we replace almost equal signs ($\approx$) by equality signs ($=$), we shall get ideal controlled sources. As ideal values are impossible to achieve, the negative feedback methodology achieves "almost" ideal values.

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11.3 THE FEEDBACK CONCEPT

The use of feedback can make practical amplifier characteristics approach those of ideal amplifiers. For each amplifier, we sample (analog value) the output signal by a suitable network and transmit this (sampled) signal back to the input signal through a feedback network. The original input signal and the feedback signal are summed (compared, i.e., difference found) by means of a mixer network. This combined (summed up) signal is applied to the input of the basic amplifier. The main constituent elements of a feedback system are shown in Fig. 11.5.

(a) *The signal source (Input).* It represents the signal to be amplified. It may be a voltage source V_S in series with R_S or a current source I_S in shunt with R_S.

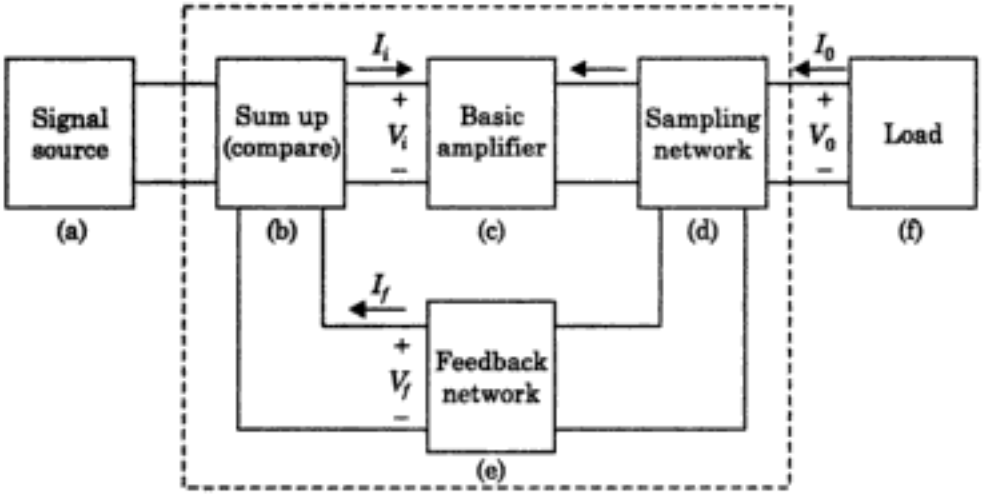
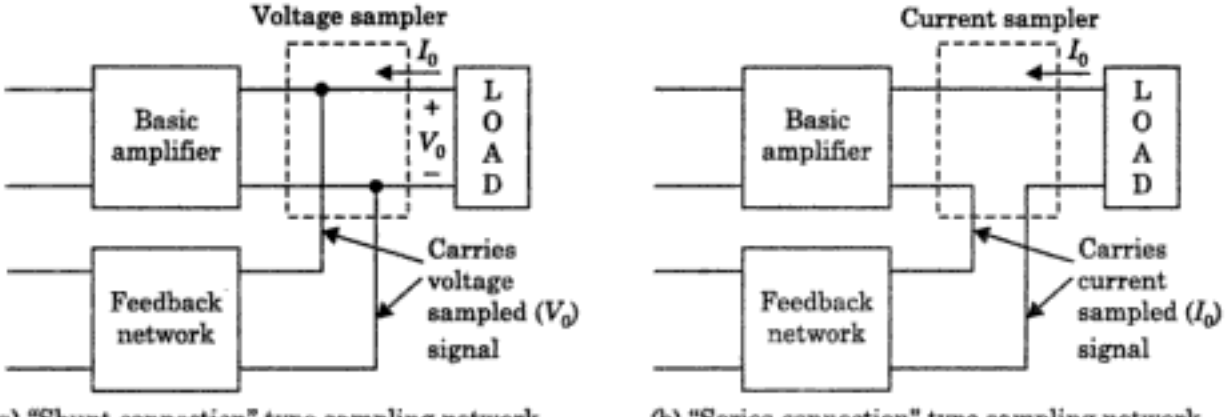


Fig. 11.5 The structure of a single-loop feedback amplifier. The basic amplifier may be any of the four circuits shown in Figs. 11.1 to 11.4.

(b) *The output signal.* It can be either a voltage across or the current in the load resistance R_L (or impedance Z_L). It is the output signal that we desire to be independent of the load and insensitive to parameter variations in the basic amplifier.

(c) *The sampling network:* It provides a measure of the output signal, i.e., a signal proportional to the output. Two sampling networks are shown in Fig. 11.6.



(a) "Shunt-connection" type sampling network (V_0 is sampled here)

(b) "Series-connection" type sampling network (Current I_0 is sampled here)

Fig. 11.6 Two types of sampling methods.

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For example, in Fig. 11.2, if, say, A_i increases due to β variation (say) then I_0 and, therefore, I_f also increases. The value $I_i = I_S - I_f$ decreases, i.e., the driving current to the basic amplifier decreases which decreases the amplifier's output, thus offsetting the effect of the increased A_i. This action is the basis of *negative feedback*. The summing network provides a difference signal, the amplifier output changes in a direction opposite to the change in the output. The net effect is to maintain a constant output signal which is independent of variations in gain (A_V or A_i or G_m or Z_m).

11.4 FEEDBACK AMPLIFIER TOPOLOGIES

As there are four types of basic amplifier topologies each approximating the characteristics of an ideal controlled source, so there are four basic signal-loop feedback amplifier topologies. These are as follows:

(i) *Shunt-shunt.* Input ports of feedback network connected in parallel to input signal and output of the amplifier also connected in parallel to the summing network via feedback network. Thus, here the currents are compared and voltage is sampled.

(ii) *Shunt-series.* Currents are compared and output currents are sampled.

(iii) *Series-series.* Voltages compared and output currents sampled.

(iv) *Series-shunt.* Voltages compared and output voltages sampled.

The first part of the nomenclature of these four topologies indicates the mechanism of summing or comparison. We can sum voltages in series and currents in shunt. Similarly, the second part of the nomenclature gives the method of sampling. We can sample voltage (V_0) by shunt connection and we sample current (I_0) by series.

Note: An alternative (old scheme as in many books) is based on the nomenclature where the first part indicates the quantity sampled, followed by input connection (mixing method) we shall, however, follow the new names.

New names *(Input connection, Output connection)*	*Old names* *(Quantity sampled, Input connection)*
Shunt—shunt	Voltage—shunt
Shunt—series	Current—shunt
Series—series	Current—series
Series—shunt	Voltage—series

The impedance levels decrease when the networks are connected in parallel and impedance levels increase when connected in series. Thus, for shunt-shunt configuration we expect low input and low output impedance. Similarly, in shunt-series, we expect low input and high output impedance. This also implies that if we wish to increase the input impedance for the feedback amplifier, we may choose either *series-series* or *series-shunt* configuration. Similarly, if we wish to decrease output impedance, the topologies *shunt-shunt* or *series-shunt* may be chosen.

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11.5 THE IDEAL FEEDBACK AMPLIFIER

Each of the four feedback amplifier (FBA) topologies has several common characteristics. A generic representation of a feedback amplifier is shown in Fig. 11.8.

In Fig. 11.8, the input signal X_S, the output signal X_0, the feedback signal X_f and the difference (comparison) signal X_i each represents either a voltage or the current Σ is a summing network. Thus,

$$X_i = X_S + X_f \tag{11.5}$$

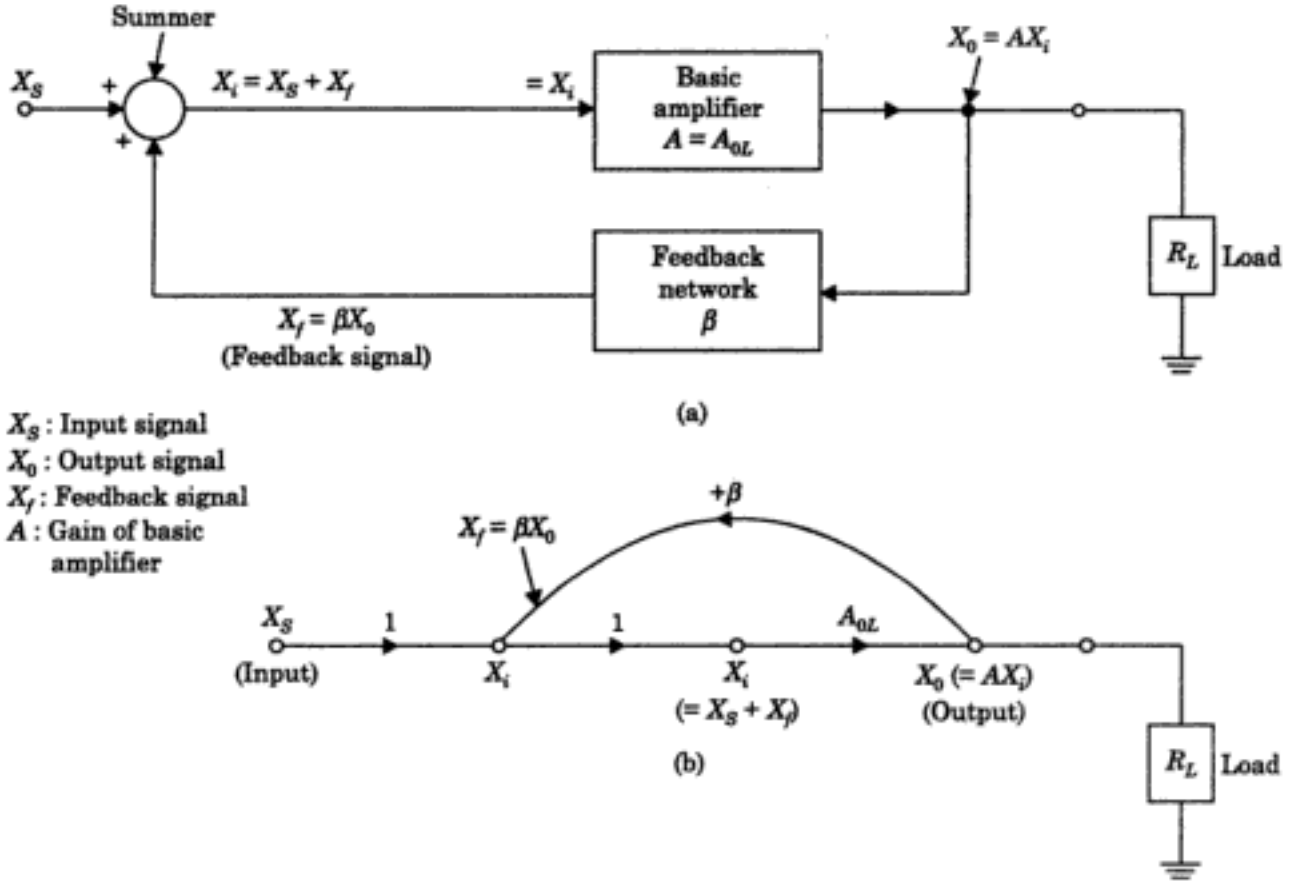


Fig. 11.8 A feedback amplifier model (generic) (a) block diagram, (b) signal-flow graph representation.

Note: In Fig. 11.8(b), the arrows indicate the gains and nodal values or the output 'potential' or 'voltage' at the node. When an arrow has been shown with a parameter/scaling factor then the signal gets multiplied by this scaling factor. A blank arrow (with no scaling factor shown) implies a scaling factor of unity, i.e., the signal just passes with no change.

The signal X_i is the output of the summing network. If the feedback signal X_f is 180° out of phase with the input X_S, as is true in negative-feedback systems, then $|X_i| = |X_S| - |X_f|$, i.e., $|X_i|$ decreases as $|X_f|$ increases.

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Table 11.2 Signals and Transfer Ratios in Feedback Amplifiers Along with Various Other Parameters

Signal or Ratio	*Feedback Topology*			
	Shunt-shunt	*Shunt-series*	*Series-series*	*Series-shunt*
X_0	Voltage (V_0)	Current (I_0)	Current (I_0)	Voltage (V_0)
X_S, X_i, X_f	Current (I_S, I_i, I_f)	Current (I_S, I_i, I_f)	Voltage (V_S, V_i, V_f)	Voltage (V_S, V_i, V_f)
$A = A_{0L}$ (a ratio)	V_0/I_i (Z_m)	I_0/I_i (A_i)	I_0/V_i (G_m)	V_0/V_i (A_V)
β (a ratio)	I_f/V_0	I_f/I_0	V_f/I_0	V_f/V_0

The reverse transmission of the feedback network, denoted by β is:

$$\beta = \frac{X_f}{X_0} \tag{11.6}$$

The transfer ratio β is often a real number but, in general, is a function of frequency. (*Note* that β used here is NOT the one used in BJT which was the *CE* short circuit current gain).

The name reverse transmission associated with β is logical, as it indicates the "fraction of output signal" ($= \beta X_0$) that is fedback (in the reverse direction).

The open loop gain of the amplifier A, is defined by

$$A = \frac{X_0}{X_i} \tag{11.7}$$

We may also use the symbol A_{0L} (instead of A) for open loop gain.

From Eqs. (11.6) and (11.7), we have

$$A\beta = \frac{X_0}{X_i} \times \frac{X_f}{X_0}$$

or

$$A\beta = \frac{X_f}{X_i} \tag{11.8}$$

The gain with feedback is obtained by

Feedback gain: $$A_F = \frac{X_0}{X_S} = \frac{X_0}{X_i - X_f} \qquad \left(\because\ X_i = X_S + X_f \;\Rightarrow\; \therefore\ X_S = X_i - X_f\right)$$

$$= \frac{X_0/X_i}{1 - X_f/X_i} \qquad \text{(Dividing num. \& denom by } X_i\text{)}$$

$$= \frac{A}{1 - A\beta} \qquad \left(\because\ X_0/X_i = A, \text{ from Eq. (11.7)};\ \text{and } X_F/X_i = A\beta, \text{ from Eq. (11.8)}\right)$$

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$$\therefore \quad \boxed{\text{Feedback gain } A_F = \frac{A}{1 - A\beta} = \frac{A_{0L}}{1 - A_{0L}\beta} \quad \text{(closed-loop gain)}} \tag{11.9}$$

where A_{0L} = transfer function without feedback (open-loop gain)

For negative feedback, $|A_F| < |A|$; and $|1 - A\beta| > 1$.

Note that if $\beta = 0$ (i.e. no feedback) then $A_F = A$, as expected. *A is* called **open-loop gain** *($\beta = 0$)* **and often denoted as** A_{0L}. A_F (when $\beta \neq 0$) is also called **closed-loop gain.**

If $|A_F| < |A_{0L}|$, it is negative feedback, if $|A_F| > |A_{0L}|$, it is positive feedback case. We do not let $|A_F|$ exceed $|A_{0L}|$ in negative feedback circuits. We may let $|A_F|$ exceed $|A_{0L}|$ in oscillators (see Chapter 12). Where we use A, it would be taken as A_{0L} in this chapter.

The return ratio or loop gain (T): It is seen in Fig. 11.8 that the signal X_i is multiplied by A in passing through the amplifier and then by β in transmission through the feedback network. Such a path takes us from the amplifier input X_i to its output AX_i to $A\beta X_i$ to the input point again. The product $-A\beta$ is called **loop gain** or **return ratio** T. Thus, Eq. (11.9) can be written as:

$$A_F = \frac{A}{1 - \beta A} = \frac{A_{0L}}{1 + T} = \frac{A_{0L}}{F} \tag{11.10}$$

where $T = -A\beta$ and $T > 0$ for –ve feedback, i.e. **T is always a +ve quantity.**

In the literature, another parameter called **return difference** F is also mentioned. We define F by

$$F = 1 + T \tag{11.11}$$

We shall see that the factor $(1 + T)$ appears in many calculations.

The return ratio $(-A\beta)$ is the negative of the ratio of the fedback signal (X_f) to the amplifier input (X_i). Often, the quantity $F = 1 - A\beta = 1 + T$ is referred to as the return difference. *In negative feedback case, both T and F are positive quantities* (In some standard books symbol D is used instead of F here).

To determine A_F from signal flow graph: From the signal flow graph, Fig. 11.9, we have

$$X_i = X_S + \beta X_0$$

i.e., $$X_i = X_S + \beta A X_i \qquad (\because X_0 = AX_i)$$

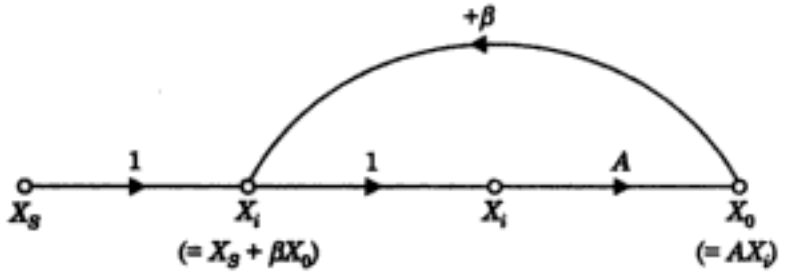


Fig. 11.9 The signal-flow graph of ideal feedback amplifier.

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$$\therefore \quad X_i - \beta A X_i = X_S$$

$$\text{or} \quad \frac{X_i}{X_S} = \frac{1}{1 - \beta A}$$

$$\therefore \quad \frac{X_0}{X_S} = \frac{A X_i}{X_S} = \frac{A}{1 - \beta A}$$

$$\text{i.e.,} \quad \boxed{A_F = \frac{A}{1 - \beta A} = \frac{A}{1 + T}} \tag{11.12}$$

as found earlier. Thus, the signal-flow graph method is simpler for calculation of feedback gain A_F.

Before we tackle practical questions/numericals, we make some assumptions for obtaining *approximate* results. Thereafter, we shall explain the procedure to obtain *exact* results in feedback analysis.

Fundamental assumptions: Three major assumptions made (for approximate analysis) in the ideal feedback amplifiers, are as follows:

1. The *feedback network is unilateral*. It implies that the input signal is transmitted to the output through the amplifier A and NOT through the feedback network β. If the amplifier is deactivated by making $A = 0$ (say, by making $g_m = 0$ in the transistor) then the output signal must become zero.
2. The *amplifier A is unilateral* and transmits signal only from the input to the output, i.e. the feedback signal (βX_0) is transmitted from output to the input through the feedback network only, and not through other path.
3. The transfer ratio β *is independent* of the source and load resistances R_S and R_L, respectively.

In practical amplifiers, the feedback network usually consists of passive elements (R, C, L) and thus transmits a signal from input to output also. Also, both A and β are affected by the load and source resistances. Such deviations from the idealities, can, however, be ignored in the approximate analysis method, which we propose in Section 11.8.

EXAMPLE 11.1

A feedback amplifier is to be designed to have a closed-loop gain of 50 ± 0.1. The basic amplifier has a gain which can be controlled to within ±10%. Determine the values of open-loop gain, the return ratio and the reverse transmission β of the feedback network.

Solution: Here $A_{0L} = A_{0L}$ with ± 10% variation. Let exact open loop gain (ideal) = $A_{0L} = A$, say

and $$T = |\beta A_{0L}| = \beta A \text{ (ideal) call } \beta A = B, \text{ (say)}$$

As $$A_F = \frac{A_{0L}}{1 + T} = \frac{A}{1 + B} \text{ (ideal)}$$

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Again when $A_{0L} = 0.9A$, $A_F = 50 - 0.01 = 49.99$

$$\therefore \quad 49.99 = \frac{0.9A}{1 + \beta(0.9A)}$$

$$49.99(1 + 0.9\beta A) = 0.9A$$

or $$49.99 + 0.9A(49.99\beta - 1) = 0 \qquad \text{(ii)}$$

Solving Eqs. (i) and (ii) for A and β,

$$50.01 + 1.1A(50.01\beta - 1) = 0 \quad | \times 0.9$$

$$49.99 + 0.9A(49.99\beta - 1) = 0 \quad | \times (-1.1)$$

$$\therefore \quad (50.01 \times 0.9 - 49.99 \times 1.1) + A\beta[1.1 \times 0.9 \times 50.01 - 1.1 \times 0.9 \times 49.99] = 0$$

or $$-9.98 = -1.1 \times 0.9A\beta(50.01 - 49.99)$$

or $$A\beta = +9.98/(1.1 \times 0.9 \times 0.02) = +504.040404$$

Putting $A\beta = -504.040404$ in Eq. (i), we obtain

$$50.01 + 1.1 \times 50.01(+504.040404) = 1.1A$$

or $$50.01 + 27727.76666 = 1.1A$$

or $$A = +25252.525 \quad \textbf{Ans.}$$

$$\therefore \quad \beta = +504.040404/(+25252.525) = 0.01996 \quad \textbf{Ans.}$$

Check When $A_{0L} = 0.9 \times 25252.525 = 22727.2725$ (i.e. 10% below ideal value)

Then $$A_{F1} = \frac{22727.2725}{(1 + 0.01996 \times 22727.2725)}$$

$$= 49.990002 = 49.99$$

When $A_{0L} = 1.1 \times 25252.525 = 27777.7775$ (i.e. 10% above ideal value)

Then $$A_{F2} = \frac{27777.7775}{(1 + 0.01995 \times 27777.7775)}$$

$$= 50.010002 \approx 50.01$$

Thus, the values of $A_{0L} = 25252.525$ and $\beta = 0.01996$ are correct. **Ans.**

Note: It may be seen that if wish to have very small variation of the gain (as was the case in this example, we require the open loop gain A_{0L} very high (as in the Op-ams) and sufficient feedback constant β.

11.6 PROPERTIES OF NEGATIVE FEEDBACK AMPLIFIERS

The negative feedback reduces the gain (by a factor $\frac{1}{1+T} = \frac{1}{1-\beta A}$). But there are other advantages, and that is why it is very popular, and extensively used in practical situations.

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Again if $\Delta T = -25$ then

$$\frac{\Delta A_F}{A_F} = \frac{-25}{49} \times \frac{1}{1+49-25} = \frac{-1}{49} \approx -2\%$$

Thus 50% variation in T has produced variation in A_F from –2% to 2/3% only. This illustrates the effectiveness of the negative feedback. Thus, the closed-loop gain A_F can be controlled precisely even when the internal amplifier gain A varies substantially. Note that

$$A_F = -\frac{1}{\beta}\frac{T}{1+T} \qquad \text{[due to Eq. (11.15)]}$$

$$= -\frac{1}{\beta}, \text{ if } T >> 1$$

As β is the transfer function of the usually passive feedback network, *A_F is essentially indepenent of the gain A_{OL} of the basic amplifier.* A_F depends only on the ratio (β) of passive components. For similar reason, we observe that in operational amplifiers (Op-amp), the inverting and also non-inverting gains are proportional to $-R_2/R_1$ or $(1 + R_2/R_1)$, i.e. on the ratio R_2/R_1 and not on the open loop gain of the Op-amp.

11.6.2 Non-linear Distortion (Effect of Negative Feedback on Distortion)

Obtaining a distortionless amplified signal is always a desired feature. Practically, an amplifier may behave linear for small signals. However, for large input signals, it becomes non-linear, and the output waveform is distorted.

A typical voltage amplifier is shown in Fig. 11.10 and its transfer characteristic in Fig. 11.11. *The slope of the transfer characteristic curve in Fig. 11.11 gives the voltage gain.* The voltage gain A_V here is 100 for $|v_i| \le 40$ mV. In the non-linear portion, the voltage gain A_V is < 100 and A_V is zero for $|v_i| \ge 60$ mV (In a BJT, when $A_V = 0$, it corresponds to cutoff or saturation region). Thus, in the given characteristic, there is distortion in the output V_0 for $|v_i| > 40$ mV. We may express it analytically, typically as follows:

$$|V_o| = \begin{cases} 100 \,.\, |v_i| & \text{for} \quad |v_i| \le 40 \text{ mV} \\ 100 \,.\, |v_i| - (50\,|v_i| - 2)^2, & 40 \le |v_i| \le 60 \text{ mV} \\ 5, & |v_i| \ge 60 \text{ mV} \end{cases} \tag{11.19}$$

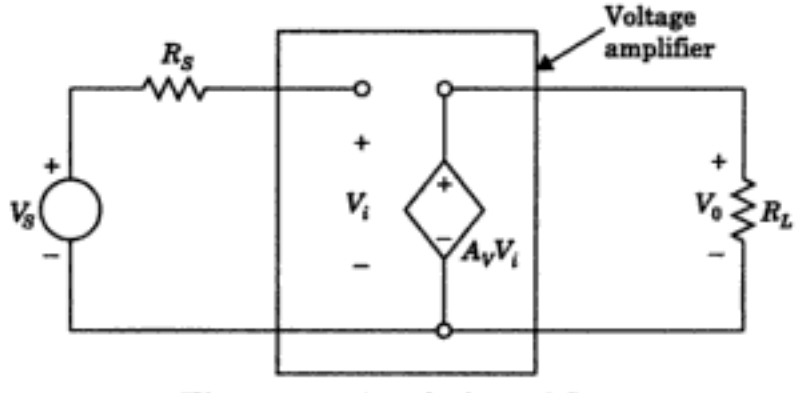


Fig. 11.10 An ideal amplifier.

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or $A_{0L} = -1285$ ($\because$ it is a negative amplifier)

(a) Here $\beta = 1.2\% = 0.012$

$\therefore$ $T = -\beta A_{0L} = \beta(-A_{0L}) = 0.012 \times 1285 = 15.42$

$\therefore$ Output is fundamental,

$$B_1|_{\text{with feedback}} = V_S \cdot A_F$$

$$= 0.028 \frac{|A_{0L}|}{1+T}$$

$$= 0.028 \frac{1285}{1+15.42}$$

$$= 2.19 \text{ V} \quad \textbf{Ans.}$$

Note that with feedback, the distortion voltage is:

$$B_2|_{\text{with feedback}} = \frac{B_2}{1+T}$$

$$= \frac{0.07 \times 36}{1+15.42} = \frac{2.52}{1+15.42} = 0.1535 \text{ V} \quad \text{(i.e., 7\% of the 1st harmonic)}$$

Thus, with 1.2% feedback, the fundamental (B_1) as well as the distortion (B_2) get reduced by a factor (1 + T). In unfedback case B_1 = 36 V, B_2 = 2.52 V. With 1.2% negative feedback,

$$B_{1F} = 2.19 \text{ V}$$

$$B_{2F} = 0.1535 \text{ V}$$

Note that with –ve feedback, both B_1 and B_2 get reduced by a factor 1/1 + T and percentage viz. B_{2F}/B_{1F} remains unchanged if input V_S is kept constant.

(b) Here, the output $B_{1F} = 36$ V

B_{2F} = 1% of B_{1F} = 1% of 36 V

i.e. $\dfrac{B_{2F}}{B_2} = \dfrac{1}{7}$ $\begin{cases} \because \text{ 2nd harmonic with no feedback = 7\%} \\ \because \text{ 2nd harmonic with feedback = 1\%} \end{cases}$

But $B_{2F} = \dfrac{B_2}{(1+T)}$ $\therefore$ $1 + T = T$ or $T = 6$

and $|A_F| = \dfrac{|A_{0L}|}{(1+T)} = \dfrac{1285}{(1+6)} = 183.57$

New input $\bar{V}_S = \dfrac{B_{1F}}{A_F}$

$$= \frac{36}{183.57} = 0.196 \text{ V}$$

The new input is $\bar{V}_S$ = 0.196 V which yields an output of B_{1F} = 36 V and B_{2F} = 1% of B_{1F}. **Ans.**

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The situation here is as if the "signal input" is $\left(V_s + \frac{V_n}{A_2}\right)$ to an amplifier with gain (A_1A_2) alongwith feedback network (β). Thus we can write V_0 = (Input signal) × (Gain of feedback amplifier) i.e.

$$V_0 = \left(V_s + \frac{V_n}{A_2}\right) \cdot \frac{A_1A_2}{1 + \beta A_1A_2}$$

$$= \underbrace{V_s \frac{A_1A_2}{1 + \beta A_1A_2}}_{\text{Signal part}} + \underbrace{V_n \frac{A_1}{1 + \beta A_1A_2}}_{\text{noise part}}$$

$$\therefore \quad \text{Output SNR} = \frac{V_s \dfrac{A_1A_2}{1 + \beta A_1A_2}}{V_n \dfrac{A_1}{1 + \beta A_1A_2}}$$

$$\therefore \quad \boxed{\text{With feedback, SNR} = \frac{A_2V_s}{V_n} = A_2 \times \text{SNR (with no feedback)}} \qquad (11.25)$$

Thus, O/P SNR is A_2 times that of the earlier case (A_1 only). A_2 may only be a voltage amplifier, with low current drain from power supply, hence less noisy. In general, hum noise is due to high current. For low currents, power supply hum noise may be negligible and therefore, A_2 behaves as noiseless amplifier.

An alternative proof of noise reduction: The noise reduction is achieved by feeding back the 'noisy output' such that a stage before the noisy amplifier stage is 'noiseless'. Figure 11.21 shows a noisy amplifier A_1.

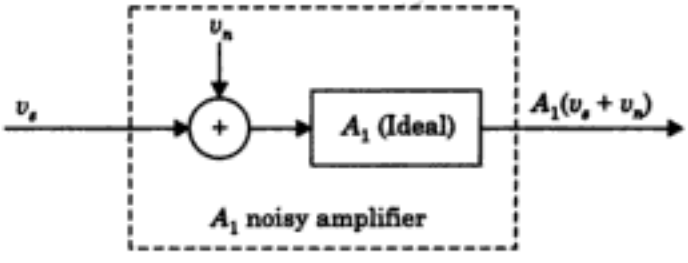


Fig. 11.21 A noise signal introduced by a noisy amplifier.

If amplifier A_1 is noisy, then

$$\text{Input SNR} = \frac{v_s}{v_n}$$

and $$\text{Output SNR} = \frac{A_1v_s}{A_1v_n} = \frac{v_s}{v_n} = \text{Input SNR}$$

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Now, precede A_1 (noisy amplifier) by an amplifier A_2 (a noiseless amplifier) and allow overall negative feedback, as shown in Fig. 11.22.

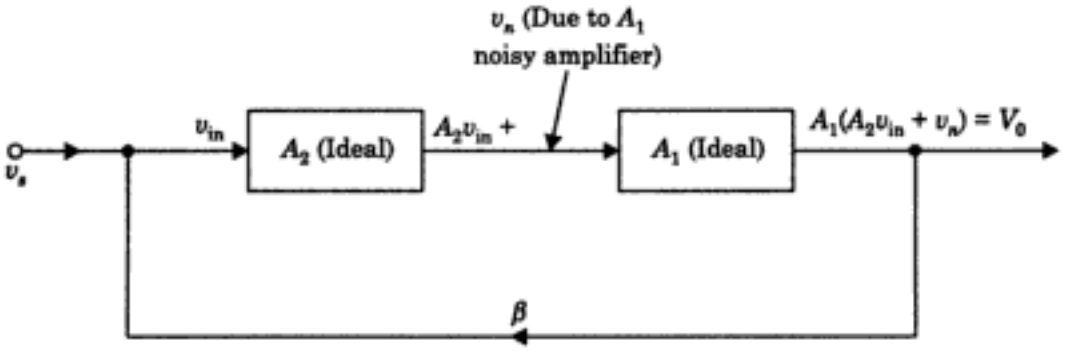


Fig. 11.22 Direct proof of noise reduction by using A_2 a noiseless amplifier before a noisy amplifier, A_1. Amplifier A_1 adds noise v_n to its output signal.

Input is v_s, A_2(ideal), (A_1 and v_n) noisy amplifier,

$$v_{in} = v_s + \beta V_0 = v_s + \beta(A_1A_2v_{in} + A_1v_n) \quad \text{(i)}$$

$$\therefore \quad (1 - \beta A_1A_2)v_{in} = v_s + \beta A_1v_n$$

$$\text{or} \quad v_{in} = (v_s + \beta A_1v_n)/(1 - \beta A_1A_2) \quad \text{(ii)}$$

Now,

$$V_0 = A_1A_2v_{in} + A_1v_n$$

$$= A_1A_2\left[\frac{v_s + \beta A_1v_n}{1 - \beta A_1A_2}\right] + A_1v_n \qquad \text{(using (ii))}$$

$$= \frac{A_1A_2v_s}{1 - \beta A_1A_2} + A_1v_n\left\{1 + \frac{\beta A_1A_2}{1 - \beta A_1A_2}\right\}$$

$$= \frac{A_1A_2v_s}{1 - \beta A_1A_2} + \frac{A_1v_n}{1 - \beta A_1A_2}$$

$$= \frac{A_1A_2}{1 - \beta A_1A_2}\left[v_s + \frac{1}{A_2}v_n\right] = A_Fv_s + \left(\frac{A_F}{A_2}v_n\right)$$

Clearly,

$$\left.\frac{\text{Signal}}{\text{Noise}}\right|_{\text{at output}} = \frac{v_s}{\frac{1}{A_2}v_n} = A_2\frac{v_s}{v_n} = A_2 \times \text{Input SNR (without } A_2 \text{ and with no feedback)}$$

This is the same result as in Eq. 11.25, obtained earlier.

EXAMPLE 11.5

Consider a power-output stage with voltage gain $A_1 = 1$, an input signal $V_s = 1$ V, and a hum signal V_n of 1 V. Assume that this power stage is preceded by a small signal with gain $A_2 = 100$ V/V and that overall feedback with $\beta = 1$ is applied. If V_S and V_n remain unchanged, find the signal and noise voltages at the output and hence the improvement in S/N ratio.

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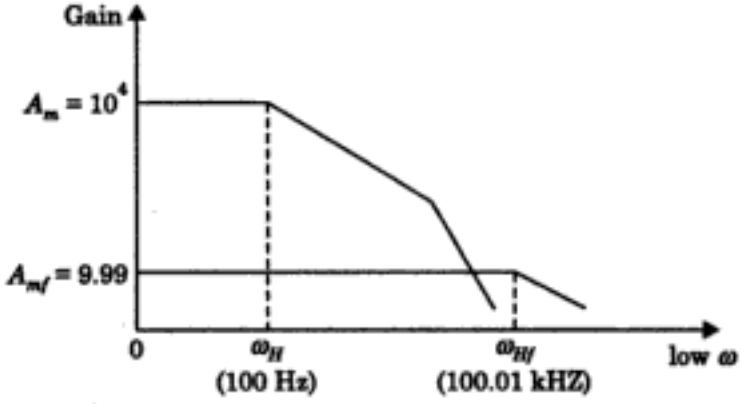
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EXAMPLE 11.7

Consider the non-inverting operational amplifier of Example 11.6. Let the open-loop gain A have a low frequency values of 10^4 and a uniform −6 dB/octave roll off at high frequencies with a 3 dB frequency of 100 Hz. Find the low frequency gain and the upper 3 dB frequency of a closed-loop amplifier, with $R_1 = 1\ k\Omega$, $R_2 = 9\ k\Omega$.

Solution: Refer to Fig. 11.24 and Fig. 11.25 showing various parameters. As in Example 11.6,

$$\beta = \frac{R_1}{R_1 + R_2} = \frac{1}{1+9} = \frac{1}{10}$$



ω_H = 100 Hz upper 3 dB cut off with no feedback

$A_M = 10^4$ mid band (dc frequency) gain

Fig. 11.25 Frequency response given in Ex. 11.7.

Now,
$$A_{fM} = \frac{A_M}{(1 + \beta A_M)}$$

$$= \frac{10^4}{1 + \frac{1}{10} \times 10^4} = \frac{10^4}{1001} = 9.99001 \quad \textbf{Ans.}$$

and
$$\omega_{Hf} = \omega_H(1 + \beta A_M)$$

$$= 100\left(1 + \frac{1}{10} \times 10^4\right) = 100(1001) = 100100 = 100.01 \text{ kHZ} \quad \textbf{Ans.}$$

11.7 IMPEDANCE IN FEEDBACK AMPLIFIERS

The ideal input and output impedances of amplifiers can never be achieved in practice. However, it is possible to improve upon the impedances by the use of negative feedback technique. In this section, we shall show that the feedback amplifiers can be used to make practical amplifier characteristics approximate those of ideal amplifiers. To do so we shall require that the input and the output resistances (impedances) of the feedback amplifiers

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or
$$\frac{V}{I_S} = \boxed{R_{1F} = \frac{R_i}{1-\beta A} = \frac{R_i}{1+T}} \tag{11.27}$$

For shunt-series or shunt-shunt, $R_{1F} < R_i$ as $(1 + T)$ is always ≥ 1 for negative feedback. Clearly, when $\beta = 0$, i.e., $T = 0$ then $R_{1F}\big|_{\beta=0} = R_i$, the no feedback case.

Note: In Fig. 11.27, I_S and I_f are of opposite phase, hence I_i has lower magnitude than that of I_S. This causes lower value of $V(= I_i R_i)$ than $I_S \cdot R_i$. A low voltage drop across the input is equivalent to lower impedance offered by the input device, i.e., low input offered by the amplifier.

Output Impedance R_{0F}:

(a) *Shunt sampling on output side:* When the output of a feedback amplifier employs a shunt connection, negative feedback reduces the output impedance. This statement is true for both shunt-shunt as well as series-shunt, i.e., irrespective of the input connections. Assuming β independent of load resistance and the output voltage V_0 is due to basic amplifier, i.e., AX_i.

We know that, see Fig. 11.28,

$$V_0 = A_F X_S$$

i.e.
$$V_0 = \frac{A}{1-\beta A} X_S$$

Now,
$$I_{SC} = \frac{V_0}{R_0}\bigg|_{\beta=0} = \frac{AX_S}{R_0}$$

(∵ shorting terminals 1 and 2 renders $V_0 = 0$, this amounts to $\beta = 0$)

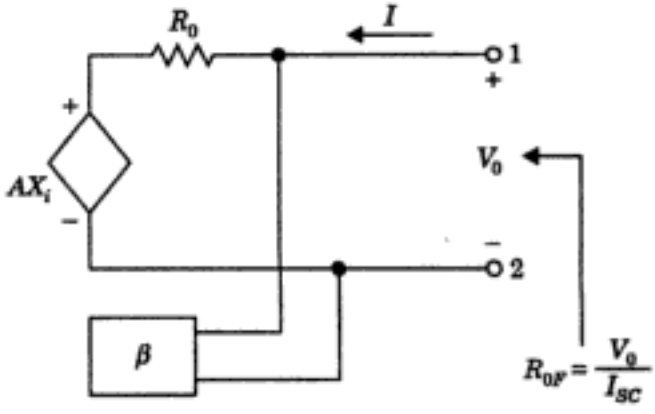


Fig. 11.28 Shunt output connection to compute R_{0F}.

$$R_{0F} = \frac{V_0}{I_{SC}} = \frac{AX_S/(1-\beta A)}{AX_S/R_0} = \frac{R_0}{1-\beta A}$$

Hence
$$\boxed{R_{0F} = \frac{V_0}{I_{SC}} = \frac{R_0}{1-\beta A} = \frac{R_0}{1+T}} \quad ** \quad \text{(for series-shunt and for shunt-series)} \tag{11.28}$$

Clearly, when $\beta = 0$, $R_{0F}\big|_{\beta=0} = R_0$, as expected.

(b) ***Series sampling on output side.*** The output impedance is increased when a negative-feedback amplifier employs a series-connected output (and is independent of the input configuration, i.e., whether it is series-series or shunt-series). Consider Fig. 11.29. To find R_{0f}, disconnect X_S (no signal), apply a voltage V across terminals 1 and 2, measure current I.

***Or directly (alternative proof)*

To find R_{0F}, disconnect X_S, apply a voltage, say, V across terminals 1 and 2 and find current I. Then $V/I = R_{0F}$.

Here
$$AX_i = A(X_S + X_f) = A(0 + \beta V) = A\beta V$$

$$I = \frac{(V - AX_i)}{R_0} = \frac{(V - A\beta V)}{R_0} = V \cdot \frac{1-\beta A}{R_0}$$

$$R_{0F} = \frac{V}{I} = \frac{R_0}{(1-\beta A)} = \frac{R_0}{(1+T)}, \text{ as expected}$$

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Then $R_{0F} = V/I$.

As $$AX_i = A(X_S + X_f)$$
$$= A(0 + \beta I) \quad (\because X_S = 0 \text{ and } X_f = \beta I)$$

$$I = \frac{V}{R_0} + AX_i = \frac{V}{R_0} + A\beta I$$

(assuming drop in β network to be zero volt)

or $$I(1 - A\beta) = \frac{V}{R_0}$$

$$\therefore \quad R_{0F} = \frac{V}{I} = R_0(1 + T) \quad (\because -A\beta = T)$$

or $$\boxed{R_{0F} = R_0(1 - A\beta) = R_0(1 + T)} \; ** \quad (11.29)$$

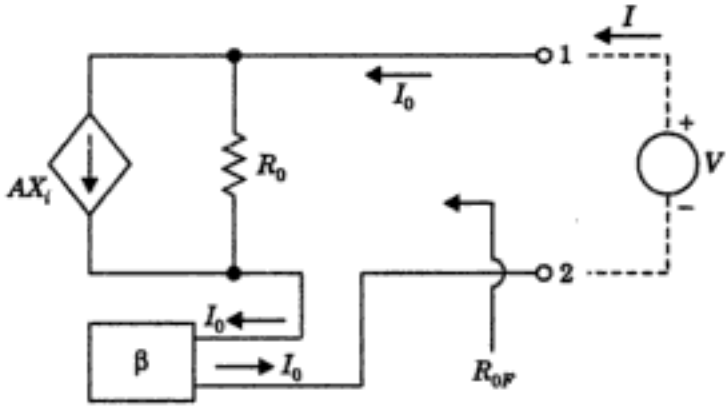


Fig. 11.29 Series output connection to compute R_{0F}.

for series-shunt and for shunt-series

Table 11.4 gives the various useful results for ready reference.

Table 11.4 Properties of Feedback Amplifier Structures Showing Various Parameters and R_{1F}, R_{0F}

Topology	*Amplifier Classifiation (A)*	*Comparison Signal (X_S, X_f)*	*Output Signal (Sample) (X_0)*	*Input Impedance (R_{1F})*	*Output Impedance (R_{0F})*
Shunt-shunt	Current to voltage converter (Z_m)	Current (I_S, I_f)	Voltage (V_0)	Low $R_i/(1 + T)$	Low $R_0/(1 + T)$
Shunt-series	Current amplifier (A_i)	Current (I_S, I_f)	Current (I_0)	Low $R_i/(1 + T)$	High $R_0(1 + T)$
Series-series	Voltage to current converter (G_m)	Voltage (V_S, V_f)	Current (I_0)	High $R_i(1 + T)$	High $R_0(1 + T)$
Series-shunt	Voltage amplifier (A_v)	Voltage (V_S, V_f)	Voltage (V_0)	High $R_i(1 + T)$	Low $R_0/(1 + T)$

****Alternatively**

If we short terminals 1 and 2 to get I_{SC}, then we can write

$$I_{SC} = -I_0 = -A_F X_S = -\frac{A}{1 - \beta A} X_S$$

$$V_{0C} = -AX_i R_0 = -AR_0(X_S + 0) = -AR_0 X_S$$

[$\because$ with 1, 2 open circuit $I_0 = 0 \quad \therefore \quad \beta I_0 = X_f = 0$ (Note this step)]

$$\therefore \quad \frac{V_{0C}}{I_{SC}} = R_{0F} = \frac{-AR_0 X_S}{-\frac{A}{1 - \beta A} X_S} = R_0(1 - \beta A) = R_0(1 + T), \text{ as expected.}$$

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Solution [*Topology determination*]:

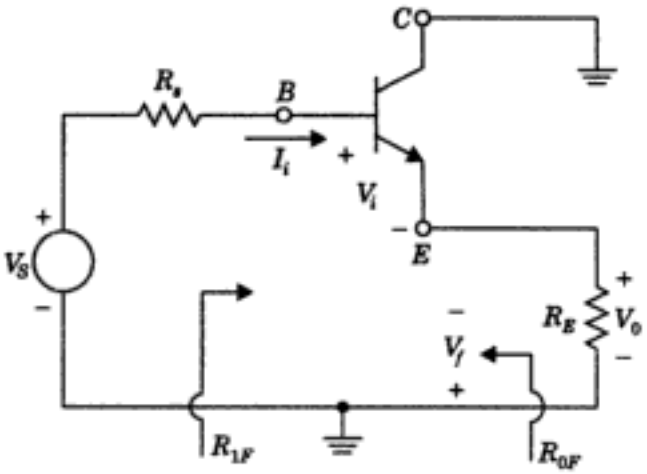


Fig. 11.30 Emitter follower (Given circuit). Ex. 11.8.

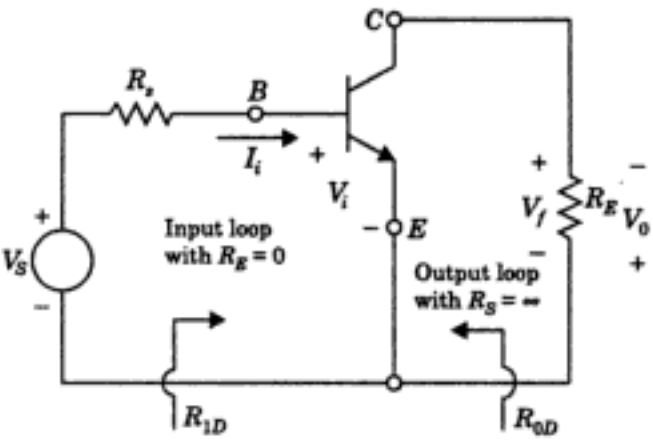


Fig. 11.31 The circuit of emitter follower without feedback (to find A_{0L} or A_D)

The input V_i contains a component R_E which is connected to the output voltage V_0. Clearly, the input is the series connected topology and

$$V_i = V_S + V_f \quad (\because X_i = X_S + X_f)$$

The feedback voltage V_f is measured across R_E and the polarity of V_f is so chosen to make $X_i = X_S + X_f$ in the summing network. So polarity of V_f is as shown in Fig. 11.30.

Note that V_f is negative of V_0. As V_0 increases, $V_i = V_S + V_f$ decreases, so it is the case of –ve feedback.

To decide upon output topology, if we short-circuit the output terminal, i.e., make $R_E = 0$ then V_0 becomes zero. It also makes $V_f = 0$. Thus, output is shunt connected topology and the *emitter follower topology is series-shunt*. We expect high R_{IF} and low R_{OF}.

[*The amplifier circuit without feedback*

[*To find* A_{0L}]

Input circuit

Set $V_0 = 0$ to avoid feeding back. Being shunt an output side, setting $V_0 = 0$ makes $V_f = 0$. We can set $V_0 = 0$ by shorting the output node, i.e., put $R_E = 0$. This makes V_S appear directly across B and E.

Output circuit

As input is series topology, we must set $I_i = 0$ to avoid feedback voltage reach input, i.e., make $R_S = \infty$. Then seen from output side, R_E appears in the output loop.

Doing so, Fig. 11.31 is drawn corresponding to emitter follower 'without feedback'. The voltages V_0 and V_f are shown with signs consistent with Fig. 11.30.

Figure 11.32 is equivalent of Fig. 11.31 replacing the active device BJT by its ac model. In Figs. 11.32, we have

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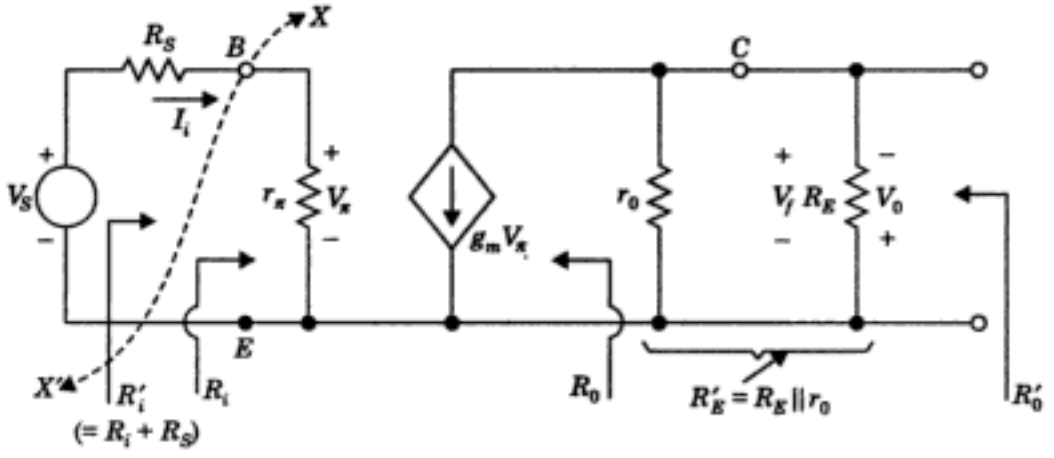


Fig. 11.32 The equivalent circuit of circuit in Fig. 11.31 when the BJT is replaced by its ac model.

$$V_f = -V_0 \quad \therefore \quad \beta = \frac{V_f}{V_0} = -1$$

$$V_0 = g_m V_\pi \,.\, R_E' \quad (\text{where } R_E' = r_0 \| R_E)$$

$$V_\pi = \frac{V_S}{R_S + r_\pi} \times r_\pi$$

$\therefore$ $$V_0 = g_m R_E' \,.\, \frac{V_S r_\pi}{R_S + r_\pi}$$

and $$A_{0L} = \frac{V_0}{V_S} = \frac{(g_m r_\pi) R_E'}{R_S + r_\pi}$$

$$T = -\beta A_{0L} = -(-1) A_{0L} = \frac{\beta_0 R_E'}{R_S + r_\pi} \qquad (\because\ g_m r_\pi = \beta_0 \text{ and } \beta = -1)$$

Thus, $$A_F = \frac{A_{0L}}{1 + T} = \frac{\beta_0 R_E' / (R_S + r_\pi)}{1 + \beta_0 R_E' / (R_S + r_\pi)}$$

or $$A_F = \frac{\beta_0 R_E'}{R_S + r_\pi + \beta_0 R_E'} \quad \textbf{Ans.} \tag{i}$$

If $R_E << r_0$ then $R_E' = R_E \| r_0 \approx R_E$, and we get

$$A_F = \frac{\beta_0 R_E}{R_S + r_\pi + \beta_0 R_E}$$

Note that for common-emitter, we had obtained

$$A_V = \frac{(\beta_0 + 1) R_E}{R_S + r_\pi + (\beta_0 + 1) R_E} \tag{ii}$$

which, for $\beta_0 >> 1$ is equal to $\dfrac{\beta_0 R_E}{(R_S + r_\pi + \beta_0 R_E)}$

The *slight difference in the two results (i) and (ii) is attributed to neglecting the forward transmission of the feedback network,* i.e., (ii) is exact and (i) is almost correct.

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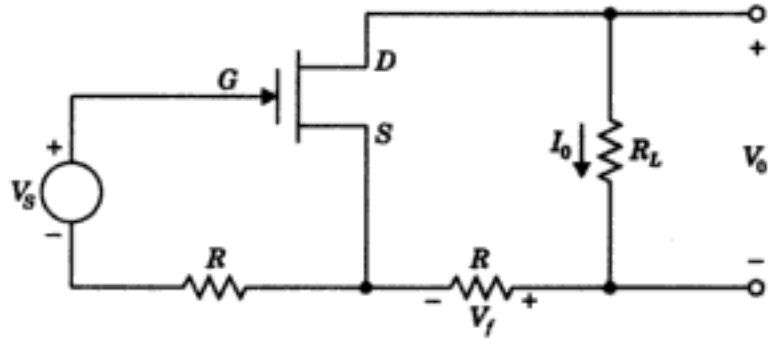


Fig. 11.37 The amplifier without feedback but including the loading of R.

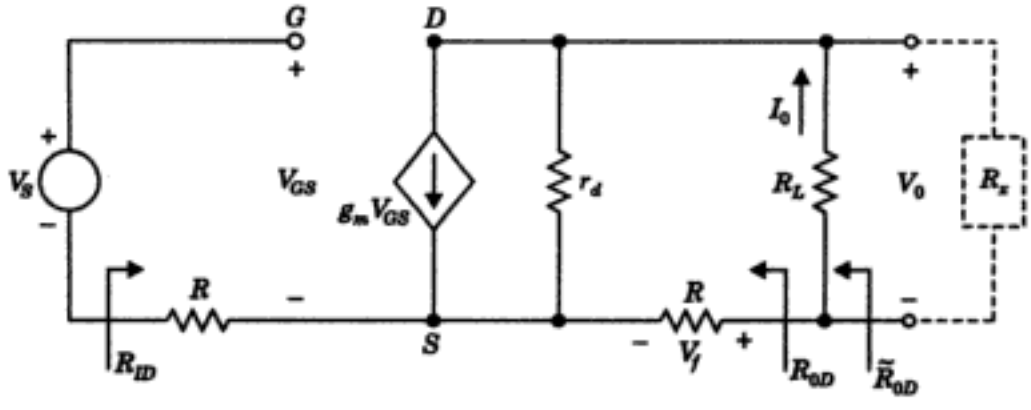


Fig. 11.38 The FET replaced by its small-signal low frequency model.

Figure 11.38 is the small-signal model of Fig. 11.37. The current $g_m V_{GS}$ divides in two parallel links: r_d and $(R + R_L)$. Thus we can write $I_0 = (g_m V_{GS})\ .\ r_d/(r_d + R_L + R)$

$$\therefore \quad A_{0L} = \frac{I_0}{V_S} = \frac{g_m r_d}{r_d + R_L + R} = \frac{\mu}{r_d + R_L + R} \qquad (\because\ g_m r_d = \mu) \tag{i}$$

$$\beta = \frac{V_f}{I_0} = -R \tag{ii}$$

$$T = -\beta A_{0L} = \frac{\mu R}{r_d + R_L + R} \tag{iii}$$

$$1 + T = 1 + \frac{\mu R}{r_d + R_L + R} = \frac{r_d + R_L + (1+\mu)R}{r_d + R_L + R} \tag{iv}$$

$$A_F = \frac{A_{0L}}{1+T} = \frac{\mu/(r_d + R_L + R)}{(r_d + R_L + (1+\mu)R)/(r_d + R_L + R)}$$

$$\therefore \quad A_F = \frac{\mu}{r_d + R_L + (1+\mu)R} \tag{v}$$

R_{ID}, $R_{IF} = \infty$ both

If R_L is considered as an external load then

$$T_{SC} = T\big|_{R_L = 0} = \frac{\mu R}{r_d + R_L + R}\bigg|_{R_L = 0} = \frac{\mu R}{r_d + R}$$

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$$T_{OC} = T\big|_{R_L=\infty} = \frac{\mu R}{r_d + R_L + R}\bigg|_{R_L=\infty} = 0$$

$$R_{0D} = r_d + R$$

$$\therefore \quad R_{0F} = R_{0D}\frac{1+T_{SC}}{1+T_{OC}} = (r_d + R)\frac{1+\dfrac{\mu R}{r_d+R}}{1+0}$$

$$\therefore \quad R_{0F} = r_d + (1+\mu)R \tag{vi}$$

If R_L is a part of output impedance then feedback impedance

$$\tilde{R}_{0F} = R_{0F} \,||\, R_L = \frac{R_L[r_d + (1+\mu)R]}{R_L + r_d + (1+\mu)R} \tag{vii}$$

Or directly (assuming a resistance R_x placed parallel to R_L on RHS in Fig. 11.38)

$$\tilde{R}_{0F} = \tilde{R}_{0D}\frac{(1+T_{Rx=0})}{(1+T_{Rx=\infty})}, \quad \tilde{R}_{OD} = R_L \,||\, (r_d + R)$$

$$= \frac{[(r_d+R)\,||\,R_L]\left[1+\dfrac{\mu R}{r_d+R'_L+R}\right]\Bigg|_{Rx=0}}{\left[1+\dfrac{\mu R}{r_d+R'_L+R}\right]\Bigg|_{Rx=\infty}}, \quad \text{where } R'_L = R_L \,||\, R_x$$

$$= \frac{\left[\dfrac{(r_d+R)R_L}{r_d+R+R_L}\right]\left[1+\dfrac{\mu R}{r_d+R}\right]}{1+\dfrac{\mu R}{r_d+R_L+R}} = \frac{R_L[r_d+(1+\mu)R]}{r_d+(1+\mu)R+R_L} \quad \text{[as found in (vii)]}$$

EXAMPLE 11.11

In the circuit shown in Fig. 11.39, Q_1 and Q_2 are identical transistors having $r_\pi = 1$ kΩ and $g_m = 0.1$ Ω.

(a) Which amplifier type does this circuit approximate?

(b) Determine the input and output resistances and the transfer ratio of the amplifier.

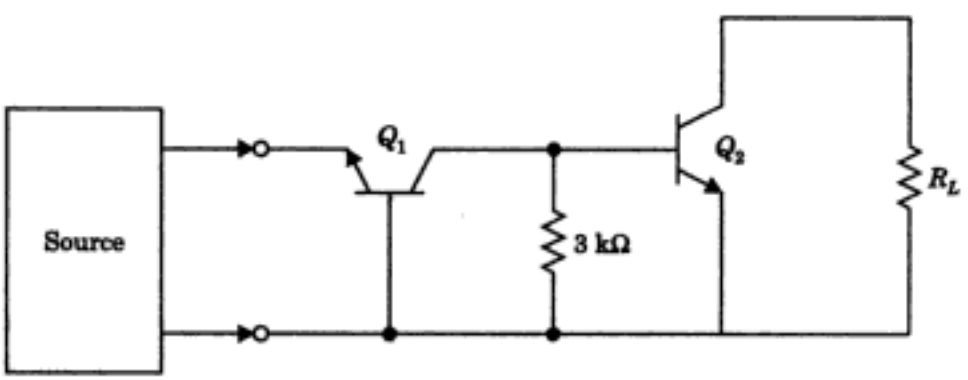


Fig. 11.39 The given circuit, Ex. 11.11.

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Solution (a) It is a CB-CE cascade, configuration. It has low input and high output impedance and hence corresponds to a current amplifier.

(b) The low frequency equivalent circuit is shown in Fig. 11.40.

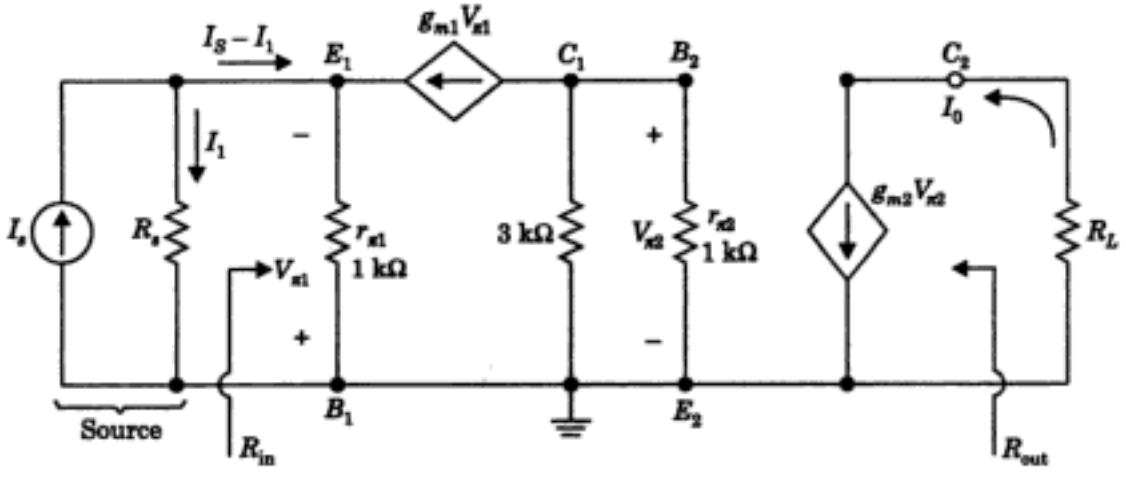


Fig. 11.40 The low frequency equivalent circuit.

$$\beta_0 = g_m r_\pi = 0.1 \times 1000 = 100$$

$$R_{in} = \frac{r_\pi}{1+\beta_0} \quad \text{(for a CB case)}$$

$$= \frac{1000}{1+100} \approx 10\,\Omega \quad \textbf{Ans.}$$

$$R_{out} = r_0 \text{ of } Q_2 \to \infty \quad \textbf{Ans.}$$

To find $A_i \triangleq \dfrac{I_0}{I_S}$

$$V_{\pi1} = -I_1 R_S$$

$$= -\left(I_S \times \frac{R_{in}}{R_S + R_{in}}\right) R_S \approx -I_S \frac{R_{in} R_S}{R_S} = -I_S R_{in}$$

$$(\because R_{in} << R_S)$$

$$V_{\pi2} = (-g_{m1} V_{\pi1})(3\ \text{k}\Omega \,||\, 1\ \text{k}\Omega)$$

$$= -g_{m1}(-I_S R_{in}) \times \frac{3000 \times 1000}{3000 + 1000} = +g_{m1} I_S R_{in} \times 750$$

$$I_0 = g_{m2} V_{\pi2} = g_{m2}(g_{m1} I_S R_{in} \times 750)$$

$\therefore$

$$\frac{I_0}{I_S} = g_{m1} g_{m2} \times R_{in} \times 750$$

$$= 0.1 \times 0.1 \times 10 \times 750 = 75$$

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or $v_i = -200(v_s - v_f)$, i.e., gives v_i as a function of v_s and v_f **Ans.**

(b) Given $v_0 = -4000 v_i$ (due to inverting amplifier)

$\therefore$ $v_0 = (-4000)[-200(v_s - v_f)]$

or $v_0 = 8 \times 10^5 \left(v_s - \frac{v_0}{300}\right) \quad \left(\because v_f = \frac{v_0}{300} \text{ (given)}\right)$

$\therefore$ $v_0 \left[1 + \frac{8 \times 10^5}{300}\right] = +8 \times 10^5 v_s$

or $\frac{v_0}{v_s} = 300$ **Ans.**

EXAMPLE 11.13

In the circuit shown in Fig. 11.42, Q_1 and Q_2 are identical transistors having $r_\pi = 1$ kΩ and $g_m = 0.1$ ℧.

(a) Which amplifier type does this circuit approximate.?

(b) Determine the input and output resistances and find the transfer ratio of the amplifier.

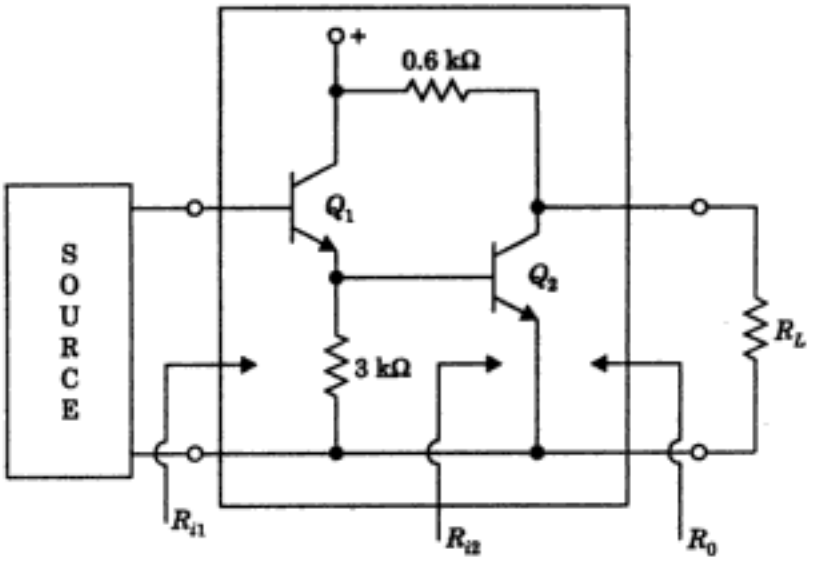


Fig. 11.42 The given circuit, Ex. 11.13.

Solution: (a) Q_1 is common collector and Q_2 is common emitter stage. Hence the given circuit is cascade of CC and CE stages. As the R_{in} of a CC is high and the R_0 of the CE is low, therefore, the given circuit approximates a voltage amplifier. If R_L is chosen a low resistance, the amplifier can be considered a voltage-to-current converter.

(b) $\beta_0 = g_m r_\pi = 0.1 \times 1000 = 100$

$R_{i1} = r_{\pi 1} + (1 + \beta_0)(R_{E1} \| R_{i2})$ (Input resistance of a CC)

$R_{i2} = r_{\pi 2} = 1$ kΩ $\quad \therefore \quad R_{E1} \| R_{12} = 3\,\text{k}\Omega \| 1\,\text{k}\Omega = \frac{3}{4}\,\text{k}\Omega$

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$$\therefore \quad R_{i1} = 1 + (1+100)\left(\frac{3}{4}\right) = 76.75\ \text{k}\Omega$$

$$R_0 = R_{C2} \| r_0 = 0.6\ \text{k}\Omega \text{ as } r_0 = \infty \text{ here.}$$

$$A_{V1}(CC) = \frac{(1+\beta_0)R_{E1}}{r_{\pi 1} + (1+\beta_0)R_{E1}} = \frac{(1+100)\times 3}{1+(1+100)\times 3} = \frac{303}{304} = 0.9967$$

$$R_{01} = R_E \| \frac{r_{\pi 1}}{1+\beta_0} = 3\ \text{k}\Omega \| \frac{1}{101} = 0.00986\ \text{k}\Omega \equiv R_S \text{ for second stage}$$

$$\therefore \quad A_{V2} = -\frac{\beta_0 R_{C2}}{R_S + r_{\pi 2}} = -\frac{100\times 0.6}{0.00986+1} = -59.4$$

$$A_V = A_{V1} \,.\, A_{V2} = 0.9967 \times (-59.4) = -59.218 \quad \textbf{Ans.}$$

EXAMPLE 11.14

(a) For the circuit shown in Fig. 11.43, determine A_{0L}, T, β and A_F. Use the approximate analysis.

(b) What is the feedback topology employed?

(c) Obtain R_{1F} and R_{0F}.

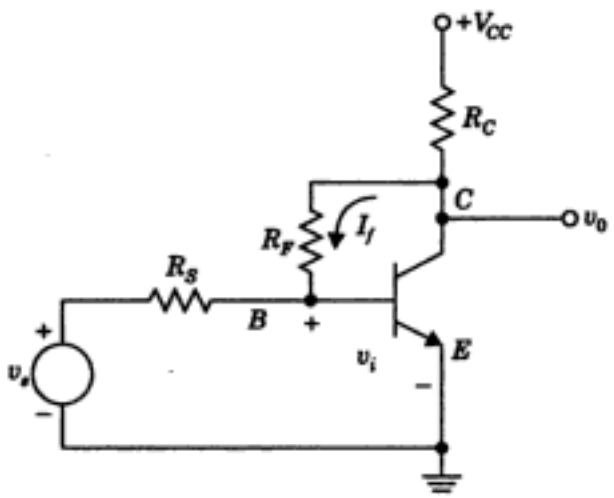


Fig. 11.43 The given circuit (shunt-shunt configuration), Ex. 11.14.

Solution: (b) This is *shunt-shunt* topoplogy.

(a) To draw equivalent circuit without feedback [shown in Fig. (11.44)].

To draw input circuit: Short circuit V_0, i.e., make $V_0 = 0$ (by making $R_C \to 0$). Therefore, R_F appears across B and E

To draw output circuit: Short circuit V_i, i.e., make $V_i = 0$. (by making $R_S \to 0$)

R_F appears across R_C

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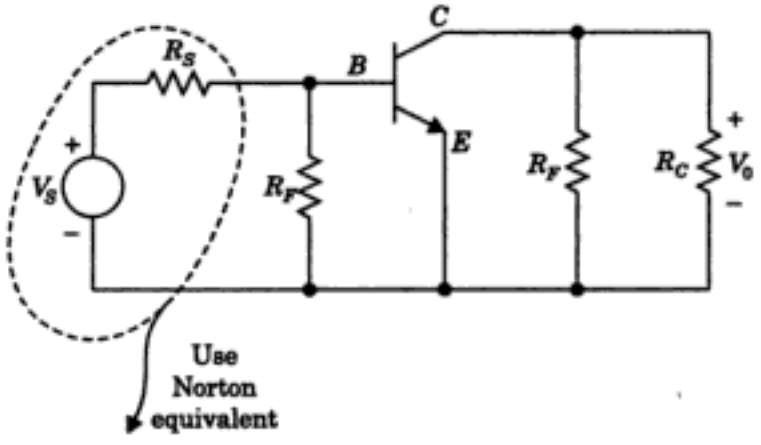


Fig. 11.44 Equivalent circuit without feedback but including loading due to R_F.

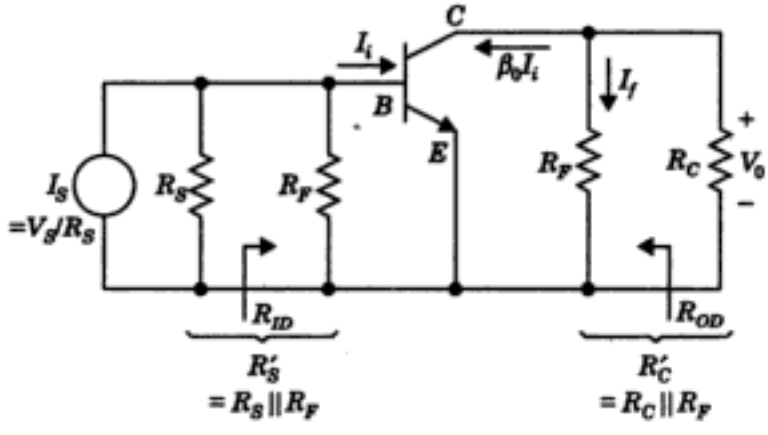


Fig. 11.45 After converting voltage source to current source, by using Norton's equivalent.

The circuit in Fig. 11.44 is redrawn in Fig. 11.45 by replacing V_S and R_S (in Fig. 11.44) by a Norton equivalent.

Assume $r_b = 0,\ r_0 = \infty$ (Early effect impedance)

$$A_{0L} = \frac{V_0}{I_S} = (-\beta_0 I_i) R_C'$$

$$= -\beta_0 \frac{R_S'}{R_S' + r_\pi} . R_C' \qquad \left(\because\ I_i = \frac{I_S . R_S'}{R_S' + r_\pi} \right)$$

$$= -\beta_0 \frac{R_S R_F / (R_S + R_F)}{R_S R_F / (R_S + R_F) + r_\pi} . \frac{R_C R_F}{R_C + R_F}$$

$$= -\beta_0 \frac{R_S R_F}{R_S R_F + r_\pi (R_S + R_F)} . \frac{R_C R_F}{(R_C + R_F)} \quad \textbf{Ans.}$$

$$\beta = \frac{I_f}{V_0} = \frac{1}{R_F} \quad \textbf{Ans.}$$

$$T = -\beta A_{0L} = \left(-\frac{1}{R_F} \right) A_{0L} = \frac{\beta_0 R_C R_S R_F}{(R_C + R_F)(R_S R_F + r_\pi (R_S + R_F))} \quad \textbf{Ans.}$$

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$$T_{SC} = T\Big|_{\substack{R_C \to 0 \\ \therefore R_L \to 0}} = 0$$

$$R_{0F} = \frac{R_{0D}}{(1 + T_{0C})} = \frac{(R_F \,||\, r_0)}{\left(1 + \dfrac{\beta_0 r_0 R_S R_F}{(r_0 + R_F)[R_S R_F + r_\pi (R_S + R_F)]}\right)}$$ **Ans.**

EXAMPLE 11.15

For the circuit shown in Fig. 11.46, determine the small signal gain V_0/V_s, the input resistance R'_{1F} and the output resistance R'_{0F}. Assume $\beta = 100$ and $r_\pi = 1$ kΩ for the transistor. (Assume $I_{CQ} = 2.5$ mA and $V_T = 25$ mV)

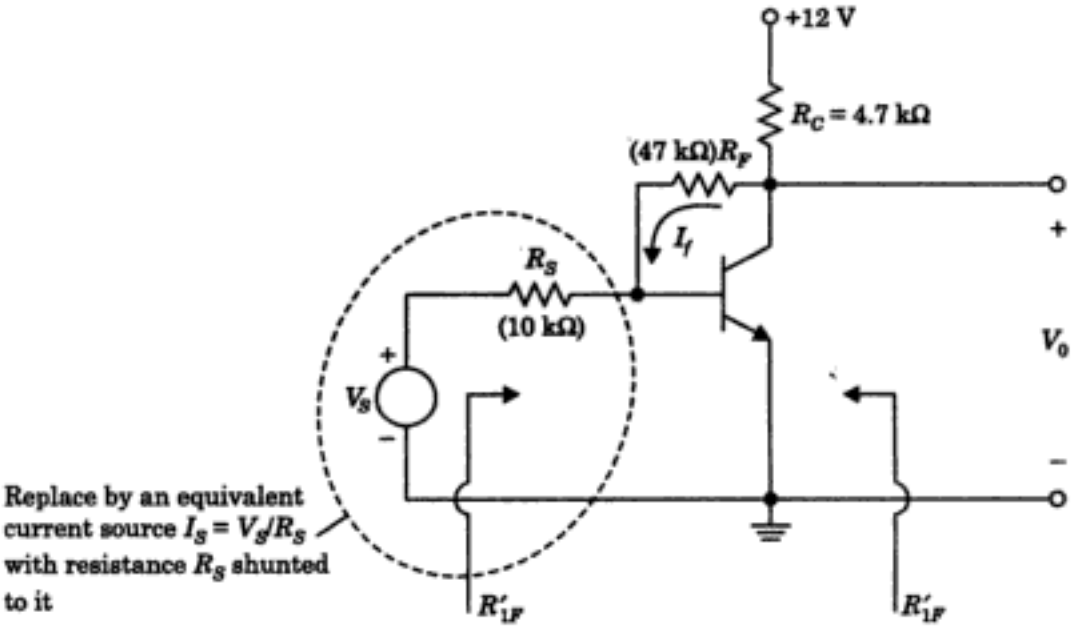


Fig. 11.46 The given circuit, Ex. 11.15.

Solution: As $I_{CQ} = 2.5$ mA and $V_T = 25$ mV $\therefore$ $g_m = 2.5/25 = 1/10$℧. $r_\pi = \beta/g_m = \dfrac{100}{(1/10)}$ = 1000 Ω. Being a –ve feedback with shunt-shunt topology, we first change signal source V_S to I_S by using Norton's equivalent.

Then

$$A_{0L} \triangleq \frac{V_0}{I_S},$$

where

$$I_S = \frac{V_S}{R_S}$$

Amplifier without feedback (to find A_{0L}) is shown in Fig. 11.47. (Use procedure as in Example 11.14)

$$V_0 = (-g_m v_\pi)(R_F \,||\, R_C)$$

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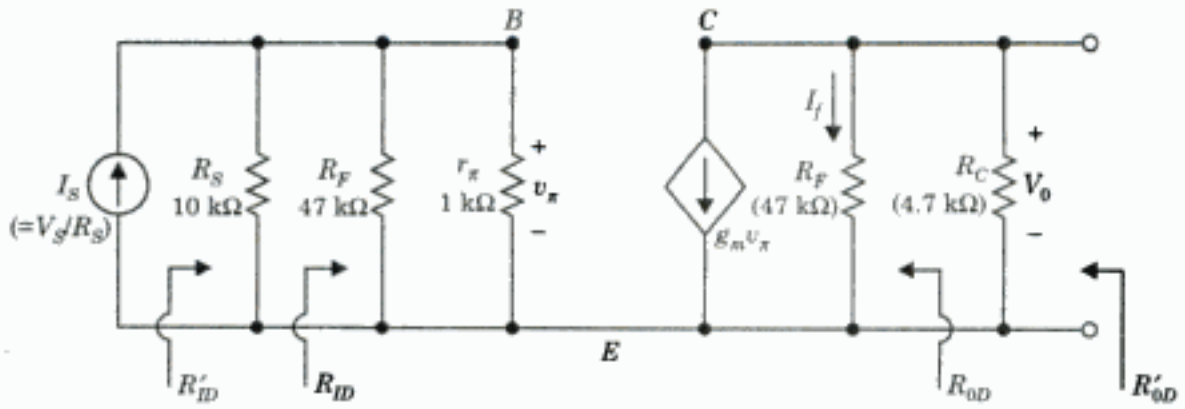


Fig. 11.47 ac model of Fig. 11.46 drawn without feedback but taking loading due R_F, R_S and R_L (Here $R_L = R_C$).

$$\therefore \quad \frac{V_0}{I_S} = -g_m(R_F \,\|\, R_C)(R_S \,\|\, R_F \,\|\, r_\pi)$$

$$[\because \; v_\pi = I_S(R_S \,\|\, R_F \,\|\, r_\pi)]$$

$$= -100(47 \,\|\, 4.7)(10 \,\|\, 47 \,\|\, 1) \quad \left(\because \; g_m = \frac{1}{10}\,\text{℧} = 100\ \text{m℧}\right)$$

$$= -100(4.27)(0.89) = -380.88 \times 10^3$$

and $$A_{0L} = -380.88 \times 10^3\ \Omega$$

Now, $$\beta = \frac{I_f}{V_0} = \frac{1}{R_F}$$

$$= \frac{1}{47 \times 10^3} = 0.02127 \times 10^{-3}$$

$$T = -\beta A_{0L}$$

$$= -(0.02127 \times 10^{-3})(-380.88 \times 10^3) = 8.102$$

With feedback, $$A_F = \frac{A_{0L}}{1 + T}$$

$$= \frac{-380.88 \times 10^3}{1 + 8.102} = -41.84 \times 10^3\ \Omega$$

$$A_{VF} = \frac{V_0}{V_S} = \frac{V_0}{I_S} \times \frac{I_S}{V_S} \qquad \left(\text{Take } I_S/V_S = \frac{1}{R_S}\right)$$

$$= (-41.84 \times 10^3) \times \frac{1}{10 \times 10^3} = -4.184 \quad \textbf{Ans.}$$

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Thus, we have found

$$A_{0L} = -380.88 \times 10^3\ \Omega \left(\text{i.e. } \frac{V_0}{I_S}\right);\quad A_F = -41.84 \times 10^3\ \Omega \left(\frac{V_0}{I_S}\right)$$

$$\beta = 0.02127 \times 10^{-3}\ \mho; \qquad A_F = -4.184 \left(\frac{V_0}{V_S}\right)$$

$$T = 8.102$$

R_{IF} seen by **current or voltage source** = 0.0986 kΩ

$$R'_{IF}\big|_{I_S} = 0.0978\ \text{k}\Omega;\quad R'_{0F} = 0.469\ \text{k}\Omega$$

$$R'_{IF}\big|_{V_S} = 10.0986\ \text{k}\Omega;\quad R_{0F} = 0.521\ \text{k}\Omega.$$

Ans.

EXAMPLE 11.16

In the amplifier circuit shown in Fig. 11.49, the transistors have $\beta_0 = 150$ and $I_{CQ} = 1.5$ mA each. Determine (i) A_F and T, (ii) R_{1F} and R_{0F}.

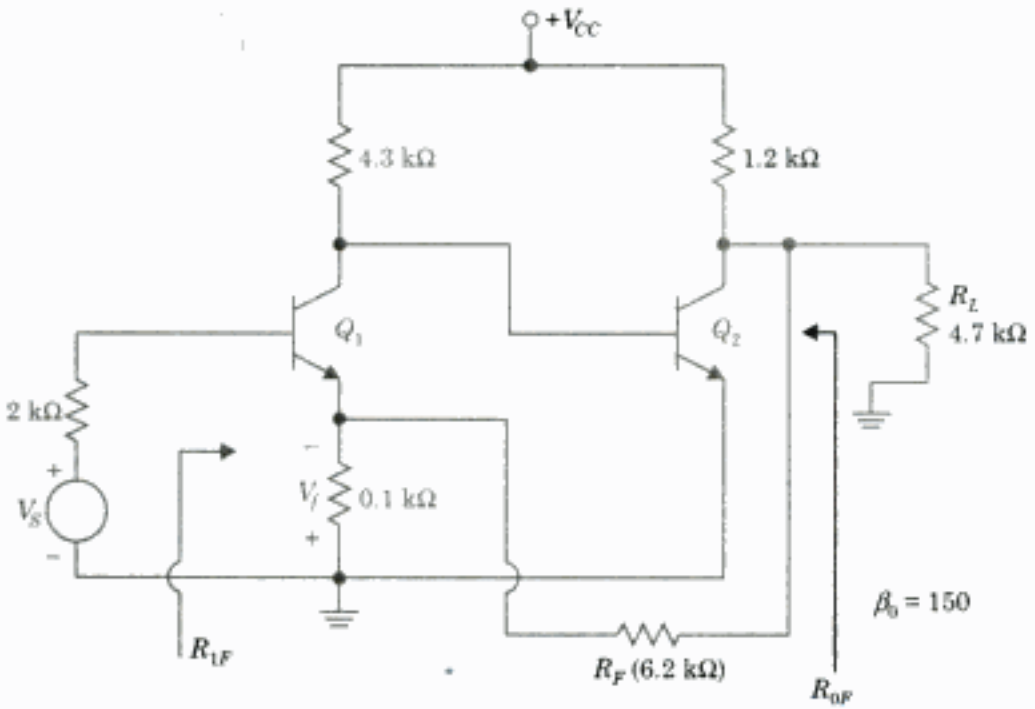


Fig. 11.49 The given circuit, Ex. 11.16.

Solution: *Series-shunt topology*

The amplifier without feedback but taking loading effect is depicted in Fig. 11.50.

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1.5}{25} = 60\ \text{m}\mho$$

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$$= 19.298(1 + 9.71) = 206.68 \text{ k}\Omega$$

$$\therefore \quad R_{IF} = R'_{IF} - R_S$$

$$= 206.68 - 2.0 = 204.68 \text{ k}\Omega \quad \textbf{Ans.}$$

Output side (Directly)

$$R'_{0D} = R_{0D} \| R_L$$

$$= 1.008 \text{ k}\Omega \| 4.7 \text{ k}\Omega = 830 \ \Omega$$

$$(\because R_{OD} = 1.2 \| (6.2 + 0.1) \text{ K} = 1.008 \text{ k}\Omega)$$

$$R'_{0F} = \frac{830}{(1+T)} = \frac{830}{(1+9.71)} = 77.5 \ \Omega$$

(being series-shunt topology i.e., shunt on output side)

$$\therefore \quad R_{0F} = \frac{77.5 \times 4700}{4700 - 77.5} = 78.79 \ \Omega \quad \textbf{Ans.}$$

EXAMPLE 11.17

(a) For the circuit shown in Fig. 11.51, determine T, A_{0L} and A_F.

(b) Evaluate R_{0F}. The MOSFETs have g_m = 1 mΩ, r_d = 20 kΩ.

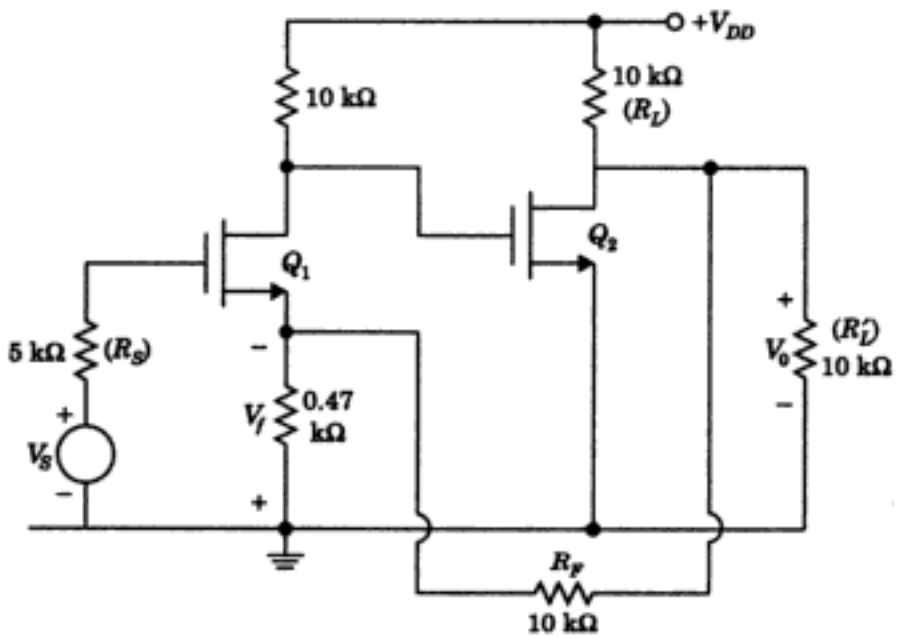


Fig. 11.51 The given circuit, Ex. 11.17.

Solution: This is a *series-shunt* connection. The equivalent circuit, without feedback but taking loading effect is as shown in Fig. 11.52.

Input circuit: Short circuit R_L.

$$\therefore \quad V_0 = 0 \text{ and } R_F \text{ appears } \| \text{ to } 0.47 \text{ k}\Omega$$

Output circuit: Open the input, i.e., make $R_S = \infty$, therefore, (0.47 kΩ + R_F) appears in parallel to R_L as shown. Figure 11.53 shown the ac equivalent circuit of Fig. 11.52.

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Then $$r_{01} = \frac{V_{A1}}{I_{CQ1}} = \frac{125}{0.25} = 500\ \text{k}\Omega$$

and $$r_{02} = \infty\ \Omega \quad \text{as} \quad V_{A2} = \infty$$

Now, $$\beta = \frac{I_f}{I_0} = \frac{I_f}{I_E} = -\frac{0.82}{20 + 0.82} = -0.0394$$

($\because$ $I_0 = I_E$ and I_E is the net current thro' parallel resistors 20 kΩ and 0.82 kΩ)

$\therefore$ $$A_I\big|_{\text{No feedback}} = \frac{I_0}{I_S} = \frac{I_0}{I_{b2}} \frac{I_{b2}}{I_{C1}} \frac{I_{C1}}{I_{b1}} \frac{I_{b1}}{I_S}$$

In Fig. 11.56, we observe that (assuming $r_{01} = \infty$)

$$\frac{I_0}{I_{b2}} = \beta_2 = 150; \quad \frac{I_{C1}}{I_{b1}} = \beta_1 = 200;$$

$$\frac{I_{b2}}{I_{C1}} = \frac{R_{C1}}{R_{C1} + R_{\text{in}2}} = \frac{R_{C1}}{R_{C1} + [r_{\pi 2} + (1 + \beta_2)(20 \,\|\, 0.82)]} = \frac{20}{20 + [7.5 + (1 + 150)(20 \,\|\, 0.82)]}$$

$$\frac{I_{b1}}{I_S} = \frac{(R_S \,\|\, 20.82)}{r_{\pi 1} + (R_S \,\|\, 20.82)} = \frac{(1) \,\|\, (20.82)}{20 + (1 \,\|\, 20.82)} = \frac{0.954}{20 + 0.954}$$

$\therefore$ $$A_I\big|_{\text{No feedback}} = (150)\frac{20}{20 + 126.4}(200) \cdot \frac{0.954}{20 + 0.954} = 186.59$$

If $r_{01} = 500$ kΩ for Q_1 is also taken into account, R_{C1} gets modified to $R_{L1} = R_{C1} \,\|\, r_{01} = 20\ \text{k}\Omega \,\|\, 500 = 19.2$ kΩ. Then

$$A_I\big|_{\text{No feedback}} = (150)\frac{19.2}{19.2 + 126.4}(200)\frac{0.954}{20 + 0.954} = 180.11 = A_{0L} \quad \textbf{Ans.}$$

(so small difference)

$$T = -\beta A_{0L}$$
$$= -(-0.0394)(180.11) = 7.096 \approx 7.1 \quad \textbf{Ans.}$$

$$A_F = \frac{A_{0L}}{1 + T} = \frac{180.11}{1 + 7.1} = 22.36 \quad \textbf{Ans.}$$

Thus, $$A_{IF} = 22.36 \quad \textbf{Ans.}$$

$$A_{VF} = A_{IF} \cdot \frac{R_L}{R_S} = (22.36)\frac{5.6}{1} = 124.5 \quad \textbf{Ans.}$$

To find R_{IF}

$$\tilde{R}_{ID} = R_S \,\|\, R_{ID} = 1\ \text{k}\Omega \,\|\, (20 + 0.82) \,\|\, 20\ \text{k}\Omega = 1\ \text{k}\Omega \,\|\, 10.2 = 0.9107\ \text{k}\Omega$$

$$\tilde{R}_{IF} = \frac{\tilde{R}_{ID}}{(1 + T)} = \frac{0.9107}{(1 + 7.1)} = 0.1124\ \text{k}\Omega$$

$$R_{IF} = \frac{\tilde{R}_{IF} \times R_S}{R_S - \tilde{R}_{IF}} = \frac{0.1124 \times 1}{1 - 0.1124} = 0.126\ \text{k}\Omega = 126\ \Omega \quad \textbf{Ans.}$$

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EXAMPLE 11.19

In the two-stage feedback amplifier shown in Fig. 11.57, the transistors are identical and have the following parameters:

$$\beta_0 \text{ (or } h_{fe}) = 50,\ r_\pi \text{ (or } h_{ie}) = 2\ \text{k}\Omega,\ r_0 \left(\text{or } \frac{1}{h_{oe}}\right) = \infty \text{ and } h_{re} = 0$$

Calculate: (a) $A_{IF} = \frac{I_0}{I_S}$; (b) $R_{1F} = \frac{V_i}{I_S}$; (c) $A'_{1F} = \frac{I_0}{I'_i}$; (d) $A_{VF} = \frac{V_0}{V_S}$ where $V_S = I_S R_S$.

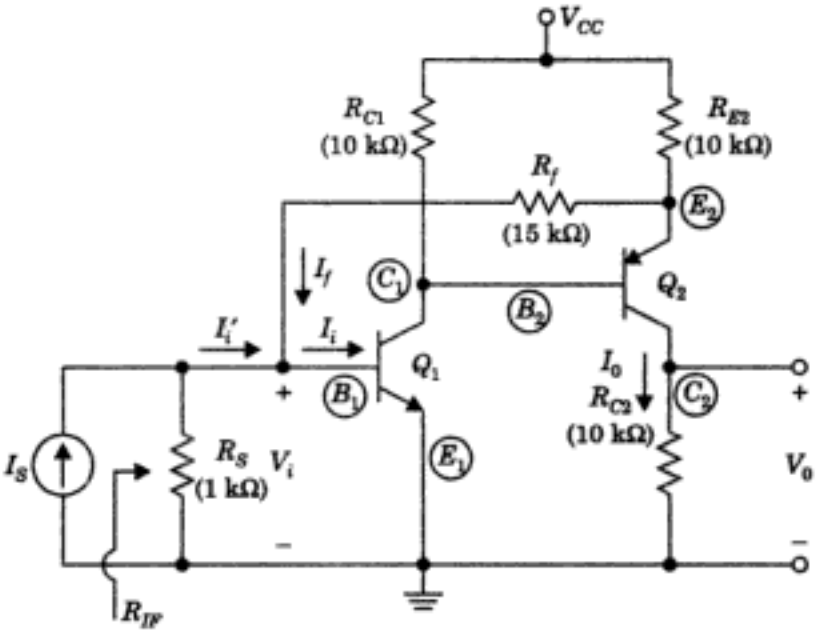


Fig. 11.57 The given feedback circuit, Ex. 11.19.

Solution: Input side is clearly current missing and, therefore, shunt-topology. On the output side in Fig. 11.57, if we short R_{C2} to make $V_0 = 0$, the potential at the emitter of Q_2 *does not become zero.* The feedback current I_f continues. Hence output sensing is not of V_0 but of I_0 i.e. series-topology. Clearly, this is the case of *shunt-series* feedback topology. Figure 11.58 shows an equivalent circuit without feedback but taking loading effect into account.

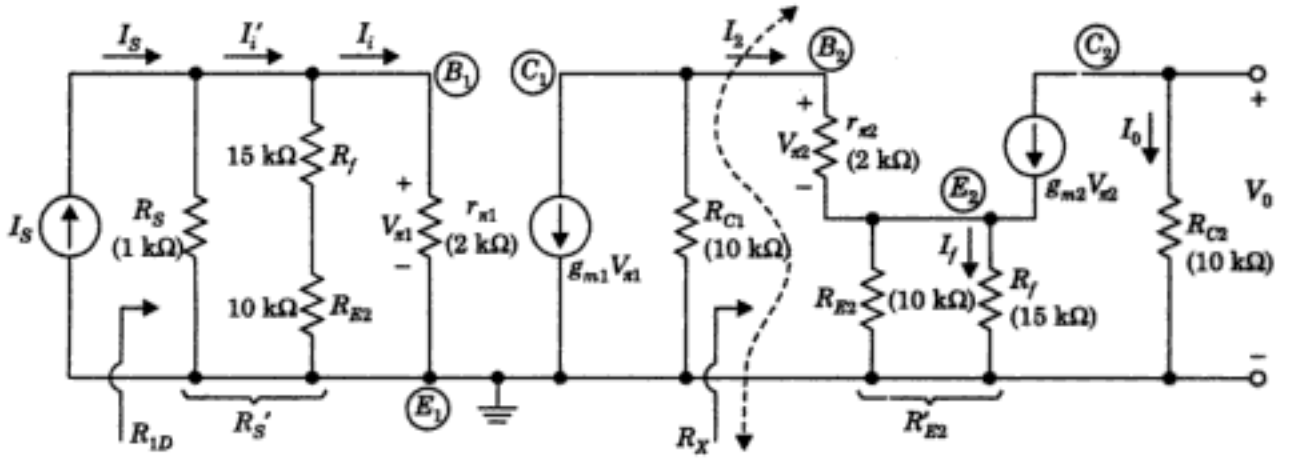


Fig. 11.58 The equivalent circuit without feedback but taking loading effect.

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Input circuit:

Make $R_{C2} = \infty$ i.e. open circuit $\therefore$ $(R_f + R_{E2})$ appears across B_1 and earth, i.e. parallel to R_S.

Output circuit:

Short the shunt, i.e., make $R_S = 0$ $\therefore$ R_f appears in parallel with R_{E2}.

Here, define

$$R'_S = R_S \,||\, (R_f + R_{E2})$$

$$= 1\ \text{k}\Omega \,||\, (15 + 10\ \text{k}\Omega) = \frac{1 \times 25}{1 + 25} = \frac{25}{26}\ \text{k}\Omega$$

$$V_{\pi 1} = (2) \times I_S \times \frac{25/26}{2 + 25/26} = \frac{2 \times 25}{77} I_S = \frac{50}{77} I_S$$

Also $$g_{m1} = g_{m2} = \frac{\beta_0}{r_\pi} = \frac{50}{2} = 25\ \text{m}\mho$$

$$g_{m1} V_{\pi 1} = 25 \times \frac{50}{77} I_S = \frac{1250 I_S}{77}$$

$$Z_x = R_x = r_{\pi 2} + (1 + \beta_{02}) R'_{E2}$$

where $$R'_{E2} = R_{E2} \,||\, R_f$$

$$= 10\ \text{k}\Omega \,||\, 15\ \text{k}\Omega = \frac{10 \times 15}{(10 + 15)} = 6\ \text{k}\Omega$$

$\therefore$ $$R_x = 2 + (1 + 50) \times 6 = 308\ \text{k}\Omega$$

$$I_2 = (-g_{m1} V_{\pi 1}) \times \frac{R_{C1}}{R_{C1} + R_X}$$

$$= \left(-\frac{1250 I_S}{77}\right) \times \frac{10}{10 + 308} = (-I_S) \frac{1250 \times 5}{77 \times 159} = (-I_S) \frac{6250}{77 \times 159}$$

$$I_0 = (-\beta_{02} I_2) = (-50)(-I_S) \frac{6250}{77 \times 159} = 25.52 I_S$$

$\therefore$ $$\frac{I_0}{I_S} = A_I \big|_{\text{open loop}} = 25.52$$

Also, $$I_f = (1 + \beta_{02}) I_2 \times \frac{R_{E2}}{R_{E2} + R_f}$$

$$= (1 + 50) \left(-I_S \frac{6250}{77 \times 159}\right) \times \frac{10}{10 + 15} = -I_S \times 10.4$$

$$\beta = \frac{I_f}{I_0} = \frac{-I_S \times 10.4}{25.52 I_S} = -0.4$$

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(d) $$A_{VF} = \frac{V_0}{V_S} = \frac{I_C R_{C2}}{I_S R_S} = \left(\frac{I_C}{I_S}\bigg|_{\text{with feedback}}\right)\left(\frac{R_{C2}}{R_S}\right)$$

$$= (2.27)\frac{10}{1} = 22.7$$

$$\left(\because \frac{I_C}{I_S}\bigg|_{\text{with feedback}} = A_{IF} = 2.27 \text{ from (i)}\right)$$

or $A_{VF} = 22.7$ **Ans.**

EXAMPLE 11.20

In Fig. 11.59, transistors Q_1 and Q_2 are identical having $\beta_0 = 50$, $r_\pi = 1.1$ kΩ each. Make reasonable approximations where appropriate, and neglect the reactances of the capacitors (i.e. $C \to C_\infty$). Calculate: (a) $A_{VF} = \frac{V_0}{V_S}$, (b) $A_{IF} = \frac{I_0}{I_S}$, where $V_S = I_S R_S$, (c) R_{IF} and (d) R_{0F}.

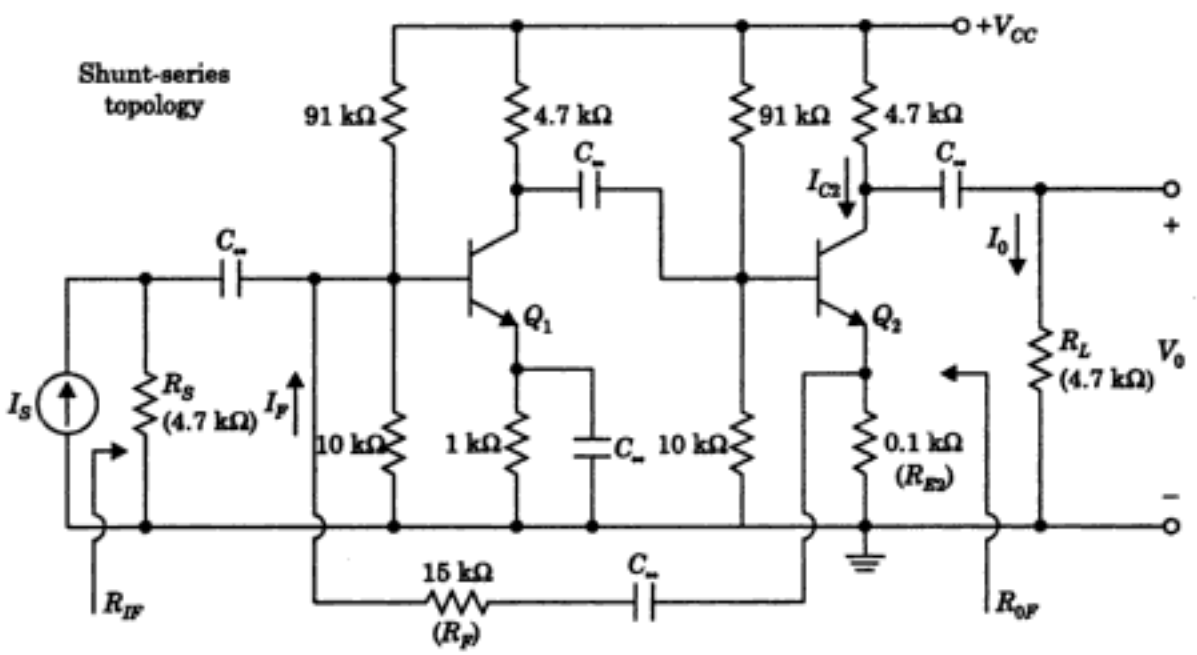


Fig. 11.59 The given circuit with negative feedback, Ex. 11.20.

Solution: This is clearly a shunt series topology. The output R_L and R_{C2} are parallel $= \frac{4.7}{2} = 2.35$ kΩ. If R'_L (= $R_L || R_{C2}$) is open circuited then the feed current I_F is zeroised (because emitter of Q_2 assumes zero potential for no current I_{C2} or I_{E2}. This is *shunt-series* topology equivalent circuit without feedback which is shown in Fig. 11.60.

Input side: When R'_L is open circuited, there is no current in R_{E2} and therefore resistance 15 kΩ (R_F) in series with 0.1 kΩ (R_{E2}) appears in parallel with R_S on the input side, as shown in Fig. 11.60.

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Output side: When R_S is shorted, the resistance 15 kΩ (R_F) appears in parallel with 0.1 kΩ (R_{E2}) on the output side in Fig. 11.60.

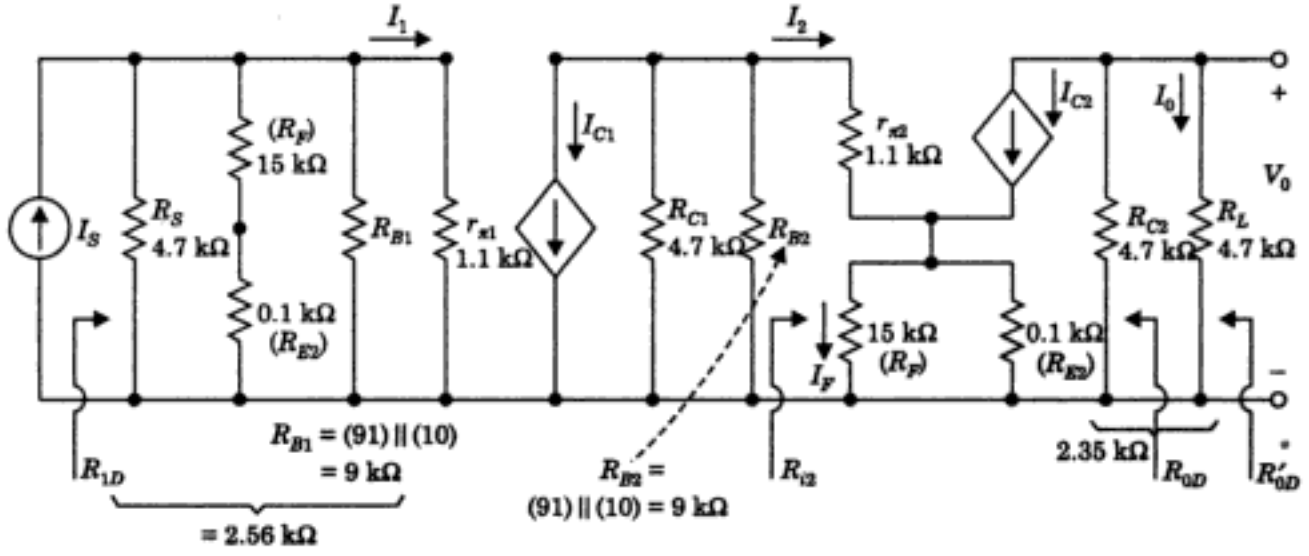


Fig. 11.60 Equivalent circuit of amplifier without feedback.

To find $\frac{V_0}{I_S}$ *with no feedback*

$$(4.7\ \text{k}\Omega) \| (15.1\ \text{k}\Omega) \| (9\ \text{k}\Omega) = 2.56\ \text{k}\Omega$$

$$\therefore \quad I_1 = I_S \times \frac{2.56}{2.56 + 1.1} = 0.6994 I_S$$

$$I_{C1} = \beta_{01} I_1 = 50(0.6994 I_S) = 34.97 I_S$$

As
$$R_{i2} = r_{x2} + (1 + \beta_0)(15\ \text{k}\Omega \| 0.1\ \text{k}\Omega)$$
$$= 1.1 + (1 + 50)(0.0993) = 6.17\ \text{k}\Omega$$

$$\therefore \quad I_2 = (-I_{C1}) \frac{R_{C1} \| R_{B2}}{(R_{C1} \| R_{B2}) + R_{i2}} = (-I_{C1}) \frac{4.7 \| 9}{(4.7 \| 9) + 6.17}$$

$$= (-34.97 I_S) \frac{3.0876}{3.0876 + 6.17} = -11.66 I_S$$

$$I_{C2} = \beta_0 I_2 = (-11.66 I_S) \times 50 = -583 I_S$$

$$v_0 = (-I_{C2})(4.7 \| 4.7) = (+ 583 I_S)(2.35) = 1370 I_S$$

Then
$$A_{ID} = \frac{I_0}{I_S} = \frac{-\frac{1}{2} I_{C2}}{I_S} = \left(-\frac{1}{2}\right) \frac{-583 I_S}{I_S} = 291.5$$

$$I_F = I_{C2} \times \frac{0.1}{15 + 0.1} = \frac{(-583 I_S)(0.1)}{15.1} = -3.86 I_S$$

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$$\frac{I_{b3}}{I_{c2}} = \frac{-R_{L2}}{(R_{L2} + R_{in3})}$$

$$= -\frac{7.075}{7.075 + 75.26} = -0.0859$$

$$\frac{I_{c2}}{I_{b2}} = \beta_0 = 200$$

$$\frac{I_{b2}}{I_{c1}} = \frac{-R_{L1}}{(R_{L1} + R_{in2})}$$

$$= -\frac{4.95}{(4.95 + 5.0)} = -0.49748$$

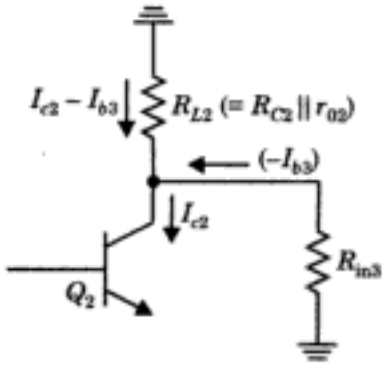


Fig. 11.62a Explaining how to calculate I_{b3}/I_{c2}.

$$\frac{I_{c1}}{I_{b1}} = \beta_0 = 200$$

$$\frac{I_{b1}}{V_S} = \frac{1}{(R_S + R_{in1})}$$

$$= \frac{1}{(0.60 + 59.8)} = 0.016556 \times 10^{-3}\ \text{℧}$$

$\therefore$ $A_{0L} = (200)(-0.0859)(200)(-0.49748)(200)(0.016556 \times 10^{-3}) = 5.6599$

Thus, $$T = -\beta A_{0L} = -\left(\frac{-R_1 R_2}{R_1 + R_2 + R_F}\right)(5.6599)$$

$$= \frac{[0.2 \times 0.33]10^6}{[0.2 + 0.33 + 20]10^3}(5.6599) = 0.01819 \times 1000 = 18.19 \quad \textbf{Ans.}$$

$$A_F = \frac{A_{0L}}{1 + T} = \frac{5.6599}{1 + 18.19} = 0.2949 \quad \textbf{Ans.}$$

(d) $$\frac{V_0}{V_S} = \frac{-I_0 R_{L3}}{V_S} = -A_F \,.\, R_{L3} = -0.2949(R_{C3} \| r_{03})$$

$$= -0.2949 \times 10^3 \frac{10 \times 250}{10 + 250}$$

$\therefore$ $$\frac{V_0}{V_S} = -2835.6 \quad \textbf{Ans.}$$

EXAMPLE 11.22

The FETs in the circuit shown in Fig. 11.63 are identical and have $g_m = 2$ m℧ and $r_d = 20$ kΩ. The circuit parameters are $R_D = 12$ kΩ, $R_G = 500$ kΩ, $R_s = 50$ Ω and $R_F = 5$ kΩ. Determine A_F and R_{0F}.

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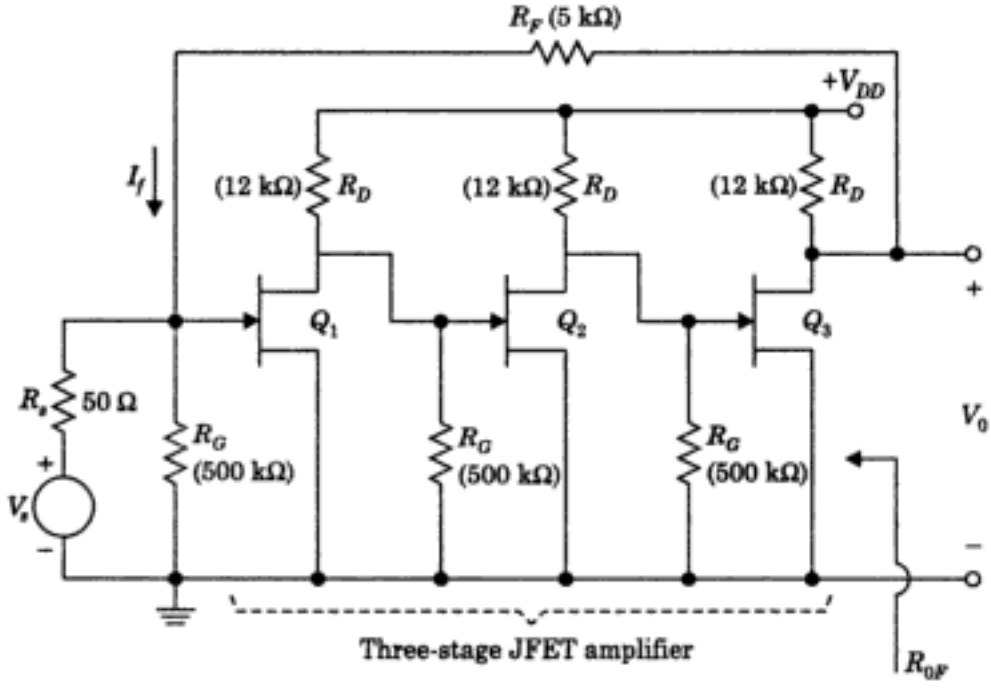


Fig. 11.63 The given circuit, Ex. 11.22.

Solution: This is *shunt-shunt* topology so we convert input V_s, R_s into $I_s = V_s/R_s$ shunted by R_s. The amplifier without feedback but taking loading effect is shown in Fig. 11.64. Input of three-stage amplifier = ∞ Ω

Output impedance of three-stage amplifier is:

$$= r_d \,||\, R_D = 20 \text{ k}\Omega \,||\, 12 \text{ k}\Omega = 7.5 \text{ k}\Omega$$

$$A_V = A_{V1}\, A_{V2}\, A_{V3}$$

where

$$A_{V1} = -g_m\,(R_D \,||\, r_d \,||\, R_G)$$
$$= -2 \times 10^{-3}\,(12 \,||\, 20 \,||\, 500) \times 10^3$$
$$= -2 \times 10^{-3}\,(7.39) \times 10^3 = -14.778$$

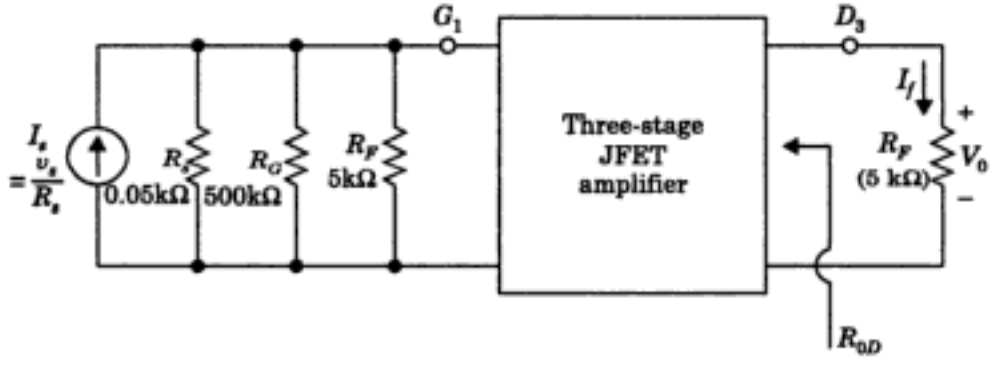


Fig. 11.64 Circuit without feedback, with loading effect, and replacing 3-stage JFET by an equivalent amplifier.

$$A_{V2} = A_{V1} = -14.778$$
(∵ Q_1, Q_2 have similar output side connections)

$$A_{V3} = -g_m\,(R_D \,||\, r_d)$$

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$$= -2 \times 10^{-3} \times 7.5 \times 10^{3} = -15$$

$$\therefore \quad A_V = (-14.778)(-14.778)(-15) = -3276$$

We can replace 3-stage amplifier as shown in Fig. 11.65.

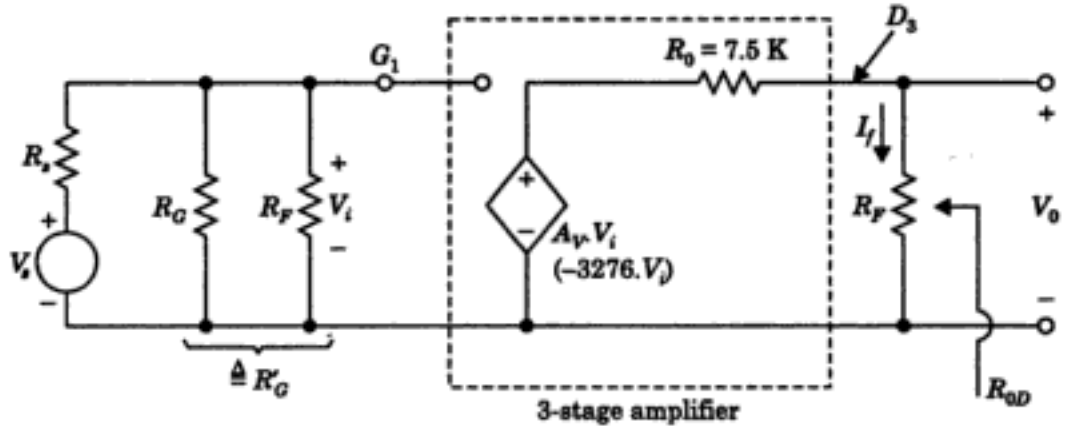


Fig. 11.65 Equivalent diagram of Fig. 11.64

To find V_0/V_s with no feedback

In Fig. 11.65,

$$V_i = \frac{V_s \times R'_G}{R_s + R'_G}, \quad R'_G = R_G \| R_F = 500\ \text{k}\Omega \| 5\ \text{k}\Omega \approx 4.95\ \text{k}\Omega$$

$$= V_s \cdot \frac{4.95}{0.05 + 4.95} = V_s \cdot \frac{4.95}{5.00} \qquad \text{(i)}$$

$$V_0 = (A_V V_i)\frac{R_F}{R_0 + R_F} = (-3276 \,.\, V_i)\frac{5}{7.5 + 5} = (-3276 V_i)\frac{5}{12.5} \qquad \text{(ii)}$$

From Eqs. (i) and (ii)

$$A_{0L}\big|_{\text{voltage gain}} = \frac{V_0}{V_s} = -3276 \times \frac{5}{12.5} \times \frac{4.95}{5.00} = -1297$$

Being shunt-shunt topology,

$$\beta = \frac{1}{R_F} = \frac{1}{5000} \qquad \left(\because\ \beta = \frac{X_f}{X_0} = \frac{I_f}{V_0} = \frac{1}{R_f}\ \text{in Figs. 11.64 and 11.65}\right)$$

$$A_{0L} = \left.\frac{V_0}{I_S}\right|_{0L} = \left.\frac{V_0}{V_s/R_s}\right|_{0L} = A_V\big|_{0L} \times R_s$$

$$= -1297 \times 50 = -64850\ (\equiv R_M)$$

$$T = -\beta R_M = -\frac{1}{5000} \times (-64850) = 12.97$$

$$A_F = \frac{A_{0L}}{1 + T} = \frac{-64850}{1 + 12.97} = -4642$$

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P11.9 Use the approximate analysis to determine A_{0L}, β, T and A_F for a Source Follower. (series-shunt case), as shown in Fig. 11.67.

$$\left(\textbf{Ans. } T = A_{0L} = g_m(r_d \,\|\, R_S),\ A_F = \frac{\mu R_S}{[r_d + (1+\mu)R_S]}\right)$$

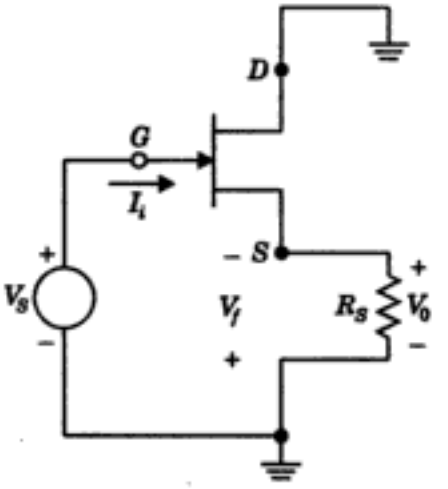


Fig. 11.67 Circuit for P11.9.

P11.10 The circuit shown in Fig. 11.68 has the following parameters: R_C = 4 kΩ, R_F = 40 kΩ, R_S = 10 kΩ, r_π = 1.1 kΩ, β_0 = 50. (a) Find A_{VF} (b) Find R_{1F} and R_{0F}.

(***Ans.*** (a) $A_{VF} = -3.2$, (b) $R_{1F} = 196.7\ \Omega$; $R_{0F} = 890\ \Omega$)

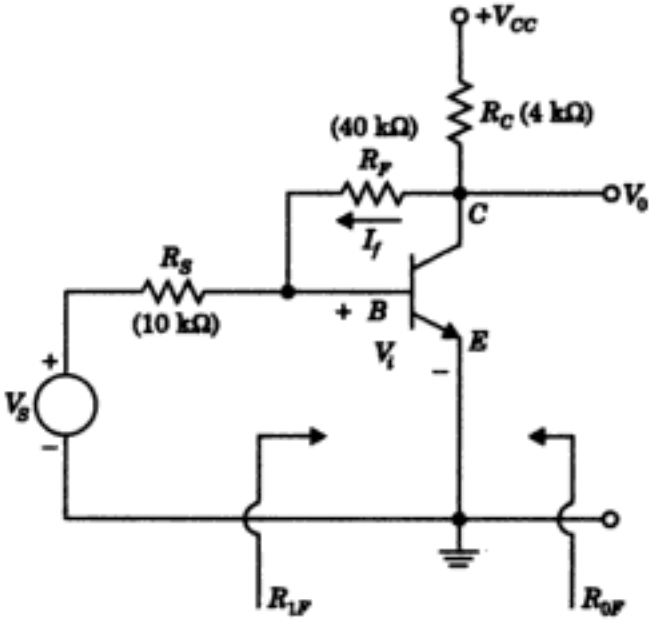


Fig. 11.68 The given circuit, for P11.10.

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CHAPTER 12 Oscillators

12.1 INTRODUCTION

An oscillator is a circuit that provides ac output signal without applying any ac input signal. Thus, it is different from an amplifier where a small ac signal is applied at the input terminals so as to obtain amplified output. The standard waveforms that can be obtained from oscillator circuits are: sinusoidal, square, triangular or pulse. These standard ac signals are required in many systems, such as computer and control systems where clock pulses are needed for timing; communication systems where sine waves are used as a carrier; in test and measurement systems where various types of waveforms are used for testing and characterization of electronic devices and circuits.

The most commonly used waveform is a sinusoidal waveform and can be obtained by using positive feedback in amplifiers. The feedback signal is used instead of an input signal. If conditions on loop gain and phase are satisfied, it is possible to obtain an output signal without any external input signal. In this chapter, we will discuss the various circuits which are used for generating sine waves.

12.2 BASIC PRINCIPLE OF SINE WAVE OSCILLATORS

The basic structure of sine wave oscillators based on the use of feedback in amplifiers is shown in Fig. 12.1. It consists of an amplifier with voltage gain A and a frequency selective feedback network (having inductor or capacitive components) with the transfer ratio β. It may be noted that the loop in Fig. 12.1 is incomplete as the terminal 2 is not connected to terminal 1. To understand the operation of the circuit, consider the situation where an input signal V_i is applied at the input terminal 1 of the amplifier so that the output $v_0 = Av_i$. The feedback signal v_f at terminal 2, therefore, is $v_f = A\beta v_i$. The quantity $A\beta$, therefore, represents the loop gain of the system. If the values of A and β are adjusted so that $A\beta = 1$, the feedback signal v_f will be identically equal to the externally applied signal v_i. If the terminal 2 is

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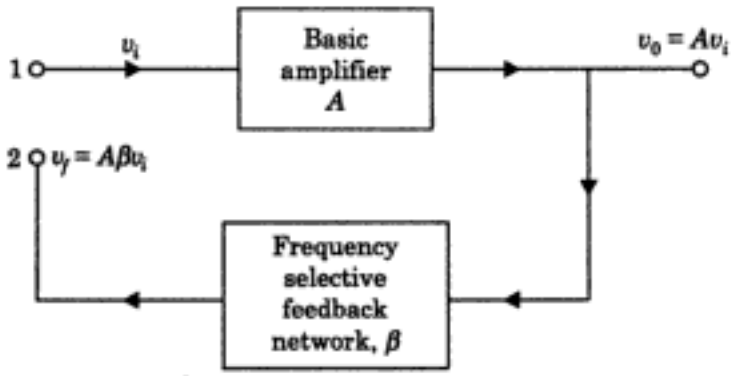


Fig. 12.1 Basic structure of a sine wave oscillator.

connected to terminal 1 and the external signal v_i is removed, the circuit will continue to give output signal as the amplifier can not distinguish whether v_i is coming from external source or from the feedback circuit. Thus, the output signal can be continuously obtained without any input signal if we can satisfy the condition on the loop gain, that is,

$$A\beta = 1 \tag{12.1}$$

This is called **Barkhausen criterion** for oscillations. The condition $A\beta = 1$ can be satisfied only at one specific frequency f_0. The circuit provides output at frequency f_0 only where the circuit components meets the condition given by Eq. (12.1). We may rewrite Eq. (12.1) as

$$A(j\omega_0)\ \beta(j\omega_0) = 1\angle 0° \tag{12.2}$$

There are infact two conditions in Eq. (12.2), one on phase and other on the magnitude of the loop gain which needs to be simultaneously satisfied to achieve oscillations. Thus, according to Eq. (12.2) the total phase shift of the loop gain should be zero or multiples of 2π and the magnitude of the loop gain, $A\beta$ should be equal to unity, that is,

$$|A\beta| = 1 \tag{12.3}$$

$$\angle A\beta = 0° \text{ or multiples of } 2\pi \tag{12.4}$$

The condition $|A\beta| = 1$ is usually difficult to maintain in the circuit as the values of A and β vary due to temperature variations, ageing of components, change of voltage and so on. If $|A\beta|$ becomes less than unity, the feedback signal v_f goes on reducing in each feedback cycle and the oscillations will die down eventually. In order to ensure that the circuit sustains oscillations inspite of variations, the circuit is designed so that $|A\beta|$ is slightly greater than unity. Now, the output amplitude will go on increasing with every feedback cycle. The signal, however can not go an increasing and gets limited due to the non-linearity of the device, that is as the transistor enters into saturation. Thus it is the non-linearity of the transistor because of which the sustained oscillations can be achieved. The value of $A\beta$ is usually kept greater by about 1 to 5% to ensure that $|A\beta|$ does not fall below unity. In explaining the principle of oscillation in Fig. 12.1, we had assumed that we first connect a signal source to start the oscillations and later remain it. In a practical oscillator, however, it is not done so. The output waveform is obtained as soon as power is turned on. Actually there is noise signal always present at the input (i.e. base) of the amplifier due to temperature (called Johnson's noise) or variation in the carrier concentration (Schottky noise). The noise signal at the frequency at which the circuit satisfies the condition $A\beta = 1$ is picked up and amplified. Since $A\beta > 1$ in the circuit, the output signal goes on increasing until it is limited by the onset of non-linearity of the transistor (as transistor enters into saturation) as shown in Fig. 12.2.

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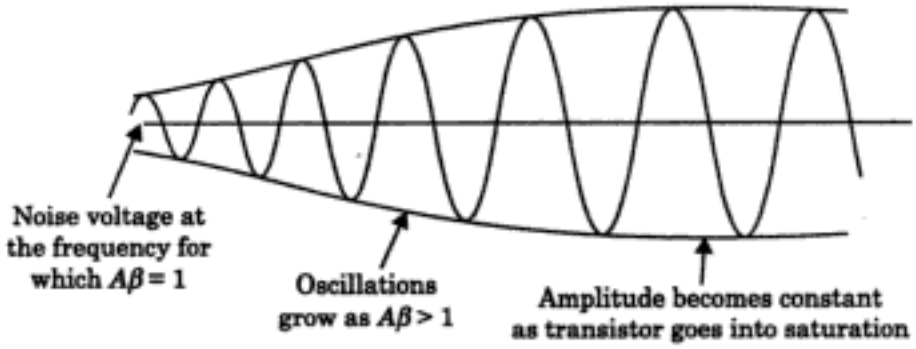

Noise voltage at the frequency for which $A\beta = 1$
Oscillations grow as $A\beta > 1$
Amplitude becomes constant as transistor goes into saturation

Fig. 12.2 Obtaining sustained oscillations from noise signal.

12.3 OSCILLATOR CIRCUITS

The various oscillator circuits can be broadly classified as:

1. RC oscillators
2. LC oscillators
3. Crystal oscillators.

The RC oscillators can provide frequencies varying from few hertz to several hundreds kHz. Two commonly used RC-oscillators are: (i) RC-phase shift oscillator, (ii) Wien-bridge oscillator. LC-oscillators are suitable for high frequencies upto hundreds of MHz. These oscillators use LC circuits as their tank or oscillatory circuit. The most popular LC-oscillators are, Hartley and Colpitts oscillators. Crystal oscillators provide highly stable frequencies, but at a fixed frequency.

12.3.1 RC Phase Shift Oscillator

The RC-phase shift oscillator can be designed using BJT or FET amplifier. We first consider an FET oscillator as there are no loading effects of feedback network on the FET amplifier due to the high input impedance of FET and it simplifies the analysis. Figure 12.3 shows the circuit of an FET oscillator which consists of a self-biased FET amplifier and a feedback network consisting of three cascaded RC sections.

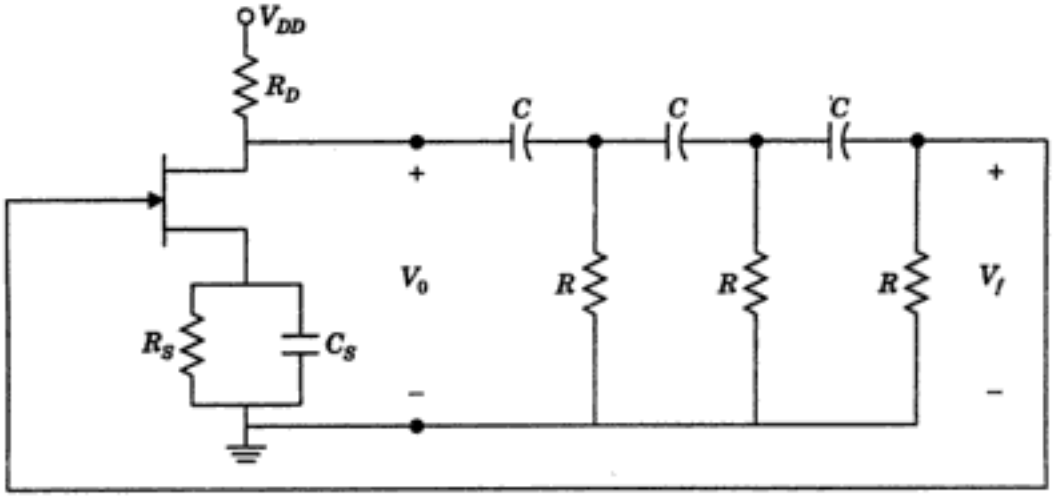


Fig. 12.3 FET phase shift oscillator.

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It can be seen that the feedback voltage V_f available at the output of the last RC section of the feedback network has been returned to the gate as input. As the FET amplifier provides 180° phase shift, the remaining 180° phase shift has to be provided by the feedback network to obtain a total of 360° phase shift round the loop. Thus, each RC section is selected so as to provide 60° phase shift at the desired frequency of oscillation. In practice, each section does not provide exactly a 60° phase shift due to loading of one RC section on the previous one. However, what one requires is a total phase shift of 180° from the feedback network.

The loop gain $A\beta$ can be computed by drawing the ac equivalent circuit as shown in Fig. 12.4(a). Here, the loop has been broken at the gate of FET and a voltage V_i is applied which gets amplified by the FET amplifier and appears as V_0. The output voltage V_0 is applied as input to the feedback network for which the output voltage is V_f. The circuit of Fig. 12.4(a) has been further simplified and is shown in Fig. 12.4(b), where the current source $g_m V_i$ has been replaced by the equivalent voltage source $g_m R_D' V_i$ where $R_D' = r_d \,||\, R_D$. Assuming that the feedback network does not load the amplifier, that is, for $R >> R_D'$, we may neglect the resistance R_D' in the simplified circuit of Fig. 12.4(b).

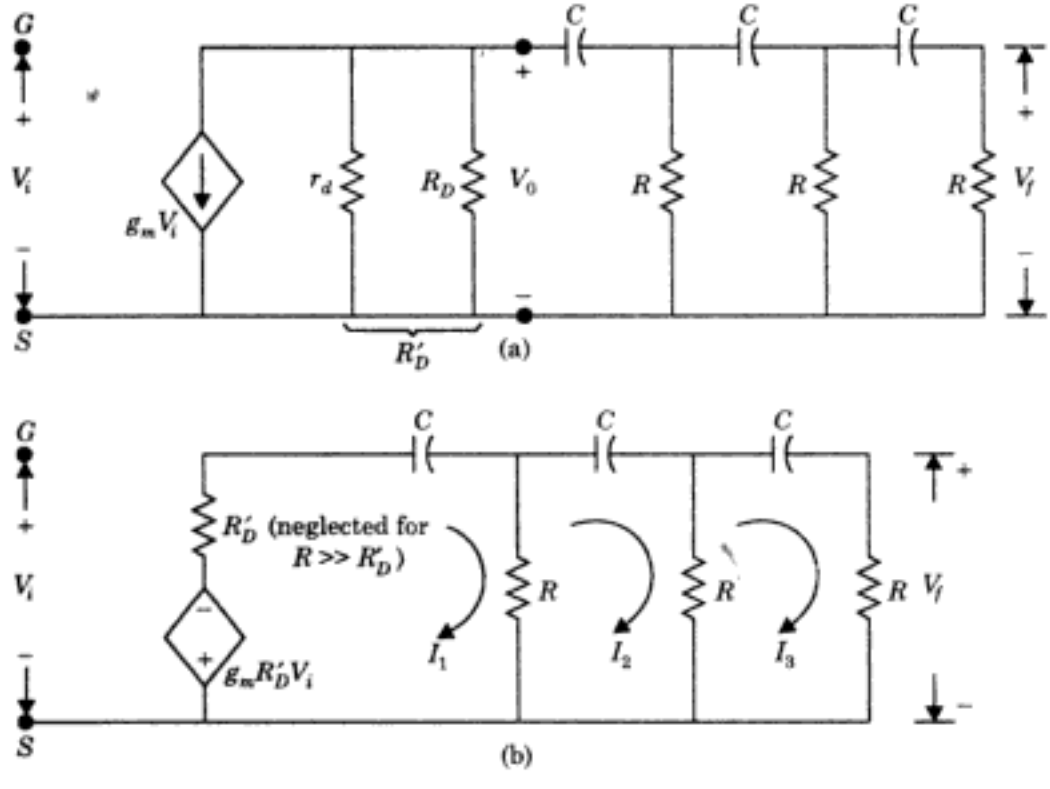


Fig. 12.4 (a) ac equivalent circuit, (b) simplified ac equivalent circuit.

The KVL equations for the three loops are:

Loop 1:

$$I_1\left(R + \frac{1}{sC}\right) - I_2 R = -g_m R_D' V_i \qquad [R_D' \text{ is neglected for } R >> R_D'] \tag{12.5}$$

Loop 2:

$$-I_1 R + I_2\left(2R + \frac{1}{sC}\right) - I_3 R = 0 \tag{12.6}$$

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Loop 3: $$-I_2R + I_3\left(2R + \frac{1}{SC}\right) = 0 \tag{12.7}$$

Also $$V_f = I_3R \tag{12.8}$$

Solving for loop gain $A\beta$, we get

$$A\beta = \frac{V_f}{V_i} = \frac{-g_m R'_D}{(1 - 5\alpha^2) + j(\alpha^3 - 6\alpha)} \tag{12.9}$$

where $$\alpha = \frac{1}{\omega RC} \tag{12.10}$$

As the loop gain $A\beta$ should be a real quantity (phase shift is zero), therefore, it is essential that $(\alpha^3 - 6\alpha)$ in the Eq. (12.9) should be zero, that is,

$$\alpha^3 - 6\alpha = 0$$

or $$\alpha^2 = 6$$

or $$\omega^2 R^2 C^2 = \frac{1}{6} \tag{12.11}$$

The frequency of oscillation f_0 is given by

$$f_0 = \frac{1}{2\pi RC\sqrt{6}} \tag{12.22}$$

Equation (12.9) thus becomes

$$|A\beta| = \frac{g_m R'_D}{29} \tag{12.13}$$

and since $|A\beta| > 1$ for sustained oscillations, therefore,

$$g_m R'_D > 29 \tag{12.15}$$

The voltage gain of the FET amplifier is given by

$$|A| = g_m R'_D \tag{12.14}$$

Therefore, $$|A| > 29 \quad \text{and} \quad \beta = \frac{1}{29} \tag{12.16}$$

Thus, the gain of the FET amplifier stage must be at least 29 to sustain oscillations.

If however, R'_D is not neglected in Fig. 12.4(b) then writing mesh equations again and solving, we get

$$A\beta = \frac{-jg_m R'_D \alpha^3}{1 - \alpha^2(6 + 4K) + j\alpha[5 + K - \alpha^2(1 + 4K)]} \tag{12.17}$$

where $$K = \frac{R'_D}{R} \tag{12.18}$$

For $A\beta$ to be a real quantity,

$$1 - \alpha^2(6 + 4K) = 0 \tag{12.19}$$

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or $$\alpha^2 = \frac{1}{6 + 4K}$$

which gives the frequency of oscillation as:

$$f_0 = \frac{1}{2\pi RC\sqrt{6 + 4K}} \tag{12.20}$$

Since $A\beta = 1$ at this frequency, we may write from Eq. (12.17)

$$\frac{g_m R'_D \alpha^2}{5 + K - \alpha^2(1 + 4K)} = 1 \tag{12.21}$$

Putting the value of α^2 and solving for gain, we get

$$|A| = g_m R'_D = 4K^2 + 22K + 29 \tag{12.22}$$

For $K = 0$ (when R'_D is neglected)

$$|A| = 29 \text{ as expected}$$

The RC feedback network can also be made using four RC sections and each section can be designed to provide 45° phase shift. However, this is not desirable as it will increase the number of components used. One could ideally obtain 180° phase shift by using only two RC sections. However, as it is not possible to get ideal capacitors, a single capacitor is not able to provide a phase shift of 90° exactly.

BJT phase shift oscillator: If a BJT is used as the active device in place of FET in the circuit of Fig. 12.3, the resistance R of the feedback network comes in parallel to the low input resistance h_{ie} of the transistor. This reduces the effective value of R in the last section of the feedback network. To overcome this, we use the circuit shown in Fig. 12.5 where voltage shunt feedback has been used in place of voltage series feedback.

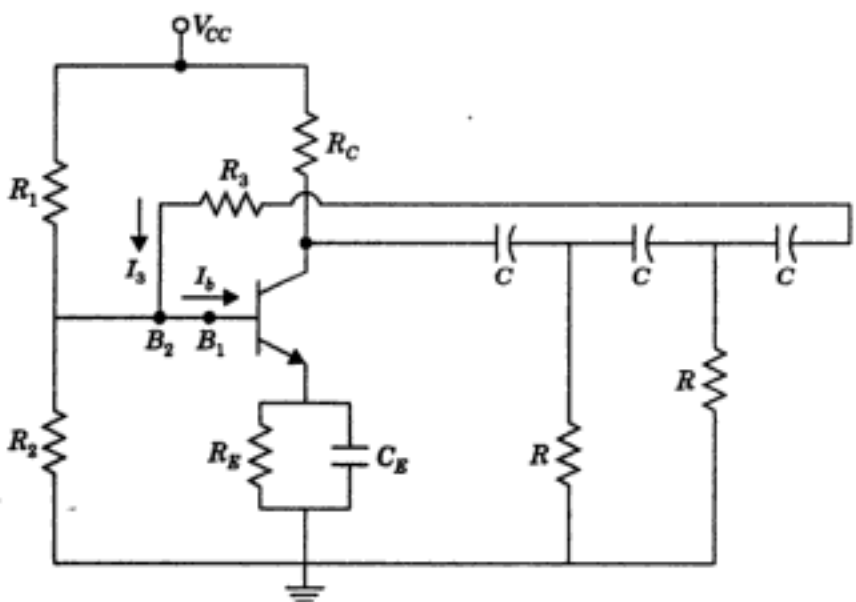


Fig. 12.5 BJT phase shift oscillator.

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account. These capacitances cause additional phase shift because of which design of the oscillator become quite complicated.

12.3.2 Wien Bridge Oscillator

The circuit of a Wien Bridge oscillator is shown in Fig. 12.7, where a 'balanced bridge' is used as the feedback network. The circuit will oscillate only at the frequency at which the bridge is balanced. The phase shift in the bridge at this frequency will be zero, so the phase shift produced by the amplifier circuit should also be zero to ensure that the phase shift round the loop is zero. This is the reason that a two-stage amplifier has been used in the circuit to provide zero phase shift.

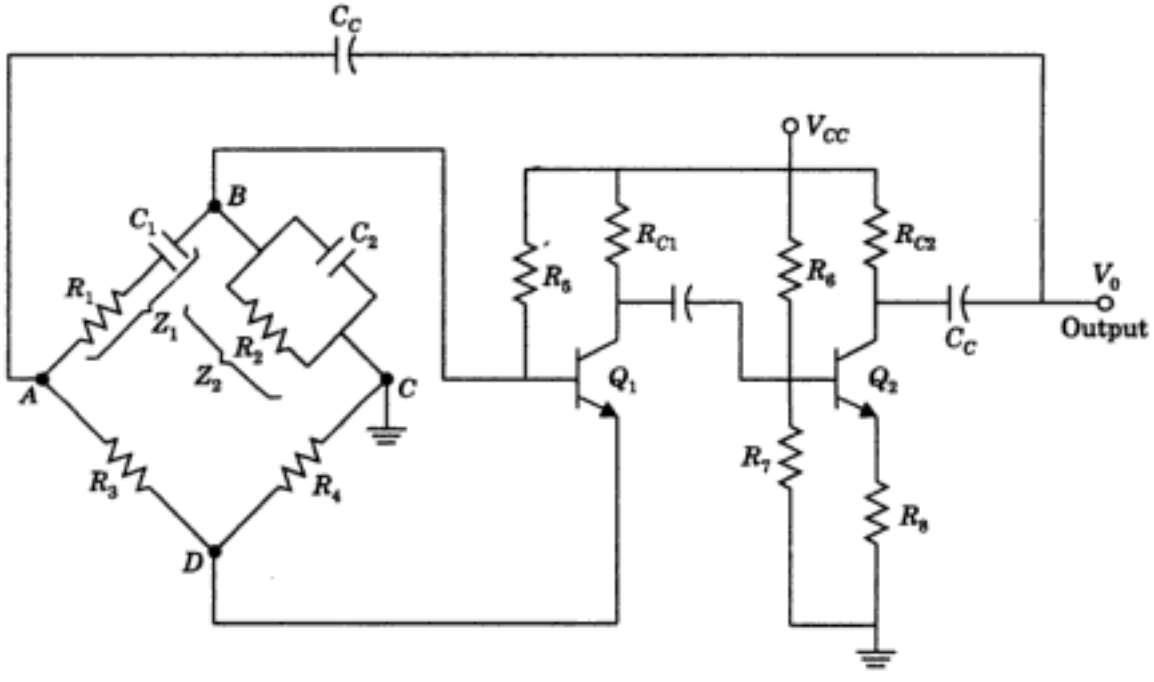


Fig. 12.7 Wien Bridge oscillator.

The output of the second stage is fed to the input terminals A and C of the bridge and the voltage across the parallel combination (R_2C_2) from the points B and C is fed as input to the first transistor stage. This input signal is in phase with the output due to transistors Q_1 and Q_2 and thus positive feedback is provided in the circuit.

The frequency of oscillation can be obtained from the feedback network shown in Fig. 12.8. The feedback factor β is:

$$\beta = \frac{Z_2}{Z_1 + Z_2} \tag{12.39}$$

where

$$Z_1 = R_1 + \frac{1}{sC_1} \tag{12.40}$$

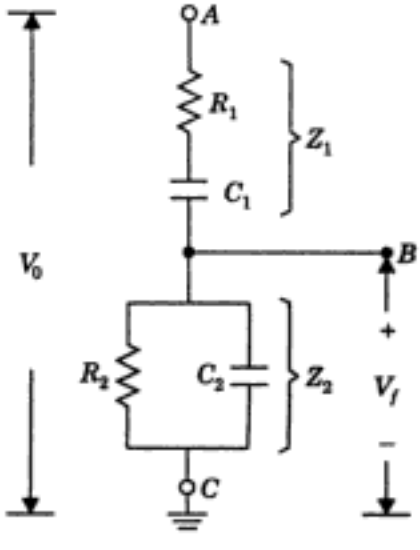


Fig. 12.8 Feedback network.

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The value of R should be much greater than R'_D to avoid loading, so choose R about 10 times greater than R'_D, say, 50 kΩ. So

$$C = \frac{8.1\,\mu s}{50\,k\Omega} = 162\ pF$$

EXAMPLE 12.2

Design a Wien Bridge oscillator to oscillate at a frequency of 2 kHz. Choose $R_1 = R_2 = R$ and $C_1 = C_2 = C$, and R should be greater than 1 kΩ.

Solution:

$$f_0 = \frac{1}{2\pi RC}$$

Say,

$$R = 10\ k\Omega$$

So

$$C = \frac{1}{2\pi \times 2 \times 10^3 \times 10 \times 10^3} = 7.96\ nF$$

For β to be 1/3, choose $R_3 = 2R_4$. We may choose $R_4 = 10$ kΩ so that $R_3 = 20$ kΩ.

12.3.3 LC Oscillator Circuits

There is a large variety of LC oscillators circuits available, such as tuned collector oscillator, tuned base oscillator, Colpitts oscillator, Hartley oscillator, clapp oscillator and crystal oscillator. We shall discuss more commonly used Hartley, Colpitts, Clapp and crystal oscillator circuits only.

Generalized oscillator circuit: A number of LC oscillator circuits can be analyzed by considering a generalized oscillator circuit shown in Fig. 12.9(a). The analysis assumes that the active element in Fig. 12.9(a) has high input impedance such as FET or an op-amp so that the feedback network does not load the amplifier. The ac equivalent circuit shown in Fig. 12.9(b) uses an amplifier with an open circuit voltage gain A_V and output resistance R_0, and with the loop broken at terminal 1.

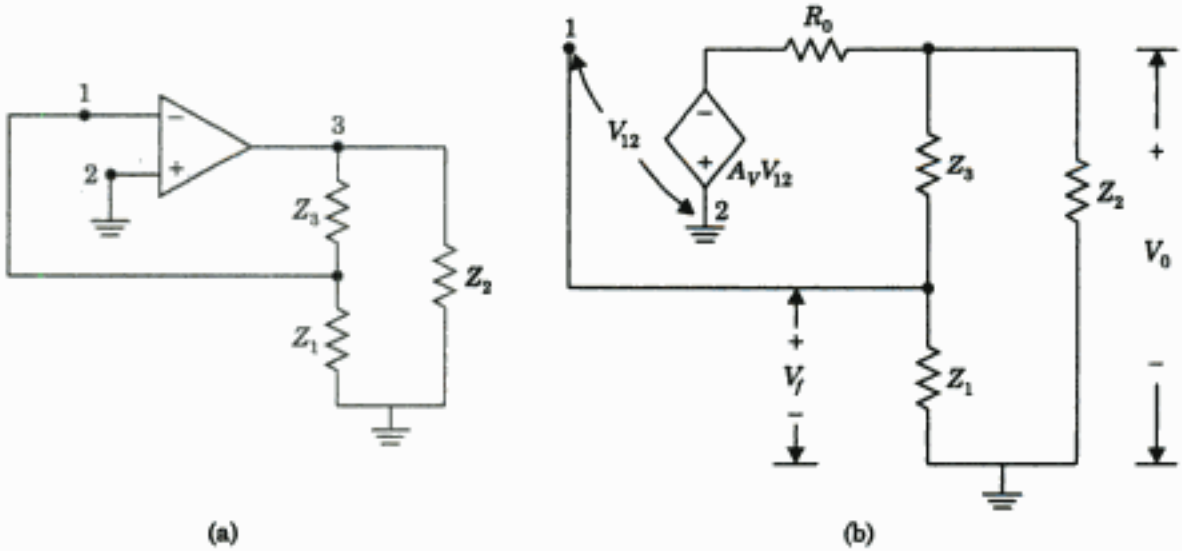


Fig. 12.9 (a) Generalized oscillator circuit, (b) ac equivalent circuit.

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at high frequencies should be used for exact analysis. For simplicity, we shall be using the above analysis only.

BJT versions of Colpitt's and Hartley oscillator are shown in Fig. 12.10. In the Colpitt's oscillator shown in Fig. 12.10(a),

$$X_1 = -\frac{1}{\omega C_1}; X_2 = -\frac{1}{\omega C_2} \quad \text{and} \quad X_3 = \omega L$$

Using Eq. (12.62),

$$X_1 + X_2 + X_3 = 0$$

or
$$-\left(\frac{1}{\omega C_1} + \frac{1}{j\omega C_2}\right) + \omega L = 0 \tag{12.63}$$

or
$$\omega L = \frac{1}{\omega C_1} + \frac{1}{\omega C_2} \tag{12.64}$$

The frequency of oscillation f_0 is:

$$f_0 = \frac{1}{2\pi\sqrt{L}}\sqrt{\frac{C_1 + C_2}{C_1 C_2}} \tag{12.65}$$

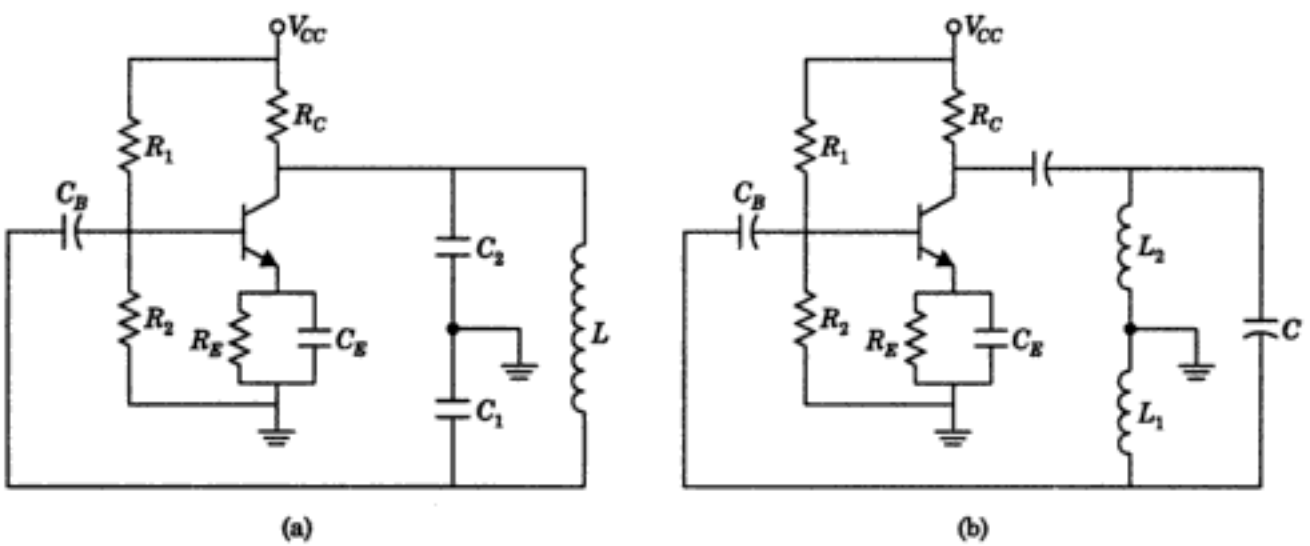


Fig. 12.10 (a) Colpitt's oscillator, (b) Hartley oscillator.

The condition on the voltage gain is obtained from Eq. (12.61).

Since $A\beta = 1$, therefore

$$A_V \frac{X_1}{X_2} = 1$$

or
$$A_V = \frac{X_2}{X_1}$$

i.e.
$$g_m R_C = \frac{C_1}{C_2}$$

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Thus, the magnitude of the voltage gain from base to collector ($g_m R_C$) must be equal to the ratio of capacitances. Of course for sustained oscillations, loop gain must be greater than unity, therefore

$$g_m R_C > \frac{C_1}{C_2}$$

As oscillations grow in amplitude, the non linear characteristics of the transistor reduce the effective value of g_m and reduces the loop gain to unity, thereby sustaining the oscillations.

Similarly, applying the condition of oscillation to the Hartley oscillator shown in Fig. 12.10(b) gives

$$f_0 = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}} \tag{12.66}$$

and

$$g_m R_C > \frac{L_2}{L_1}$$

Clapp oscillator: A modified form of Colpitts oscillator, shown in Fig. 12.11, is known as **clapp oscillator**. In this circuit, the inductor L has been replaced by a series combination of L and a capacitor C_3. Addition of capacitor C_3 improves the frequency stability of the circuit.

The frequency of oscillation is given as

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{LC_1} + \frac{1}{LC_2} + \frac{1}{LC_3}} \tag{12.67}$$

The frequency of oscillation can be varied by varying the capacitor C_3. As capacitor C_3 is usually much smaller than C_1 and C_2, the approximate frequency of oscillation can be given as:

$$f \simeq \frac{1}{2\pi}\sqrt{\frac{1}{LC_3}} \tag{12.68}$$

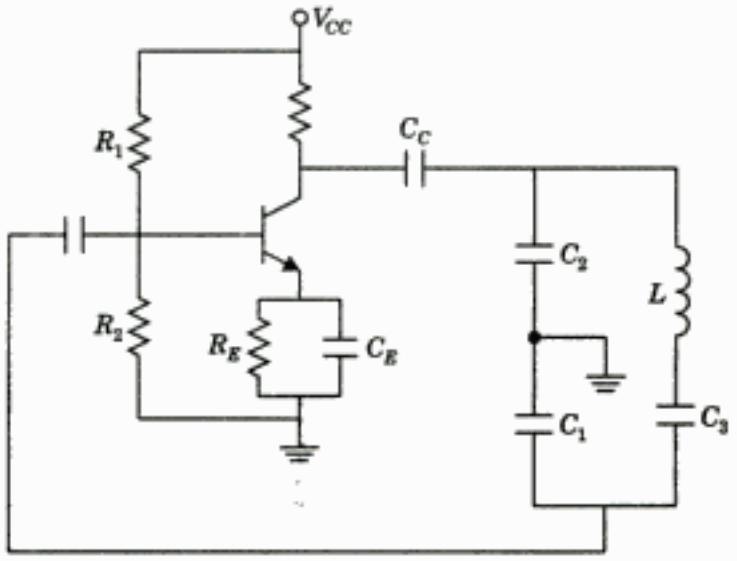


Fig. 12.11 A clapp oscillator.

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SUMMARY

- An oscillator circuit provides an ac output signal without applying any ac input signal.
- An oscillator can be made by using an amplifier and a frequency selective network in the feedback loop.
- The condition for oscillation is: loop gain $A\beta = 1$. This is called **Barkhausen criterion** for oscillations.
- In the condition $A\beta = 1$, the magnitude condition $|A\beta| = 1$ and the phase condition $\angle A\beta = 0°$ or multiples of 2π, both should be simultaneously satisfied to achieve oscillations.
- If $|A\beta| < 1$, the oscillations will die down.
- In practical oscillators, $|A\beta| > 1$ so as to ensure that the oscillations do not die due to variation in temperature, change of device or voltage changes.
- Noise voltage (thermal noise) at the input of the amplifier initiates the amplifying action.
- The output amplitude gets limited at the onset of non-linearity or as the transistor enters into saturation.
- An RC-phase shift oscillator uses three RC sections in cascade designed to provide 180° phase shift at the desired frequency of oscillation.
- The frequency of oscillation of an FET phase shift oscillator is, $f_0 = \dfrac{1}{2\pi RC\sqrt{6}}$ and the voltage gain of the amplifier should be greater than 29.
- The frequency of oscillation for a BJT phase shift oscillator is,

$$f_0 = \frac{1}{2\pi RC\sqrt{6 + 4K}}$$

where $K = R_C/R$ and the condition for oscillation is:

$$h_{fe} > 4K + 23 + \frac{29}{K}$$

- The minimum value of h_{fe} of a transistor in BJT phase shift oscillator is 45 for sustained oscillation.
- The voltage gain and frequency of oscillation for a Wien bridge oscillator are:

$$A > 3; \quad f_0 = \frac{1}{2\pi RC}$$

- The frequency of oscillation and condition of oscillation for a generalised oscillator circuit shown in Fig. 12.9 is

$$X_1 + X_2 + X_3 = 0$$

and

$$\frac{A_V X_1}{X_2} > 1$$

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- In Colpitt's oscillator, X_1 and X_2 are capacitors and X_3 is an inductor. The frequency of oscillation f_0 and condition for loop gain is given by

$$f_0 = \frac{1}{2\pi\sqrt{L}}\sqrt{\frac{C_1 + C_2}{C_1 C_2}}; \quad g_m R_C > \frac{C_1}{C_2}$$

- In Hartley oscillator, X_1 and X_2 are inductors and X_3 is a capacitor. The frequency of oscillator f_0 and condition for loop gain is given by

$$f_0 = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}; \quad g_m R_C > \frac{L_2}{L_1}$$

- A quartz crystal has electro-mechanical resonance characteristics with very high Q and, therefore, provides very stable frequencies.
- The quantity $d\theta/d\omega$ gives a measure of frequency stability of an oscillator. Larger the value of $d\theta/d\omega$, better the frequency stability.

REVIEW QUESTIONS

12.1 List some practical applications of ac signal sources.

12.2 Explain Barkhausen criterion for sustained oscillations.

12.3 Explain how oscillations are initiated in oscillators.

12.4 Explain the principle of operation of RC phase shift oscillator.

12.5 Find the frequency of oscillation and condition of oscillation for FET Phase shift oscillator.

12.6 Explain why three RC sections are needed in the phase shift oscillator.

12.7 Draw the circuit of a BJT phase shift oscillator. Explain the type of feedback used and why it is different from that used in FET oscillator.

12.8 Explain the working of a Wien Bridge oscillator. Derive the expression for frequency of oscillation and the value of the gain required for sustained oscillations.

12.9 Derive the condition of oscillation for the generalized oscillator using only reactive components.

12.10 Draw the circuit of Hartley and Colpitt's oscillator using BJT, and derive the expression for the frequency of oscillation, and condition on loop gain.

12.11 Explain the working of a crystal oscillator.

12.12 Derive and plot the impedance characteristics for a quartz crystal.

12.13 Define frequency stability. How it is computed?

NUMERICAL PROBLEMS

P12.1 An RC phase shift oscillator uses a JFET with the parameters: g_m = 5 m℧ and r_d = 50 kΩ. Determine R_D and C for R = 100 kΩ so that the circuit can oscillate at 10 kHz.

(***Ans.*** R_D = 6.56 kΩ, C = 65 pF)

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P12.2 Calculate the frequency of a BJT phase shift oscillator for $R = 6\ k\Omega$, $C = 1500\ pF$ and $R_C = 18\ k\Omega$.

(Ans. 4.2 kHz)

P12.3 Show that the frequency of oscillation of a Colpitt's oscillator, if the inductor L has a series resistance R, is given by

$$\omega_0 = \sqrt{\frac{RC_1 + R_0(C_1 + C_2)}{LC_1C_2R_0}}$$

P12.4 A Colpitt's oscillator is designed with $C_1 = 100\ pF$ and $C_2 = 7500\ pF$. Determine the range of inductor for the frequency to vary from 950 to 2050 kHz.

(Ans. 3.69 μH, 0.79 μH)

P12.5 In a Hartley's oscillator, the inductors L_1 and L_2 have a mutual inductance M. Show that the frequency of oscillation is given by

$$f_0 = \frac{1}{2\pi\sqrt{C(L_1 + L_2 + 2M)}}$$

P12.6 Determine the value of capacitor required so that a Hartley oscillator oscillates at a frequency of 450 kHz. Given: $L_1 = 1\ \mu H$, $L_2 = 100\ \mu H$ and $M = 50\ \mu H$.

(Ans. 0.83 μF)

P12.7 (a) Find the frequency of oscillation of an oscillator which uses the feedback network shown in Fig. 12.15.

(b) Draw the oscillator circuit.

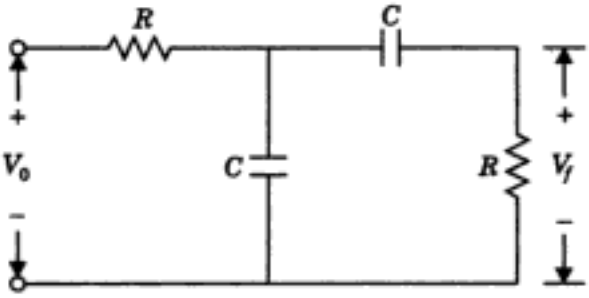


Fig. 12.15 Circuit for P12.7.

P12.8 A crystal has the following parameters: $L = 0.33$ H, $C_{series} = 0.065$ pF, $C_{parallel} = 1.0$ pF and R(inductor resistance) = 150 Ω. Find (a) the series resonant frequency (b) Q of the crystal.

(Ans. 1.098 MHz, 15000)

P12.9 Prove that the ratio of parallel to series resonant frequencies of a quartz crystal is approximately given by $\left(1 + \frac{1}{2}\frac{C_S}{C_p}\right)$.

P12.10 A 2 MHZ crystal is specified to have $L = 0.52$H, $C_s = 0.012$ pF, $C_p = 4$ pF and $r = 120\ \Omega$. Find f_s, f_p and Q.

(Ans. 2.015 MHz, 2.018 MHz, 55000)

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CHAPTER 13

Power Amplifiers and Voltage Regulators

13.1 INTRODUCTION

Most of the practical electronic systems consist of a number of amplifying stages in cascade. The function of the input and intermediate stages is to amplify the small signals received from an input source such as from a cassette or CD, microphone or from the antenna and amplify it to a large value sufficient to drive the final device which may be a loudspeaker in a public address system/music system or a cathode ray tube or a servo motor. The transistor in these stages is operated in the linear region so that the minimum distortion is added to the signal and small signal analysis is valid. Since signal voltages and currents are small, the power efficiency and power dissipation are of little concern.

There are, however, two very important requirements of the final stage or the output stage of any electronic system. Firstly, it should have a low output resistance so as to deliver the output signal to the load (final device) without any loss of signal. Further, since the output stage has to deliver large amount of power to the load in an efficient manner, it is necessary that the power dissipated in the output transistor is as low as possible. If the power delivered to the output transistor increases, its internal junction temperature will also increase and temperature beyond 150° to 200°C can destroy the silicon devices. Thus, an essential requirement of the output stage is that it should have a high power conversion efficiency. Power transistors with in-built heat sinks are usually used in the output stages. As input signal amplitude of the output stage is large, it is not possible to use small signal analysis. Therefore, the graphical analysis is carried out for the output stage as shall be seen.

Almost all electronic circuits require a dc source of power. It is necessary that the dc output voltage remain constant inspite of variations in load current, ac supply voltage or temperature. In this chapter, we also consider the regulator circuits used to provide a stable dc output voltage.

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Thus, for linear distortionless amplifier, the output power P can be calculated by reading the values of V_{max}, V_{min}, I_{max} and I_{min} on the load line drawn on the output characteristics as shown in Fig. 13.4.

13.3.1 Harmonic Distortion

In general, the static output characteristics are not parallel and equidistant for equal increments in input excitation i_b. Therefore, the dynamic transfer characteristics (i_c versus i_b) for a BJT is non-linear and not a straight line as assumed earlier. In such a case, the output voltage waveform will not be a perfect sine wave and has harmonics present in it. Such a distortion is called **non-linear** or **amplitude distortion**. The amount of distortion introduced will depend upon the non-linearity in the dynamic curve.

If we assume that the dynamic curve is represented by a point about the Q-point then the relation between i_c and i_b may be written as:

$$i_c = G_1 i_b + G_2 i_b^2 \tag{13.6}$$

where G_1 and G_2 are constants. Let the input i_b be a sinusoidal of the form:

$$i_b = I_{bm} \cos \omega t \tag{13.7}$$

Thus,
$$i_c = G_1 I_{bm} \cos \omega t + G_2 (I_{bm} \cos \omega t)^2$$

$$= G_1 I_{bm} \cos \omega t + \frac{1}{2} G_2 I_{bm}^2 (1 + \cos 2\omega t) \tag{13.8}$$

$$= \frac{1}{2} G_2 I_{bm}^2 + G_1 I_{bm} \cos \omega t + \frac{1}{2} G_2 I_{bm}^2 \cos 2\omega t$$

$$= B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t \tag{13.9}$$

where
$$B_0 = \frac{1}{2} G_2 I_{bm}^2 \tag{13.10}$$

$$B_1 = G_1 I_{bm} \tag{13.11}$$

$$B_2 = B_0 = \frac{1}{2} G_2 I_{bm}^2 \tag{13.12}$$

The total collector current i_C may be written as:

$$i_C = I_{CQ} + i_c \tag{13.13}$$

Putting the value of i_C from Eq. (13.9) in Eq. (13.13), we get

$$i_C = \underbrace{I_{CQ} + B_0}_{\text{DC term}} + \underbrace{B_1 \cos \omega t}_{\text{Fundamental}} + \underbrace{B_2 \cos 2\omega t}_{\text{Second Harmonic}} \tag{13.14}$$

The input current contains a term of the same frequency as the input (i.e., cost ωt term), a second harmonic term (i.e. cos $2\omega t$ term) and a constant (dc) term. It can be seen that the total dc component has increased from I_{CQ} to $I_{CQ} + B_0$. Thus, we can say that the parabolic dynamic curve given by Eq. (13.6) introduces a second harmonic component in the output and also since the average value of the output current has increased, rectification is also taking place.

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The amplitudes B_0, B_1 and B_2 can be found from the output characteristics shown in Fig. 13.4. As $B_0 = B_2$, we need to find only two unknown quantities, that is, B_0 and B_1. Rewriting Eq. (13.14) as:

$$i_C = I_{CQ} + B_0(1 + \cos 2\omega t) + B_1 \cos \omega t \tag{13.15}$$

In Fig. 13.4,

At $$\omega t = 0;\ i_C = I_{max} \tag{13.16}$$

and $$\omega t = \pi,\ i_C = I_{min} \tag{13.17}$$

Putting these in Eq. (13.15), we get

$$I_{max} = I_{CQ} + 2B_0 + B_1 \tag{13.18}$$

and $$I_{min} = I_{CQ} + 2B_0 - B_1 \tag{13.19}$$

Solving for B_0 and B_1, we get

$$B_0 = \frac{I_{max} + I_{min} - 2I_{CQ}}{4} \tag{13.20}$$

$$B_1 = \frac{(I_{max} - I_{min})}{2} \tag{13.21}$$

and $$B_2 = B_0$$

The second harmonic distortion D_2 is defined as:

$$D_2 = \left|\frac{B_2}{B_1}\right| \tag{13.22}$$

If the input i_b has two frequency components and is of the form $i_b = I_{bm1} \cos \omega_1 t + I_{bm2} \cos \omega_2 t$, then for the parabolic dynamic curve given in Eq. (13.6) will result in sinusoids of frequencies ω_1, $2\omega_1$, ω_2, $2\omega_2$, $\omega_1 + \omega_2$ and $\omega_1 - \omega_2$ besides the dc term.

Higher-order harmonic distortion: For large signal power amplifers, the assumption of parabolic dynamic characteristic is not justified and the dynamic transfer curve should be represented by a power-series of the form:

$$i_C = G_1 i_b + G_2 i_b^2 + G_3 i_b^3 + G_4 i_b^4 + \cdots \tag{13.23}$$

If $i_b = I_{bm} \cos \omega t$, the output current can be obtained in the form:

$$i_C = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_2 \cos 3\omega t + \ldots \tag{13.24}$$

Using proper trigonometric relations and simplifying it can be seen that the output current contains not only the second harmonic, but also third, fifth and other higher order harmonics. The amplitude of harmonics decreases as we go to higher order terms. The harmonic distortion is now defined as:

$$D_2 = \left|\frac{B_2}{B_1}\right|;\quad D_3 = \left|\frac{B_3}{B_1}\right|;\quad D_4 = \left|\frac{B_4}{B_1}\right|;\ \ldots \tag{13.25}$$

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and $$I_{c\ (\text{r.m.s. value})} = \frac{1}{\sqrt{2}} \frac{I_{max} - I_{min}}{2} = \frac{I_{max}}{2\sqrt{2}} = \frac{2I_{CQ}}{2\sqrt{2}} = \frac{I_{CQ}}{\sqrt{2}} \quad (13.47)$$

Thus, $$P_{ac} = \frac{V_{CC} I_{CQ}}{2} \quad (13.48)$$

and efficiency η is:

$$\eta = \frac{P_{ac}}{P_{dc}} \times 100\% \quad (13.49)$$

$$= \frac{V_{CC} I_{CQ}/2}{V_{CC} I_{CQ}} \times 100\% \quad (13.50)$$

$\therefore$ $$\boxed{\eta = 50\% \text{ (maximum)} \\ \text{for a transformer coupled class-A amplifier}} \quad (13.51)$$

EXAMPLE 13.1

Calculate the dc input power, ac output power and efficiency for the series fed amplifier circuit shown in Fig. 13.8, if the input signal results in a base current of 5 mA r.m.s.

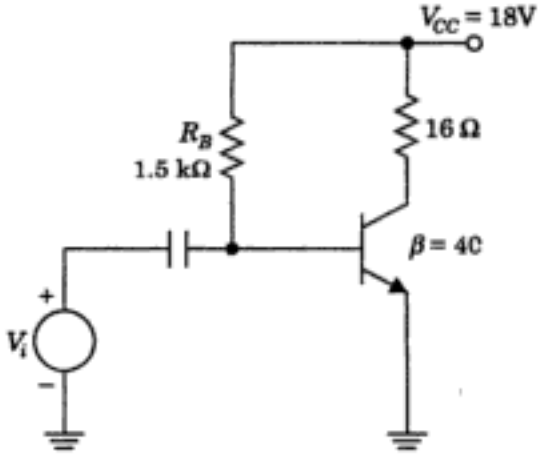


Fig. 13.8 Circuit for Ex. 1.

Solution: The Q-point is determined as:

$$I_{BQ} = \frac{V_{CC} - 0.7V}{R_B} = \frac{18V - 0.7V}{1.5\,k\Omega} = 11.5 \text{ mA}$$

$$I_{CQ} = \beta I_{BQ} = 40(11.5 \text{ mA})$$
$$= 0.46 \text{ A}$$

The dc input power is:

$$P_i \text{ (dc)} = V_{CC} I_{CQ}$$
$$= 18 \text{ V} \times 0.46 \text{ A} = 8.28 \text{ W}$$

The ac output power is given as

$$P_0(\text{ac}) = V_c I_c \quad \text{(r.m.s. values)}$$
$$= I_c^2 R_c$$

where $$I_c = \beta I_b$$
$$= 40 \times 5 \text{ mA} = 200 \text{ mA} = 0.2 \text{ A}$$

Therefore, $$P_0(\text{ac}) = (0.2A)^2 \times 16\ \Omega$$
$$= 0.04A \times 16\ \Omega$$
$$= 0.64 \text{ W}$$

$$\text{percentage, } \eta = \frac{P_0(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{0.64 \text{ W}}{8.28 \text{ W}} \times 100\% = 7.7\% \quad \textbf{Ans.}$$

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Figure 13.9 shows a class A push-pull amplifier which must use identical transistors Q_1 and Q_2 for proper operation. Another important requirement for the operation of a push-pull amplifier is to obtain two input signals, from the given input signal, which are equal in magnitude and have a phase difference of 180°. The most popular way of doing this is by using a centre-tapped transformer at the input as shown in Fig. 13.9. The output from the two transistors is connected to the load through an output centre-tapped transformer to provide impedance matching. The resistors R_1 and R_2 provide the voltage divider bias so that both transistors can work in class A operation. During the positive half cycle of the input, the signal at the base B_1 increases above the Q-point and decreases by the same amount at base B_2. Note that both the transistors are conducting all the time as both are biased for class A operation. Thus when collector current i_{C1} is increasing, current i_{C2} is decreasing. The current through the load will be proportional to the differences of i_{C1} and i_{C2} and forms the positive half cycle of the output waveform. Similarly, during the negative half cycle of the input, the signal at B_1 decreases and increases by the same amount at B_2,. The difference of i_{C1} and i_{C2} now produces the negative half cycle of the output waveforms. Such a circuit configuration has a number of advantages as we shall see.

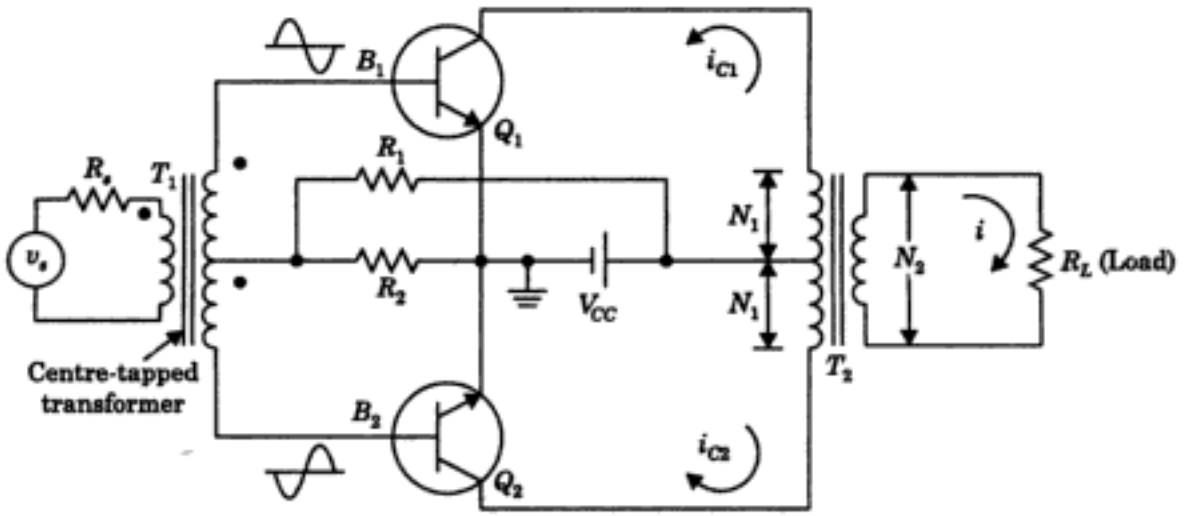


Fig. 13.9 Class A push-pull amplifier circuit.

The input signal v_s produces two voltage waveforms across the centre-tapped secondary of equal magnitude but 180° phase shift. These in turn produce input base currents i_{b1} and i_{b2} for transistors Q_1 and Q_2. If we assume that the input signal to transistor Q_1 is:

$$i_{b1} = I_{bm} \cos \omega t \tag{13.52}$$

The corresponding input signal to transistor Q_2 will be

$$\begin{aligned} i_{b2} &= -i_{b1} \\ &= I_{bm} \cos (\omega t + \pi) \end{aligned} \tag{13.53}$$

The output current i_{C1} for transistor Q_1 is given by Eqn. (13.24)

$$i_{C1} = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + \cdots \tag{13.54}$$

The output current i_{C2} for transistor Q_2 is obtained by replacing ωt by $\omega t + \pi$ in Eqn. (13.54). Thus,

$$i_{C2} = I_{CQ} + B_0 + B_1 \cos (\omega t + \pi) + B_2 \cos 2(\omega t + \pi) + \cdots \tag{13.55}$$

$$= I_{CQ} + B_0 - B_1 \cos \omega t + B_2 \cos 2\omega t - B_3 \cos 3\omega t + \cdots \tag{13.56}$$

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$$= \frac{2V_{CC}^2}{\pi R_L'} \qquad \left(\because I_m = \frac{V_{CC}}{R_L'}\right) \tag{13.60a}$$

AC power output, for peak amplitude V_m is:

$$P_{ac} = V_c I_c \tag{13.61}$$

$$= \frac{V_m}{\sqrt{2}} \frac{I_m}{\sqrt{2}} \tag{13.62}$$

$$= \frac{V_m I_m}{2} \tag{13.63}$$

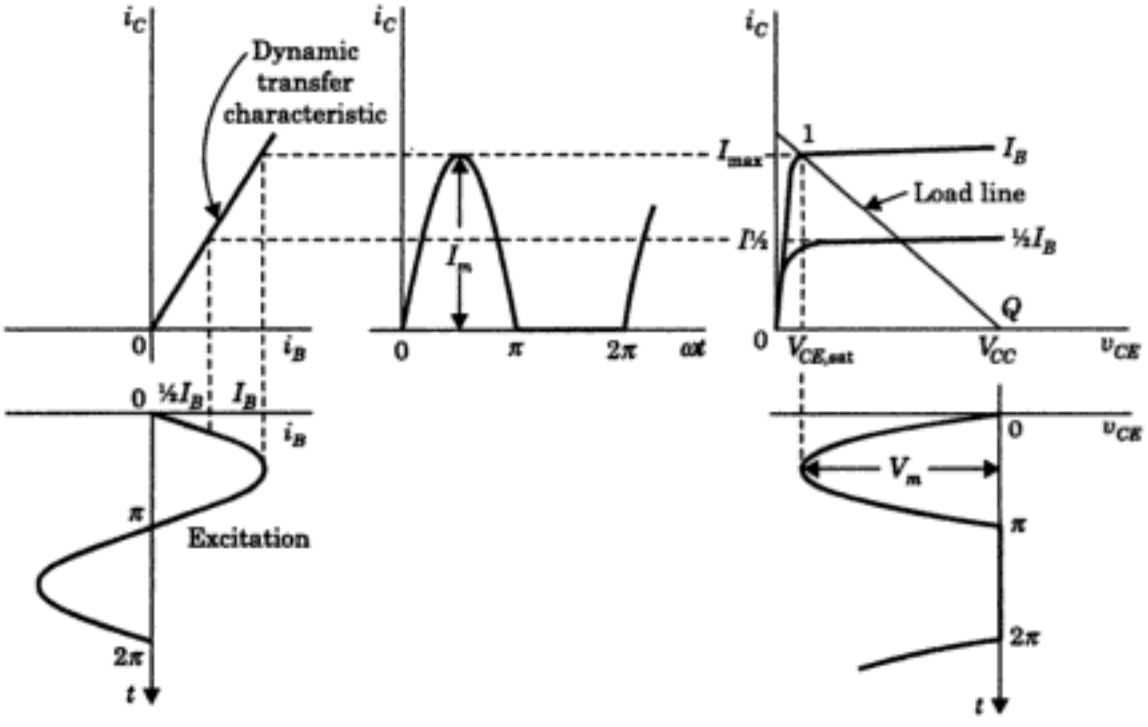


Fig. 13.10 Graphical construction for determining the output waveforms of a single class B transistor stage.

It can be seen that the maximum efficiency is obtained when peak voltage V_m is at its maximum possible value. This maximum value is limited by saturation and can be seen to be $V_{CC} - V_{CE(sat)} \simeq V_{CC}$. Therefore, the maximum ac power output can be given as:

$$P_{ac,max} = \frac{V_{CC} I_m}{2} \tag{13.64}$$

Maximum conversion efficiency η_{max} is:

$$\eta_{max} = \frac{P_{ac,max}}{P_{dc}} \tag{13.65}$$

$$= \frac{V_{CC} I_m \pi}{2 \times 2 I_m V_{CC}} \times 100\% \qquad \left(\because P_{dc} = \frac{2I_m}{\pi} V_{CC}\right) \tag{13.66}$$

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Thus, $$V_m\big|_{P_{D,\max}} = \frac{2}{\pi} V_{CC} \tag{13.75}$$

Putting the value of V_m from Eq. (13.75) in Eq. (13.71), we get

$$\boxed{P_{D,\max} = \frac{2V_{CC}^2}{\pi^2 R_L'}} \tag{13.76}$$

The efficiency, η at this value of V_m is obtained as

$$\eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{V_m I_m / 2}{2 \,.\, V_{dc} \,.\, I_{dc}} \times 100 = \frac{V_m I_m / 2}{2 \,.\, V_{CC} (I_m / \pi)} \times 100$$

or $$\eta = \frac{\pi}{4} \frac{V_m}{V_{CC}} \times 100\% \tag{13.77}$$

$$= \frac{\pi}{4} \frac{2V_{CC}}{\pi V_{CC}} \times 100\% \qquad \left(\because V_m = \frac{2}{\pi} V_{CC}\right) \tag{13.78}$$

$$= 50\%$$

It can be seen from Fig. 13.11 that as V_m is increased beyond $\frac{2V_{CC}}{\pi}$, the power dissipated decreases and the efficiency increases to 78.5%. However, the non-linear distortion increases as we go towards saturation which will flatten or clip the output waveform.

***Advantages of Class B* over class A amplifier**

1. Greater output power,
2. Greater efficiency,
3. For no signal (i.e. $v_i = 0$) the power loss is zero.

***Disadvantages* of class *B* over class *A* amplifier**

1. Harmonic distortion may be higher
2. The supply voltages need good regulation since the collector current increases from 0 to $V_{CC}/(\pi R_L)$ when v_i increases from 0 to maximum.

13.5.3 Class AB Operation

Although class B push-pull amplifier can provide high efficiency but the output waveform get distorted due to the non-linearity of the input characteristics (v_{BE} v/s i_B). We know that the base current starts flowing only after the base-emitter junction is forward biased by a voltage greater than the cut-in voltage ($V_\gamma = 0.5$ V for Si). The distortion caused by this is shown in Fig. 13.12 and is called **cross-over distortion**. This distortion can be eliminated if a perfect sinusoid base current could be provided in place of sinusoidal base voltage.

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13.7 THERMAL CONSIDERATIONS

Transistors meant to be used in power amplifiers are required to conduct large currents and also dissipate high power without getting damaged. Thus, their physical structure, packaging and specifications are different from the transistors used for small signal applications. Some of the parameters of interest for power transistors are:

Junction temperature: Power transistors dissipate large amount of power in their collector-base junctions. The dissipated power gets converted into heat which raises the junction temperature. The junction temperature T_j should not be allowed to exceed the maximum junction temperature $T_{j,\max}$ supplied in the data sheet otherwise the transistor will get damaged. For Ge transistors, $T_{j,\max}$ lies in the range 100–110°C whereas Si transistors can withstand temperature from 150°–200°C.

Thermal resistance: For a transistor dissipating P_D watts, the rise of the junction temperature, T_j relative to the surrounding ambient temperature T_A can be expressed as:

$$T_j - T_A = \theta_{jA} P_D \tag{13.80}$$

where θ_{jA} is the thermal resistance between junction and ambience and has the units of °C/watt.

As we wish to dissipate large amount of power without raising the junction temperature above $T_{j,\max}$, it is desirable that θ_{jA} be as small as possible. Equation (13.80) describes the thermal conduction process and is analogous to ohm's law which describes the electrical conduction process. The transistor manufacturer usually specifies $T_{j,\max}$, the maximum power dissipation at a particular ambient temperature, usually 25°C, T_{A0} and the thermal resistance θ_{jA}. In addition, a graph between P_D and ambient temperature, as shown in Fig. 13.16, is also provided.

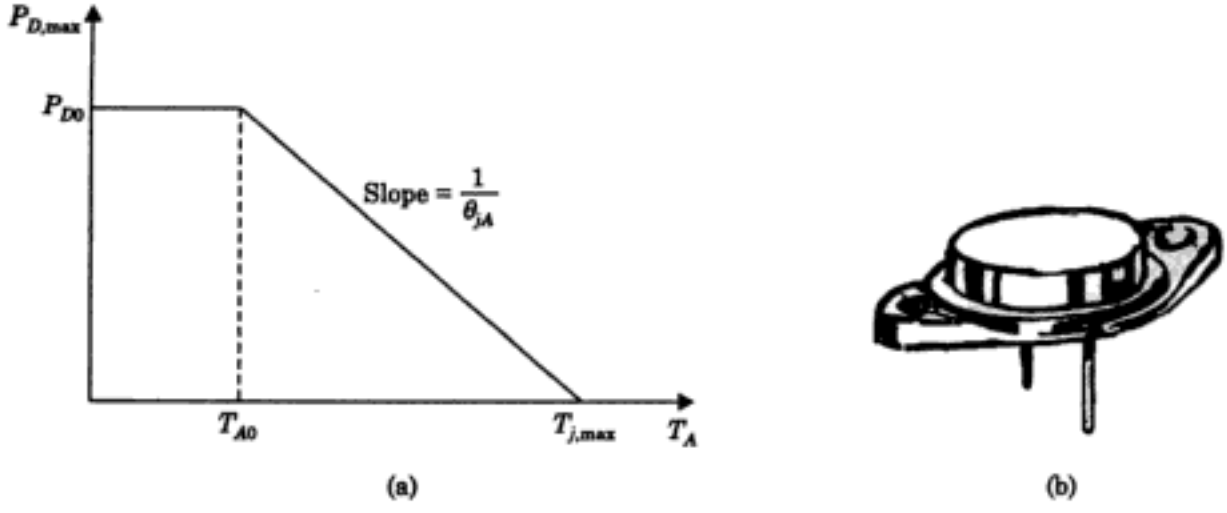


Fig. 13.16 (a) Power derating curve showing maximum allowable power dissipation versus ambient temperature, (b) The popular To –3 package for power transistors.

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The graph shows that below the ambient temperature T_{A0}, the device can safely dissipate the rated value of P_{D0} watts. If, however, the device is operated at higher ambient temperature then the maximum allowable power dissipated has to be reduced or derated. The power derating curve shown in Fig. 13.16(a) is a graphical representation of Eq. (13.80). Specifically, if ambient temperature is T_{A0} and power dissipation is at the maximum allowed (P_{D0}) then the junction temperature will be $T_{j,max}$. Substituting these quantities in Eqn. (13.80) gives

$$\theta_{jA} = \frac{T_{j,max} - T_{A0}}{P_{D0}} \tag{13.81}$$

If the ambient temperature T_A is higher than T_{A0}, the maximum allowable power dissipation $P_{D,max}$ can be obtained from Eq. (13.81).

EXAMPLE 13.6

A particular transistor has a power rating at 25°C of 200 mW, and a maximum junction temperature of 150°C. What is its thermal resistance? What is its power rating when operated at an ambient temperature of 70°C? What is the junction temperature when dissipating 100 mW at an ambient temperature of 50°C?

Solution: Using Eq. (13.81),

$$\theta_{jA} = \frac{T_{j,max} - T_{A0}}{P_{D0}}$$

$$= \frac{150 - 25}{200} = 0.625 \text{ °C/mW} \quad \textbf{Ans.}$$

Power rating at 70°C is:

$$= \frac{150 - 70}{0.625} = 128 \text{ mW} \quad \textbf{Ans.}$$

T_j, junction temperature at 100 mW is calculated as:

$$= 50 + 0.625 \times 100 = 112.5°\text{C} \quad \textbf{Ans.}$$

Transistor case and heat sink: The thermal resistance between junction and ambience, θ_{jA}, can be expressed as:

$$\theta_{jA} = \theta_{jC} + \theta_{CA} \tag{13.82}$$

where θ_{jC} = Thermal resistance between junction and transistor case (package)

θ_{CA} = Thermal resistance between case and ambience

The quantity θ_{jC} is fixed by the device design and packaging. The value of θ_{CA} can, however, be reduced by encapsulating the transistor in a relatively large metal case and placing the collector (where most of the heat is dissipated) in direct contact with case. Most of the high-power transistors are packaged in this fashion as shown by a typical package in Fig. 13.16(b). It has a metal case of about 2.2 cm, and the outside dimension of the 'seating plane' is about 4 cm. The seating plane is bolted on a metallic chasis or an extended metal surface called heat sink. The collector is electrically connected to the case. Thus heat is transferred by conduction and radiation from the transistor case to the heat sink so that θ_{CA} is very small.

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The fraction of the output voltage βV_0 is compared with the reference voltage V_{ref}. The difference $\beta V_0 - V_{ref}$ is amplified by transistor Q_2. If the output voltage increases, the sampled voltage βV_0 also increases. This increases the base emitter voltage of transistor Q_2 (as V_{ref} is fixed). If Q_2 conducts more current (I_2), the base current of Q_1 ($I_1 - I_2$) reduces which in turn reduces the load current thereby reducing the output voltage and maintaining the output voltage constant.

In Fig. 13.17, the output dc voltage V_0 is given by

$$V_0 = V_{ref} + V_{BE2} + \frac{R_1}{R_1 + R_2} . V_0$$

Simplifying, we get

$$V_0 = (V_{ref} + V_{BE2})\left(1 + \frac{R_1}{R_2}\right)$$

As
$$\beta = \frac{R_2}{R_1 + R_2} = \frac{1}{1 + R_1/R_2}$$

So
$$V_0 = \frac{(V_{ref} + V_{BE2})}{\beta}$$

As V_{ref}, V_{BE2} and β are all constants, therefore V_0 is also constant i.e. V_0 is stabilised and well regulated inspite of other variations.

13.8.2 Switching Regulator

The regulated power supplies discussed so far are referred to as linear voltage regulators, since the series pass transistor operates in the linear region. The linear voltage regulator has the following limitations:

The input stepdown transformer is bulky and is the most expensive component of the linear regulated power supply mainly because of low line frequency (50 Hz). Because of the low line frequency, large values of filter capacitors are required to decrease the ripple. The efficiency of a series regulator is usually very low (typically 50%). The input voltage must be greater than the output voltage. The greater the difference in input-output voltage, more will be the power dissipated in the series pass transistor which is always in the active region. A TTL system regulator (V_0 = 5 V) when operated at 10 V dc input gives 50% efficiency and only 25% for 20 V dc input. Another limitation is that in a system with one dc supply voltage (such as +5 V for TTL) if there is need for ±15 V for op-amp operation, it may not be economically and practically feasible to achieve this.

Switched mode power supplies overcome these difficulties. The switching regulator, also called **switched-mode regulator,** operate in a significantly different way from that of conventional series regulator circuit discussed earlier. In series regulator, the pass transistor is operated in its linear region to provide a controlled voltage drop across it with a steady dc current flow. Whereas, in the case of switched-mode regulator, the pass transistor is used as a *controlled switch* and is operated at either cutoff or saturated state. Hence the power transmitted across the pass device is in discrete pulses rather than as a steady current flow. Greater efficiency is achieved in this case, since the pass device is operated as a low impedance switch. When the pass device is at cutoff, there is no current and dissipates no power. Again when the pass device is in saturation, a negligible voltage drop appears across it and thus

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it dissipates only a small amount of average power, providing maximum current to the load. In either case, the power wasted in the pass device is very little and almost all the power is transmitted to the load. Thus, the efficiency in switched-mode power supply is remarkably high—in the range of 70–90%.

Switched-mode regulators rely on pulse width modulation to control the average value of the output voltage. The average value of a repetitive pulse waveform depends on the area under the waveform. If the duty cycle is varied as shown in Fig. 13.18a, b, c, the average value of the voltage changes proportionally, shown by V_{av} in these figures.

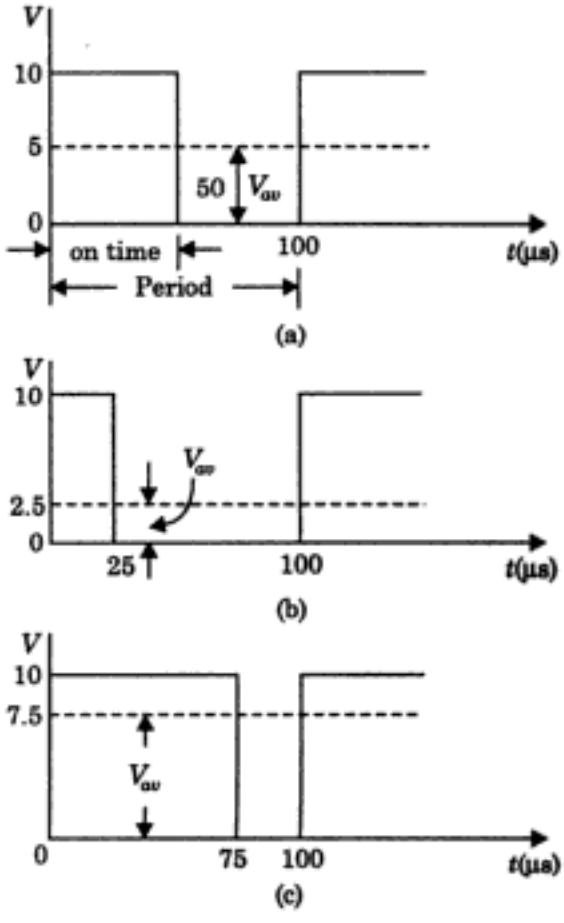


Fig. 13.18 Pulse width modulation and average value.

A switching power supply is shown in Fig. 13.19. The bridge rectifier and capacitor filters are connected directly to the AC line to give unregulated dc input. The thermistor R_t limits the high initial capacitor charge current. The reference regulator is a series pass regulator of the type shown in Fig. 13.17. Its output is a regulated reference voltage V_{ref} which serves as a power supply voltage for all other circuits. The current drawn from V_{ref} is usually very small (~10 mA), so the power loss in the series pass regulator does not affect the overall efficiency of the switched-mode power supply (SMPS). Transistors Q_1 and Q_2 are alternately switched off and on at 20 kHz. These transistors are either fully on ($V_{CE\,sat}$ ~0.2 V) or cutoff, so they dissipate very little power. These transistors drive the primary of the main transformer. The secondary is centre-tapped and full wave rectification is achieved by diodes D_1 and D_2. This unidirectional square wave is next filtered through a two stage LC filter to produce output voltage V_0.

The regulation of V_0 is achieved by the feedback circuit consisting of a pulse-width modulator (PWM) and steering logic circuit. The output voltage V_0 is sampled by a R_1R_2 divider and a fraction $R_1/(R_1 + R_2)$ is compared with a fixed reference voltage V_{ref} in comparator 1. The output of this voltage comparison amplifier is called $V_{control}$ and is shown in Fig. 13.18(a). $V_{control}$ is applied to the (–) input terminal of comparator 2 and a triangular waveform of frequency 40 kHz [also shown in Fig. 13.20(a)] is applied at the (+) input terminal. It may be noted that a high frequency triangular waveform is being used to reduce the ripple. The comparator 2 functions as a pulse width modulator and its output is a square wave v_A [Fig.13.20(b)] of perod $T(f = 40$ kHz). The duty cycle of the square wave is $T_1/(T_1 + T_2)$ and varies with $V_{control}$ which in turn varies with the variation of v_0. The output v_A drives a steering logic circuit shown in the dashed block Fig. 13.19. It consists of a 40 kHz oscillator cascaded with a flip-flop to produce two complementary outputs v_Q and $v_{\bar{Q}}$ shown in Fig. 13.20(d) and (e). The output v_{A1} and v_{A2} of AND gates A_1 and A_2 are shown in Fig. 13.20(f) and (g). These waveforms are applied at the base of transistor Q_1 and Q_2. Depending upon whether transistor Q_1 or Q_2 is on, the waveform at the input of the transformer will be a square wave as shown in Fig. 13.20(h). The rectified output v_B is shown in Fig. 13.20(i).

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decreases the pulse width of the waveform driving the main power transformer. Reduction in pulse width lowers the average value of the dc output V_0. Thus, the initial rise in the dc output voltage V_0 has been nullified.

So far we have discussed the operation of the SMPS. Now, we shall be able to justify why SMPS has better efficiency than the linear regulated power supply. We have noted that very high frequency signals (about 40 kHz or more) are being applied. The transistors Q_1 and Q_2 are acting as the switches and become alternately ON and OFF at a frequency of 20 kHz [Fig. 13.20(a)]. Again the transistor Q_1 or Q_2 is ON for very small duration and consumes negligibly small power since $V_{CE(sat)}$ (0.2 V) is small. It may also be noted that the high operating frequency used for the switching transistors allows the use of smaller transformers, capacitors and inductors. This allows a decrease in size and cost.

There are some limitations and precautions to be taken with the switching power supplies. Since the rectifier is tied directly to the ac line voltage, the rectifiers, capacitors and switching transistors must be able to withstand the peak line voltage (310 V for 220 V AC rms line). The resistor R_t must be provided to prevent the uncharged capacitors from shorting out the line when initially turned on. A switched mode power supply is more complex and requires external components like inductors and transformers. It is slow in responding to transient load changes compared to the conventional series regulator. One should be careful about the electromagnetic and radio-frequency interference while using switched mode power supply.

SUMMARY

- The final stage or output stage of any electronic system is a power amplifier or large signal amplifier.
- A power amplifier should have low output resistors so as to deliver maximum power to load.
- Amplifiers can be classified according to the transistor conduction angle: class A (conduction is for 360°); class B (conduction is for half cycle, i.e., 180°); class AB (greater than 180° but less than 360°): class C (less than 180°).
- For large input signals, the dynamic transfer characteristics of a transistor is non-linear and, therefore, produces harmonic distortion in the output.
- The harmonic distortion components are found graphically from the output characteristics of the transistor.
- A class A amplifier stage dissipates maximum power under dc quiescent conditions.
- The maximum power conversion efficiency of a class A amplifier is 25% only and, therefore, is not used as power amplifier.
- The efficiency of a class A amplifier can be increased to 50%, if load is coupled through a transformer in class A amplifier.
- A push-pull amplifier requires two signals of equal magnitude but with 180° phase differences. This is obtained by using a centre-tapped input transformer.
- All the even harmonics get cancelled in a push-pull amplifier stage.
- A class B push-pull amplifier can provide a maximum conversion efficiency of 78.5%.

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13.11 Draw the circuit of a transformerless class B push-pull amplifier.

13.12 What is crossover distortion? How it can be minimized?

13.13 Explain the terms (i) Junction temperature (ii) Thermal resistance (iii) Power derating curve.

13.14 Explain the need of voltage regulator.

13.15 What is the difference in series regulator and switching regulator.

13.16 Explain why SMPS has better efficiency than a linear regulator.

NUMERICAL PROBLEMS

P13.1 For the circuit shown in Fig. 13.21, calculate the dc input power, ac power output, efficiency if the input voltage results in a base current of 10 mA peak.

(***Ans.*** 9.65 W, 0.625 W, 6.48%)

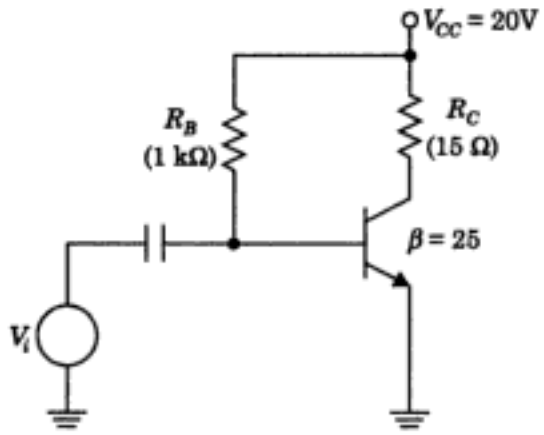


Fig. 13.21 Circuit for P-13.1

P13.2 A transistor supplies 2 W to a 4 kΩ load. The zero signal collector current I_{CQ} is 30 mA and the dc collector current with signal is 35 mA. Determine the percent second harmonic distortion.

(***Ans.*** 15.81%)

P13.3 Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.1 V, second harmonic amplitude of 0.3 V, third harmonic component of 0.1 V and fourth harmonic component of 0.05 V.

(***Ans.*** D_2 = 14.3%, D_3 = 4.8%, D_4 = 2.4%)

P13.4 Calculate the second harmonic distortion for an output waveform if $V_{CE,\min}$ = 2.4 V, V_{CEQ} = 10 V and $V_{CE,\max}$ = 20 V.

(***Ans.*** $\%D_2$ = 6.8%)

P13.5 What turns ratio transformer is needed to couple to an 8 Ω load so that it appears as an 8 kΩ effective load?

(***Ans.*** 31.6)

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